PHILIPS

Data handbook

PHILIPS

Electronic
components
and materials

Semiconductors

Book S9

1988

PowerMOS transistors

Elcoma – Philips Electronic Components and Materials Division – embraces a world-wide group of companies operating under the following names:

IBRAPE
Miniwatt
Mullard
PHILIPS
RTC
Signetics
VALVO

Elcoma offers you a technological partnership in developing your systems to the full. A partnership to which we can bring

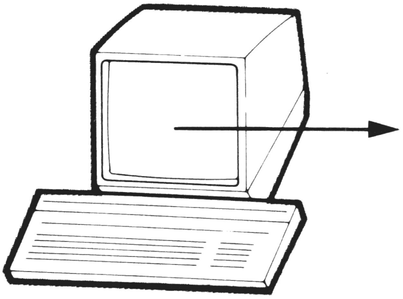
- world-wide production and marketing
- know-how
- systems approach
- continuity
- broad product line
- fundamental research
- leading technologies
- applications support
- quality

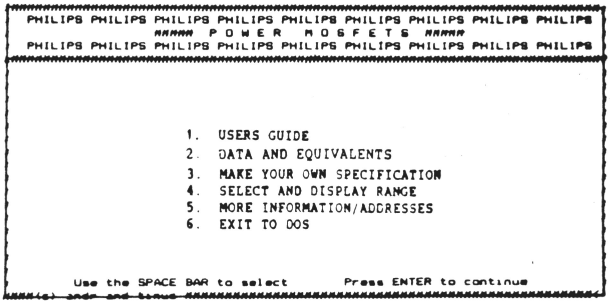
POWER AT YOUR FINGERTIPS

Do you have access to a PC compatible*?
If so, then you also have a quicker access to the Philips PowerMOS range.
We can send you a free floppy disc containing all the information you need on PowerMOS. Inserting the floppy into your PC allows you access to functions which:

- Give you a full list of transistor types and applications
- Give you a list of Philips equivalent types
- Allow you to make your own specifications
- Give you information/addresses of all the Philips National Organizations

You may also copy this disc freely





```
PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS
              ##### P O W E R   M O S F E T S #####
PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS PHILIPS



                  1.  USERS GUIDE
                  2.  DATA AND EQUIVALENTS
                  3.  MAKE YOUR OWN SPECIFICATION
                  4.  SELECT AND DISPLAY RANGE
                  5.  MORE INFORMATION/ADDRESSES
                  6.  EXIT TO DOS


     Use the SPACE BAR to select          Press ENTER to continue
```

Please send me a free copy of the **"PowerMOS at your fingertips"** floppy.

Name and Address of Company: ______________________________

Your function within the company: ______________________________

Size of the Company: ______________________________

Main activity of the Company: ______________________________

Philips International B.V.
Elcoma – M.C. dept.
Geb. BA – PO box 218
5600 MD EINDHOVEN
The Netherlands

PowerMOS transistors

POWERMOS INTRODUCTION 3
POWERMOS SELECTION GUIDE 59
POWERMOS DEVICE DATA 65

POWERMOS INTRODUCTION

PowerMOS Introduction

CONTENTS *page*

1 POWERMOS TECHNICAL DATA 9
- 1.1 Device structure 9
- 1.2 Device operation 11
- 1.3 Threshold voltage 11
- 1.4 Drain-source on-state resistance 11
- 1.4.1 Channel 12
- 1.4.2 Accumulation layer 12
- 1.4.3 Parasitic JFET 12
- 1.4.4 Spreading resistance 12
- 1.4.5 Epitaxial layer 12
- 1.4.6 Substrate 12
- 1.4.7 Wires and leads 12
- 1.5 Drain-source breakdown voltage 12

2 INTRODUCTION TO POWER MOSFETS 13
- 2.1 What is a MOSFET? 13
- 2.2 The structure of present day power MOSFETs 14
- 2.3 Advantages of power MOSFETS 14
- 2.4 Applications of power MOSFETS 14
- 2.5 The characteristics of power MOSFETS 14
- 2.5.1 The dc characteristic 14
- 2.5.2 The Safe Operating Area 15
- 2.5.3 The switching characteristics 16
- 2.6 The parallel operation of power MOSFETS 17
- 2.7 The losses in power MOSFETS 17
- 2.8 Conclusions 17

3 POWER MOSFET DRIVE CIRCUITS 17
- 3.1 The requirements of the drive circuit 17
- 3.2 Non-isolated drive circuits 18
- 3.3 Isolated drive circuits 18
- 3.4 Parallel operation 22
- 3.5 Protection against gate-source overvoltages 22

4 THE SERIES OPERATION OF POWER MOSFETS 23
- 4.1 The current-fed inverter 24

5 **THE PARALLEL OPERATION OF PHILIPS POWER MOSFETS IN SWITCHING CIRCUITS** 27
- **5.1 Advantages of parallel operation of devices** 27
  - 5.1.1 Increased power handling capability 27
  - 5.1.2 Standardisation 27
  - 5.1.3 Increased operating frequency. 27
  - 5.1.4 Increased power dissipation 27
- **5.2 Advantages of power MOSFETS for parallel operation.** 28
  - 5.2.1 Reduced likelihood of thermal runaway 28
  - 5.2.2 Low drive power requirements 28
  - 5.2.3 Very good tolerance of dynamic unbalance 28
- **5.3 Design points** 28
  - 5.3.1 Derating 28
  - 5.3.2 Layout 28
  - 5.3.3 Good thermal coupling. 29
  - 5.3.4 The suppression of parasitic oscillations 29
  - 5.3.5 Resonant power supplies. 30
  - 5.3.6 The current-fed approach 30
  - 5.3.7 The parallel operation of MOSFETs in the linear mode 30
  - 5.3.8 Conclusions 30

6 **POWERMOS TRANSISTORS IN SMPS** 31
- **6.1 PowerMos structure and operation** 31
- **6.2 PowerMOS and SMPS** 33
- **6.3 Selection guide** 33
- **6.4 Designing with PowerMOS.** 35
  - 6.4.1 Switching frequency 35
  - 6.4.2 Switching-loss equation 36
  - 6.4.3 Circuit configuration options with PowerMOS 36
  - 6.4.4 Paralleling PowerMOS transistors 38

7 **HIGH SPEED MOSFET DRIVE CIRCUITS.** 39

8 **THE PROTECTION OF PHILIPS POWERMOS AGAINST ELECTROSTATIC DISCHARGE** 42

9 **POWERMOS QUALITY AND RELIABILITY** 44
- **9.1 PowerMOS quality** 44
- **9.2 PowerMOS wafer fab** 44
- **9.3 Process controls.** 45
- **9.4 Conformance assurance** 46
- **9.5 Reliability assurance** 46
  - 9.5.1 High temperature dc blocking. 47
  - 9.5.2 High temperature storage 47
  - 9.5.3 Temperature cycling 47
  - 9.5.4 Thermal fatigue (or power cycling). 47
  - 9.5.5 High temperature gate bias. 47
  - 9.5.6 Humidity with blocking voltage. 47
  - 9.5.7 Autoclave 47

10 EXPLANATION OF THE DATA SHEET PARAMETERS 47

10.1 MOS handling 47

10.2 Use of subscripts 47

10.2.1 Voltages 47

10.2.2 Currents 47

10.3 Absolute maximum ratings 48

10.3.1 Drain-source voltage V_{DS} 48

10.3.2 Drain-gate voltage V_{DGR} 48

10.3.3 Continuous drain current I_D. 48

10.3.4 Pulsed drain current I_{DM} 48

10.3.5 Gate-source voltage V_{GS} 48

10.3.6 Maximum power dissipation P_D. 48

10.3.7 Operating temperature range T_j 48

10.3.8 Storage temperature range T_{stg} 48

10.3.9 Maximum soldering temperature T_{sold}. 48

10.3.10 Thermal resistance $R_{th\,j\text{-}mb}$ 48

10.4 Electrical characteristics 48

10.4.1 Drain-source breakdown voltage $V_{(BR)DSS}$ 48

10.4.2 Gate threshold voltage $V_{GS(TO)}$ 48

10.4.3 Zero gate voltage drain current I_{DSS} 48

10.4.4 Gate-source leakage current I_{GSS} 48

10.4.5 Drain-source on-state resistance $R_{DS(ON)}$ 48

10.4.6 Forward transconductance g_{fs}. 48

10.4.7 Input capacitance C_{iss} 48

10.4.8 Output capacitance C_{oss} 48

10.4.9 Reverse transfer capacitance C_{rss} 49

10.4.10 Turn-on time 49

10.4.11 Turn-off time 49

10.5 Reverse diode characteristics 49

10.5.1 Continuous reverse drain current I_{DR} 49

10.5.2 Pulsed reverse drain current I_{DRM} 49

10.5.3 Diode forward on-voltage V_{SD} 49

10.5.4 Reverse recovery time t_{rr} and reverse recovery charge Q_{rr}. 49

10.5.5 Repetitive peak reverse current I_{RRM} 50

10.6 Diagrams 50

10.6.1 Power dissipation $P_D = f(T)$ 50

10.6.2 Typical output characteristic $I_D = f(V_{DS})$ 50

10.6.3 Safe operating area $I_D = f(V_{DS})$. 50

10.6.4 Typical transfer characteristic $I_D = f(V_{GS})$ 50

10.6.5 Typical on-state resistance $R_{DS(ON)} = f(I_D)$ 50

10.6.6 On-state resistance $R_{DS(ON)} = f(T_j)$ 50

10.6.7 Drain-source breakdown voltage $V_{(BR)\,DSS}$. 50

10.6.8 The typical transconductance, $g_{fs} = f(I_D)$ 50

10.6.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$ 50

10.6.10 Typical capacitances $c = f(V_{DS})$. 50

10.6.11 Drain current $I_D = f(T)$ 50
10.6.12 Typical and maximum forward characteristics of the "reverse diode" $I_F = f(V_{SD})$ 50
10.6.13 Transient thermal resistance $Z_{th\ j\text{-}mb} = f(t)$ 51
10.6.14 Typical gate-source voltage $V_{GS} = f(Q_{gate})$ 51
10.7 Test circuits 52
10.7.1 Drain current I_D, I_{DSS} 52
10.7.2 Drain-source on-state resistance $R_{DS(ON)}$ 52
10.7.3 Gate threshold voltage $V_{GS(TO)}$ 52
10.7.4 Gate-source leakage current I_{GSS} 52
10.7.5 Input capacitance C_{iss} 52
10.7.6 Output capacitance C_{oss} 53
10.7.7 Reverse transfer capacitance C_{rss} 53
10.7.8 Gate charge Q_{gate} 54

11 SOLDERING INSTRUCTIONS 54
11.1 Soldering data for the metal case TO3 54
11.2 Soldering data for the plastic package TO218, TO220 54

12 TYPE DESIGNATIONS 55
12.1 Pro electron type designation code for semiconductor devices 55
12.1.1 First letter 55
12.1.2 Second letter 55
12.1.3 Range numbers 55

13 RATING SYSTEMS 56
13.1 Definitions of terms used 56
13.2 Absolute maximum rating system 56
13.3 Design maximum rating system 56
13.4 Design centre rating system 56

14 LETTER SYMBOLS 57

1 POWERMOS TECHNICAL DATA

1.1 Device structure

Philips power MOSFET devices have a vertical double-implanted (DIMOS) channel structure (see Fig.1(a)). In an N-channel powerMOS transistor there is an N+substrate with a drain metallization below. Above the N+substrate is an N– epi layer, the width of which depends on the drain-source breakdown voltage and doping concentration. Next comes the gate made of N^+ polysilicon; it is embedded in an isolating silicon dioxide layer and serves as an implantation mask for the P region (barrier region) and the N^+ source region. The source metallization covers the entire structure and thus parallels the individual transistor cells on the chip.

The layout of a typical low voltage chip is shown in Fig.1(b).

The active part of the device consists of many cells connected in parallel to give a high current handling capability. Current flow is vertical through the chip.

Cell density is determined by photolithographic tolerance requirements and use of the optimised polysilicon track width, which varies as a function of device drain-source voltage rating.

Consequently, the low voltage devices have a cell density of 820,000 cells per square inch, compared to 500,000 cells per square inch for high voltage types. All the cells are covered by a continuous layer of aluminium which makes contact with each individual cell. The polysilicon gate is contacted by bonding to the defined pad area while the source wires are bonded directly to the aluminium over the cell array. The back of the chip is metallized with a triple layer of titanium/nickel/silver and this enables the drain connection to be formed using a standard alloy bond process. The cell array is surrounded by a field plate structure to control the electric field distribution in the device.

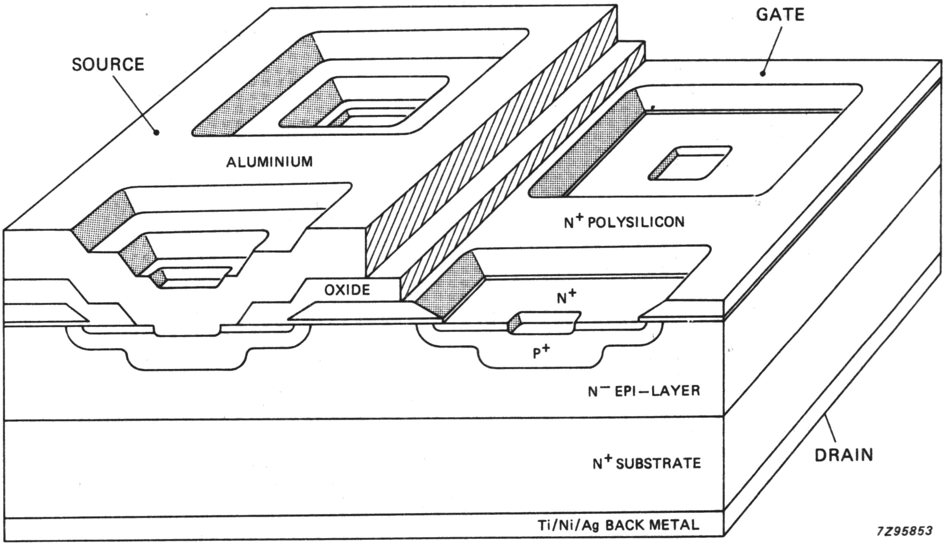


Fig.1(a) Power MOSFET channel structure.

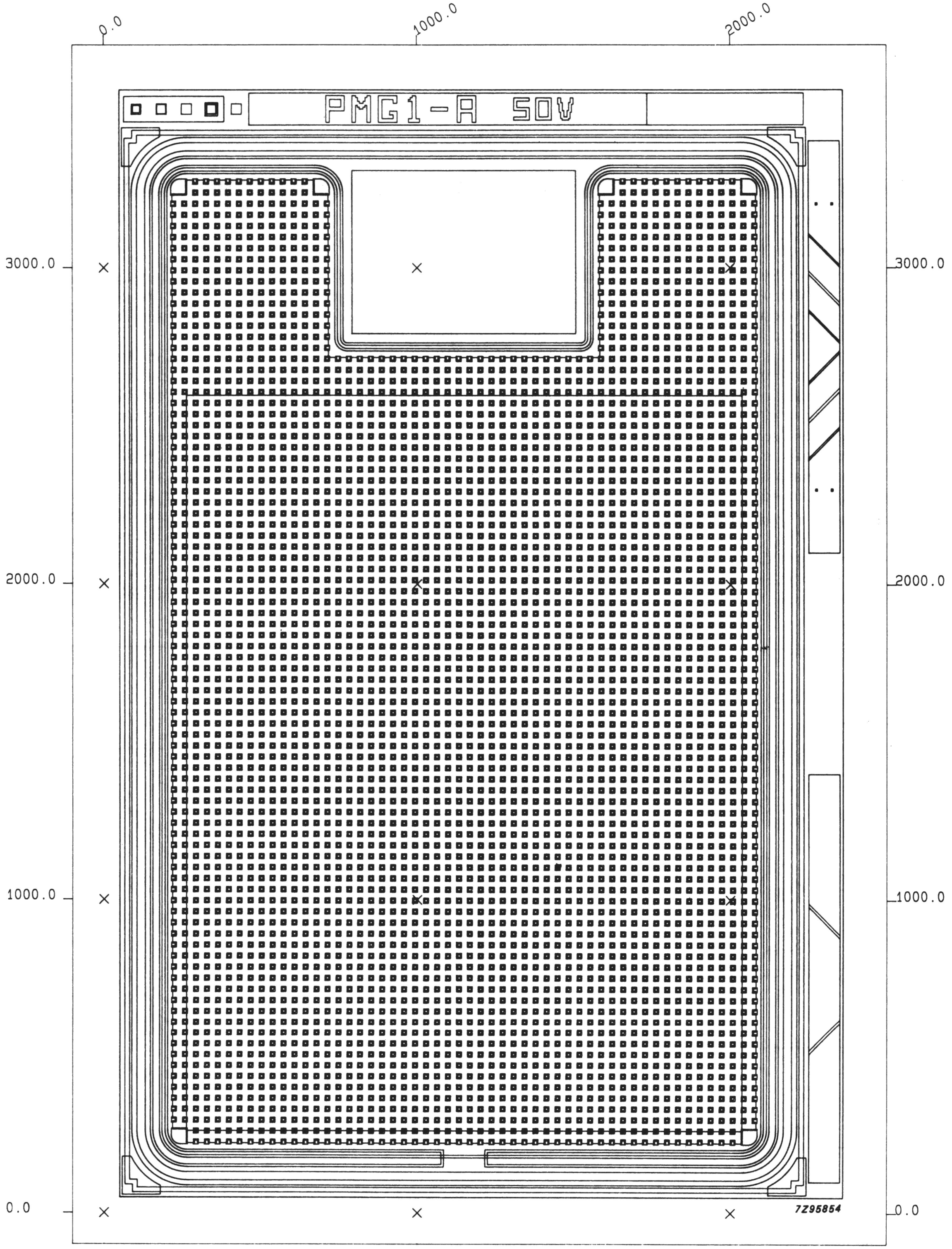

0.0
1000.0
2000.0
3000.0
2000.0
1000.0
0.0
3000.0
2000.0
1000.0
0.0
PMG1-A 50V
7Z95854

Fig.1(b) Layout of a typical low-voltage chip.

The cross-section through one cell in the array is shown in Fig.2. The channel length is approximately 1,5 microns and is defined by the difference in the sideways diffusion of the N+ source and the P− body. Both these diffusions are auto-aligned to the edge of the polysilicon gate during the fabrication process. All diffusions are formed by ion implantation followed by high temperature anneal/drive-in to give good parameter reproducibility. The gate is electrically isolated from the silicon by an 800 Angstrom layer of gate oxide and from the overlying aluminium by a thick layer of phosphorous doped oxide. Windows are defined in the latter oxide layer to enable the aluminium layer to contact the N+ source and the P+ diffusion in the centre of each cell. The P+ diffusion provides a low resistance connection between the P− body and ground potential, thus inhibiting turn-on of the inherent parasitic bipolar structure. Devices are fabricated on N/N+ epitaxial material, the thickness and doping concentration in the N layer being optimised to suit the breakdown voltage requirement.

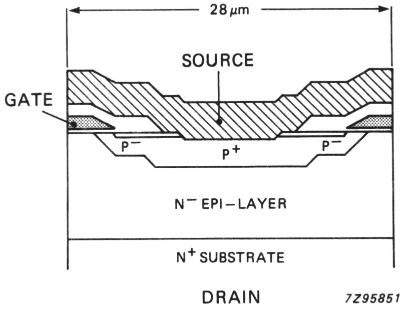


Fig.2 Cross-section of a single cell.

1.2 Device operation

Current flow in an enhancement mode power MOSFET is controlled by the voltage applied between the gate and source terminals. With both the gate and source at zero volts there is no source-drain current flow and the drain sits at the positive supply voltage. In the P− body region directly under the gate, holes are attracted to the surface. This enhances the concentration of positive charges and the silicon is in an 'accumulated' state. The P− body isolates the source and drain regions and forms two p-n junctions connected back-to-back. The only current which can flow from source to drain is the reverse leakage current.

As the gate voltage is gradually made more positive with respect to the source, holes are repelled and a depleted region of silicon is formed in the P− body below the silicon-gate oxide interface. The silicon is now in a 'depleted' state, but there is still no significant current flow between the source and drain.

When the gate voltage is further increased a very thin layer of electrons is formed at the interface between the P− body and the gate oxide, thus providing a conductive, N− channel path between the source and the drain. The silicon in the P− body is now in an 'inverted' state. A slight increase in gate voltage will result in a very significant increase in drain current and a corresponding rapid decrease in drain voltage, assuming a normal resistive load is present.

Eventually the drain current will be limited by the combined resistances of the load resistor and $R_{DS(ON)}$ of the MOSFET. The MOSFET will be effectively bottomed when $V_{gs} = +10$ volts. Subsequently reducing the gate voltage to zero volts reverses the above sequence of events. There are no stored charge effects since power MOSFETS are majority carrier devices.

1.3 Threshold voltage

The threshold voltage is normally measured by connecting the gate to the drain and then determining the voltage which must be applied across the device to achieve a drain current of 1,0 mA. This method is simple to implement and provides a ready indication of the point at which 'inversion' occurs in the device.

The P− body is formed by the implantation of boron through the tapered edge of the polysilicon followed by an anneal and drive-in. The peak boron concentration is located next to the edge of the source diffusion and this determines the actual threshold voltage. Process factors such as gate oxide thickness and doping concentration in the channel have a strong influence on the actual value of the threshold voltage. Consequently a window from 2,1 to 4,0 volts is defined in order to allow for spreads in these parameters and the other second other effects.

Positive charges in the gate oxide, for example due to sodium, can cause the threshold voltage to drift. However, this effect can be minimised by ensuring that the gate oxide is grown under ultra clean conditions. The polysilicon gate and phosphorus doped oxide layer subsequently provide a good barrier to mobile ions such as sodium and thus help to ensure good threshold voltage stability.

1.4 Drain-source on-state resistance

The overall drain-source resistance, $R_{DS(ON)}$, of a power MOSFET is composed of several elements, as shown in Fig.3.

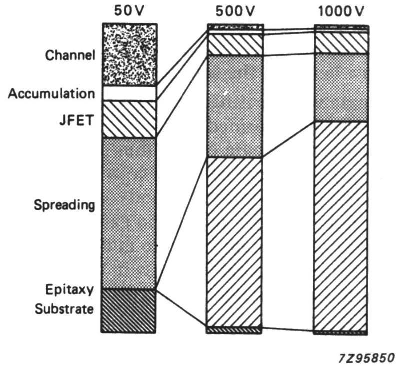


Fig.3 Power MOSFET components of $R_{DS(ON)}$.

The relative contribution from each of the elements varies with the drain-source voltage rating. For low voltage devices the channel resistance is very important while for the high voltage devices the resistivity and thickness of the epitaxial layer dominates. The properties of the various resistive components will now be discussed:

1.4.1 Channel

The unit channel resistance is determined by the channel length, gate oxide thickness, carrier mobility, threshold voltage, and the actual gate voltage applied to the device. The channel resistance can be significantly reduced by lowering the thickness of the gate oxide. The approach is used to fabricate the Logic Level MOSFET transistors and enables a similar value $R_{DS(ON)}$ to be achieved with only 5 volts applied to the gate. Of course, the gate-source voltage rating must be reduced to allow for the lower dielectric breakdown of the thinner oxide layer.

The overall channel resistance of a device is inversely proportional to channel width, determined by the total periphery of the cell windows. Channel width is over 100 cm for a 20 mm² low voltage chip. The overall channel resistance can be significantly reduced by going to higher cell densities, since the cell periphery per unit area is reduced.

1.4.2 Accumulation layer

The silicon interface under the centre of the gate track is 'accumulated' when the gate is biased above the threshold voltage. This provides a low resistance path for the electrons when they leave the channel, prior to entering the bulk silicon. This effect makes a significant contribution towards reducing the overall $R_{DS(ON)}$.

1.4.3 Parasitic JFET

After leaving the accumulation layer the electrons flow vertically down between the cells into the bulk of the silicon. Associated with each p-n junction there is a depletion region which, in the case of the high voltage devices, extends several microns into the N epitaxial region, even under zero bias conditions. Consequently the current path for the electrons is restricted by this parasitic JFET structure. The resistance of the JFET structure can be reduced by increasing the polysilicon track width. However this reduces the cell density. The need for compromise leads to an optimum value for the polysilicon track width for a given drain-source voltage rating. Since the zero-bias depletion width is greater for low doped material, then a wider polysilicon track width is used for high voltage chip designs.

1.4.4 Spreading resistance

As the electrons move further into the bulk of the silicon they are able to spread sideways and flow under the cells. Eventually paths overlap under the centre of each cell.

1.4.5 Epitaxial layer

The drain-source voltage rating requirements determine the resistivity and thickness of the epitaxial layer. For high voltage devices the resistance of the epitaxial layer dominates the overall value of $R_{DS(ON)}$.

1.4.6 Substrate

The resistance of the N+ substrate is only significant in the case of 50 V devices.

1.4.7 Wires and leads

In a completed device the wire and lead resistances contribute a few milli-ohms to the overall resistance.

1.5 Drain-source breakdown voltage

The drain-source resistance is approximately proportional to $(\hat{B}V_{dss})$ 2,5. It is important to achieve a high percentage of plane breakdown both for the cell region of the device and the edge termination structure, since this allows thinner, lower resistivity material to be used. This offers important advantages, particularly in the case of high voltage devices, in terms of reducing $R_{DS(ON)}$ per unit area. Computer models are used to investigate the influence of cell design and layout on breakdown voltage. These factors also influence the 'on-state' and switching performances and therefore a degree of compromise is necessary. Thus a high cell density may not be desirable for high voltage devices if it results in a significant reduction in the percentage of plane breakdown which might otherwise be achieved.

For the low voltage devices a field plate structure, Fig.4, is used to enhance the breakdown voltage. The plates reduce the electric field intensity at the corner of the P+ guard ring, and spread the field laterally along the surface of the device. A higher drain voltage can therefore be applied before the avalanche commences. The polysilicon gate is extended to form the first field plate, whilst the aluminium metallization forms the second plate. The polysilicon termination plate is shorted to the drain and operates as a channel stopper. The aluminium plate overlaps the termination ring and thus provides a complete electrostatic screen against any external ionic charges which might be present in the external environment.

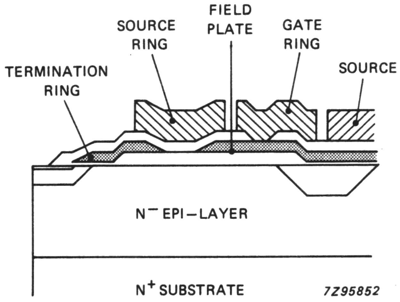


Fig.4 Field plate structure for low voltage devices.

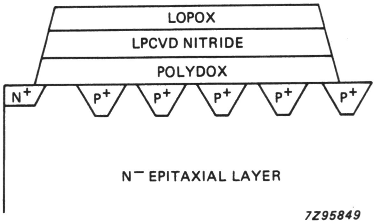


Fig.5 Ring structure for high voltage devices.

For high voltage devices a set of floating P+ rings, see Fig.5, is used to control the electric field distribution around the device periphery. The number of rings in the structure depends on the voltage rating of the device, nine rings are used for a 1000 volt type such as the BUZ50A. A three dimensional computer model enables the optimum ring spacing to be determined so that each ring experiences a similar field intensity as the structure approaches avalanche breakdown. The rings are passivated with polydox which acts as an electrostatic screen and prevents external ionic charges inverting the lightly doped N– interface to form P– channels between the rings. The polydox is passivated with layers of silicon nitride and phosphorus doped oxide.

2 INTRODUCTION TO POWER MOSFETs

2.1 What is a MOSFET?

There are two main types of Field Effect Transistor (FET) called the junction FET (JFET) and the Metal Oxide Semiconductor FET (MOSFET). In a FET the conductivity of a channel is varied by applying voltage to a control or gate terminal (G). There are two other terminals in most FETs which are connected internally to a channel. These are the source (S) and drain (D) terminals. In an N channel FET the channel is made of N type material and the drain is normally positive with respect to the source. In a P channel FET the drain is normally negative with respect to the source. The gate terminal is taken to a potential nearer that of the drain to reduce the resistance of the channel. An enhancement mode FET is turned off when the gate and source are at the same potential and depletion mode FET is turned on when the gate and source terminals are at the same potential.
A schematic representation of the JFET is shown in Fig.6.

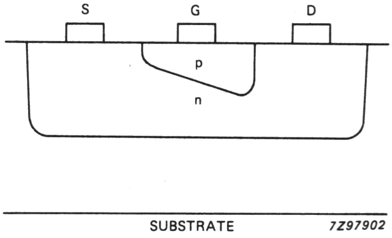


Fig.6 Structure of the Junction Field Effect Transistor (JFET).

To modulate the resistance between the drain and source terminals the voltage at the gate terminal is varied which varies the width of the depletion layer which exists mainly between gate and drain terminals. All JFETs are depletion mode devices because if the gate to source junction is forward biased excessive current will flow.

Depletion mode devices require two power supplies and so are more difficult to use than enhancement mode devices where the power supply for the gate drive circuit can easily be derived from the drain source supply. The MOSFET has a layer of insulating material between the gate and the channel. Electric field lines originating from charge on the gate cross the insulating layer and vary the channel carrier concentration and so the channel resistance. This is called inversion of the channel.

2.2 The structure of present day power MOSFETs

Present day Power MOSFETs are vertical double Diffused MOSFETs (DMOS). A schematic representation of the MOSFET structure is shown in Fig.7.

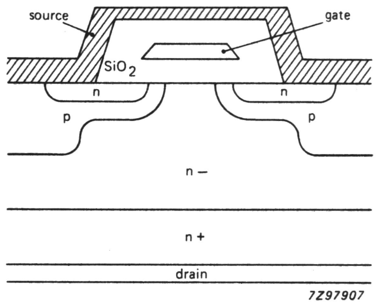


Fig. 7 Structure of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET).

The idea of a vertical channel MOSFET has been known since the 1930s but it was not until the mid 1970s that the technology of diffusion, ion implantation and material treatment had reached the level necessary to produce DMOS on a commercial scale. The vertical diffusion technique uses technology more commonly associated with the manufacture of large scale integrated circuits than traditional power device fabrication.

The first diffusion is that of the P type body region in an N channel device. Next an N type diffusion is done. The channel length can be controlled repeatedly to 1 or 2 μm with ion implantation.

Initially gate electrodes were made of metal but now they are mostly polycrystalline silicon. This means that interconnections between cells can be diffused rather than having to be made by metallization and bonding so manufacturing is made easier. A low on-resistance is achieved since many cells are paralleled on the same slice. It can be seen from Fig.7 that there is a parasitic n-p-n transistor inherent in the structure between the source and the drain. The emitter and base are shorted by source metallization and so this parasitic element manifests itself in device operation as a parasitic diode in parallel with the MOSFET channel.

P channel power MOSFETs are not as attractive for power switching since their on-resistance is higher than N channel MOSFETs of similar structure. This is because in silicon the hole mobility is much less than the electron mobility.

2.3 Advantages of power MOSFETs

Power MOSFETs offer the designer the following advantages:

- fast switching times.
- ease of paralleling.
- low drive power requirements.

2.4 Applications of power MOSFETs

Power MOSFETs are ideally suited for use in many applications, some of which are listed below.

- Switched mode power supplies (SMPS).
- Variable speed motor control.
- Power supplies for electronic data processing and telecommunications equipment.
- Uninterruptible power supplies (UPS).
- Automotive switching applications.
- Inverters.
- High frequency induction heating power supplies.
- Arc welding power supplies.
- Ultrasonic generators.

2.5 The characteristics of power MOSFETs

2.5.1 The dc characteristic

If a dc voltage source is connected across the drain and source terminals of an N channel enhancement mode MOSFET, with the positive terminal connected to the drain, and the voltage between the gate and source terminals is varied, the following changes in drain current will occur. As the gate-to-source voltage is increased from zero so that the potential of the gate becomes nearer that of the drain, there will be only negligible drain current until a voltage called the threshold voltage (V_T) is reached.

If the gate-to-source voltage is now set to a value greater than the threshold voltage and the drain-to-source voltage is increased from zero, the following changes in drain current will be observed. Any increases in drain-to-source voltage will be accompanied by increases in drain current until a value of drain-to-source voltage called the pinch-off voltage is reached.

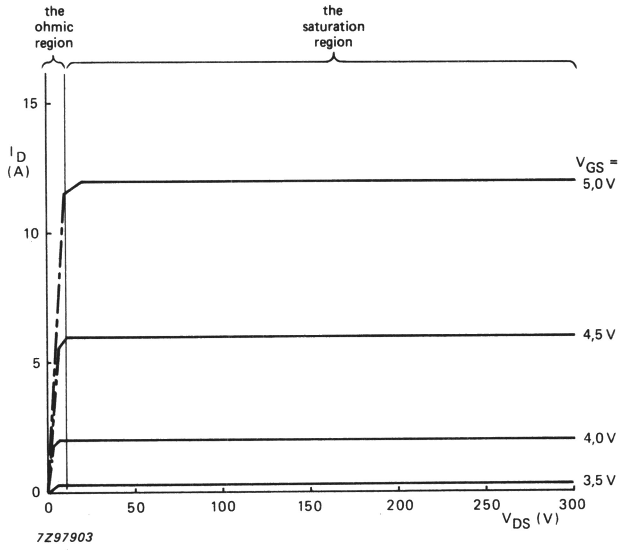


Fig.8 The typical dc characteristic of an n channel enhancement mode MOSFET.

Increasing the drain-to-source voltage above the pinch-off voltage will only cause a small change in drain current. These two regions of operation are called the Ohmic Region and the Saturation Region. The two regions can be seen in a typical dc characteristic of an N channel enhancement mode MOSFET, shown in Fig.8.

2.5.2 The Safe Operating Area

The Safe Operating Area (SOA) for the BUZ71A is shown in Fig.9.

The peak pulse current is based on a current above which internal connections may be damaged. The maximum continuous current is limited by the joule heating increasing the temperature of the silicon so that thermal degradation of the material occurs. This is an rms current limitation rather than the average current limitation which is the case for minority carrier devices such as bipolar transistors and thyristors. For pulses with small duty cycles the permissible pulse amplitude is increased. If the maximum voltage rating of the MOSFET is exceeded avalanche break-down may occur.

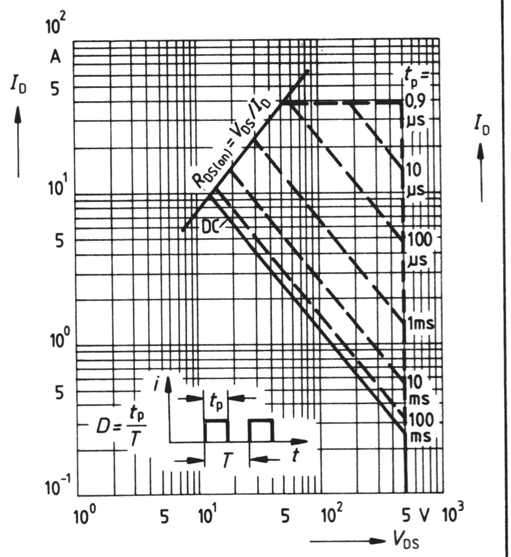


Fig.9 The Safe Operating Area of the BUZ71A.

The SOA graph shown in Fig.9 is useful in illustrating the way in which maximum values of current and voltage and duty cycle of operation constrain device operation. This graph is only valid for a case temperature of 25 °C and a junction temperature of 150 °C. In a real application the case temperature will be greater then 25 °C because of the finite thermal impedance of practical heatsinks. Also a junction temperature of between 80 °C and 125 °C would be preferable since this improves reliability. If a junction temperature of 80 °C instead of 150 °C is used then the ability of the MOSFET to withstand current spikes is improved. To calculate the maximum rms current permissible with a junction temperature of 80 °C the power losses in the device at various levels of current need to be found. This knowledge is combined with information on the thermal impedances of case to heatsink and heatsink to ambient as well as the ambient temperature in order to find the operating current levels.

2.5.3 The switching characteristics

There are various capacitances inherent in the structure of the MOSFET which are shown in Fig.10.

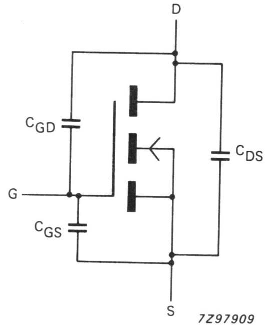


Fig.10 The internal capacitances of a Power MOSFET.

To turn the device on and off the gate-to-source capacitance has to be charged and discharged. The switching times of Power MOSFETs can be very fast. MOSFETs do not suffer from a storage time while minority carriers are removed since they are majority carrier devices. The impedance of the drive circuit influences the switching times. A lower drive source impedance produces a faster switching time. Temperature has only a small effect on device capacitances therefore switching times are independent of temperature.

In Fig.11 typical gate-source and drain-source voltages for a MOSFET switching current through a resistive load are shown. The gate source capacitance needs to be charged up to a threshold voltage (V_T) of about 3 V before the MOSFET begins to turn on. The time constant for this is $C_{GS}(R_{DR} + R_G)$ and the time taken is called the turn-on delay time ($t_{D(on)}$). When V_{GS} has reached the threshold voltage the MOSFET starts to turn on and V_{DS} begins to fall. C_{GD} now needs to be discharged as well as C_{GS} being charged so the time constant is increased and the gradient of V_{GS} is reduced. As V_{DS} becomes less than V_{GS} the value of C_{GD} increases greatly since it is depletion dependent. Therefore a plateau occurs in the V_{GS} characteristic. The time taken for I_D to rise from 10% to 90% of its on state value is called the rise time (t_r).

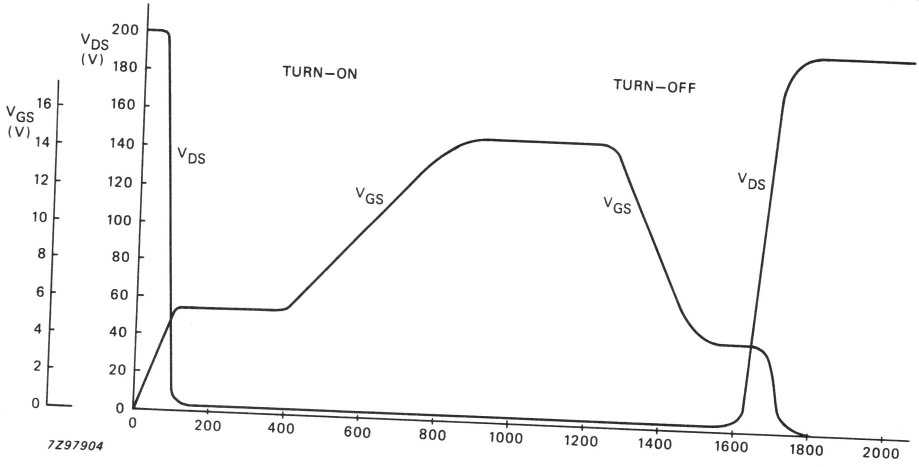


Fig.11 The switching waveforms for a MOSFET.

When V_{DS} has collapsed V_{GS} continues to rise as overdrive is applied. Gate overdrive provides benefits of reduced on-resistance and reduced risk of spurious turn-on. It also has the disadvantages of increasing the turn-off delay time ($t_{D(off)}$ and the gate drive circuit power dissipation.

To turn the MOSFET off the overdrive has first to be removed. The charging path for C_{GD} and C_{DS} now contains the load resistor (R_L) and so the turn-off time will be generally longer than the turn-on time.

2.6 The parallel operation of power MOSFETs

If power requirements exceed those of available devices then increased power levels can be achieved by paralleling devices. Paralleling of devices is made easier using MOSFETs because they have a positive temperature coefficient of resistance. If one paralleled MOSFET carries more current than the others it becomes hotter than them. This causes the on-resistance of that particular device to become greater than that of the others and so the current in it reduces. This mechanism opposes thermal runaway in one of the devices. The positive temperature coefficient also helps to prevent hot spots within the MOSFET.

2.7 The losses in power MOSFETs

There are four main causes of power dissipation in MOSFETs.

- Conduction losses – The conduction losses (P_C) are given by equation (1).

  $$P_C = I_D{}^2 R_{DS(ON)} \qquad (1)$$

  The on-resistance of the MOSFET when it is operated in the Ohmic region is dependent on the junction temperature.
- Switching losses – When a MOSFET is turned on or off it carries a large current and sustains a large voltage at the same time. There is therefore a large power dissipation during the switching interval. Switching losses are negligible at low frequencies but are dominant at high frequencies. The crossover frequency depends on the circuit configuration. For reasons explained in the section on switching characteristics a MOSFET usually turns off more slowly than it turns on so the losses at turn-off will be larger than at turn-on. Switching losses are very dependent on circuit configuration since the turn-off time is affected by the load impedance.

  Snubber components can be connected across the MOSFET to reduce turn-off losses. Inductors can be connected in series with the MOSFET to limit the rate of rise of current at turn-on to reduce turn on losses. With resonant loads switching can take place at a zero crossing of voltage or current so switching losses are very much reduced.
- Diode losses – A good approximation to the dissipation in the diode inherent in the structure of the MOSFET is the product of the diode voltage drop which is typically less than 1,5 V and the average current carried by the diode. Diode conduction can be useful in such circuits as pulse width modulated circuits used for motor control, in some stepper motor drive circuits and in voltage fed circuits feeding a series resonant load.
- Gate losses – The losses in the gate are given in equation 2 where R_G is the internal gate resistance, R_{DR} is the external drive resistance, V_{GSD} is the gate drive voltage and C_{IP} is the input capacitance of the MOSFET.

  $$P_G = \frac{C_{IP} \cdot V^2{}_{GSD} \cdot f \cdot R_G}{(R_G + R_{DR})} \qquad (2)$$

  The input capacitance varies greatly with the gate drain voltage so the expression in equation 3 is more useful.

  $$P_G = \frac{q_g \cdot V_{GSD} \cdot f \cdot R_G}{(R_G + R_{DR})} \qquad (3)$$

  Where q_g is the peak gate charge.

2.8 Conclusions

It can be seen that the operation of the Power MOSFET is relatively easy to understand. The advantages of fast switching times, ease of paralleling and low drive power requirements make the device attractive for use in many applications.

3 POWER MOSFET DRIVE CIRCUITS

MOSFETs are being increasingly used in many switching applications because of their fast switching times and low drive power requirements. The fast switching times can easily be realised by driving MOSFETs with relatively simple drive circuits, which will be described in the following paragraphs.

3.1 The requirements of the drive circuit

The switching of a MOSFET involves the charging and discharging of the capacitance between the gate and source terminals. This capacitance is typically about 2 nF. A gate-source voltage of 6 V is usually sufficient to turn a MOSFET fully on. However further increases in gate-to-source voltage can further reduce the voltage across the MOSFET. Therefore for switching times of about 50 ns the drive circuit must sink and source peak currents of about 0,5 A. However it is only necessary to carry this current during the switching intervals.

In some circuits, such as the full bridge circuit, the gate terminals of MOSFETs in the circuit need to float relative to each other. The gate drive circuitry then needs to incorporate some isolation.

The gate drive power requirements are given in equation (1)

$$P_G = Q_G \cdot V_{GS} \cdot f \qquad (1)$$

where Q_G is the peak gate charge, V_{GS} is the peak gate source voltage and f is the switching frequency.

The impedance of the gate drive circuit should not be so large that there is a possibility of dV/dt turn on. dV/dt turn on can be caused by rapid changes of drain to source voltage. The charging current for the gate drain capacitance flows through the gate drive circuit. This charging current can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on.

3.2 Non-isolated drive circuits

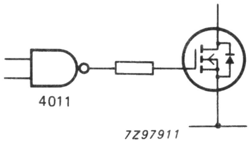


Fig.12 A very simple drive circuit utilizing a standard CMOS IC.

Faster switching speeds can be achieved by paralleling CMOS hex inverting (4049) or non-inverting (4050) buffers as shown in Fig.13.

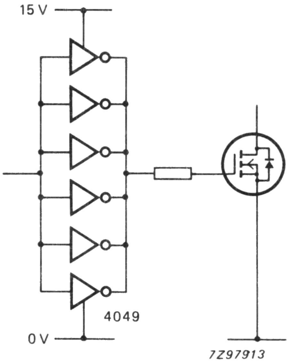


Fig.13 Driving Philips Powermos with 6 paralleled buffered inverters.

A push pull circuit can also be used as shown in Fig.14.

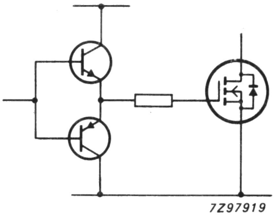


Fig.14 A drive circuit using a two transistor push pull circuit.

The connections between the drive circuit and the MOSFET should be kept as short as possible and twisted together if the shortest switching times are required. If both the drive circuit and the terminals of the MOSFET are on the same PCB then the inductance of tracks between the drive transistors and the terminals of the MOSFETs should be kept as small as possible. This is necessary to reduce the impedance of the drive circuit in order to reduce the switching times and the susceptibility of the circuit to dV/dt turn on of the MOSFET. Attention to layout also improves the immunity to spurious switching by interference.

One of the advantages of MOSFETs is that their switching times can easily be controlled. For example it may be required to limit the rate of change of drain current to reduce overshoot on the drain source voltage waveform. The overshoot may be caused by switching current in parasitic lead inductance and transformer leakage inductance. The slower turn on can be achieved by increasing the value of the gate drive resistor.

The supply rails should be decoupled near to fast switching elements such as the push-pull transistors in Fig.14. An electrolytic capacitor in parallel with a ceramic capacitor are recommended since the electrolytic capacitor will not be a low impedance to the fast edges of the MOSFET drive pulse.

3.3 Isolated drive circuits

Some circuits demand that the gate and source terminals of MOSFETs are floating with respect to those of other MOSFETs in the circuit. Isolated drive to these MOSFETs can be provided in the following way:

(a) Opto-isolators.

A drive circuit using an opto-isolator is shown in Fig.15.

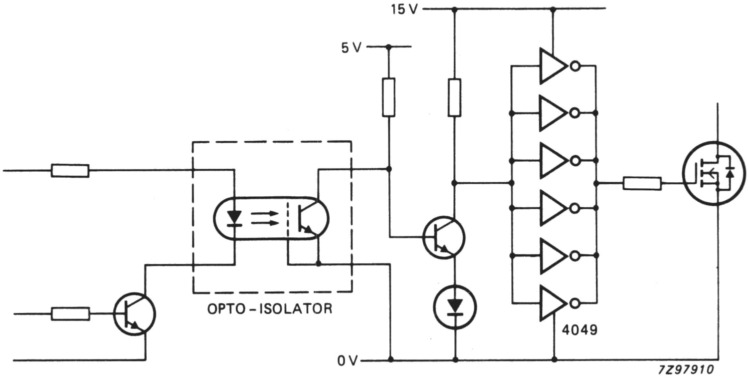


Fig.15 An isolated drive circuit using an opto-isolator.

A diode in the primary side of the opto-isolator emits photons when it is forward biased. These photons impinge on the base region of a transistor in the secondary side. This causes photogeneration of carriers sufficient to satisfy the base requirement for turn-on. In this way the opto-isolator provides isolation between the primary and secondary of the opto-isolator. An isolated supply is required for the circuitry on the secondary side of the opto isolator. This supply is required for the circuitry on the secondary of the opto-isolator. This supply can be derived from the drain-to-source voltage across the MOSFET being driven in some cases by a circuit shown in Fig.16.

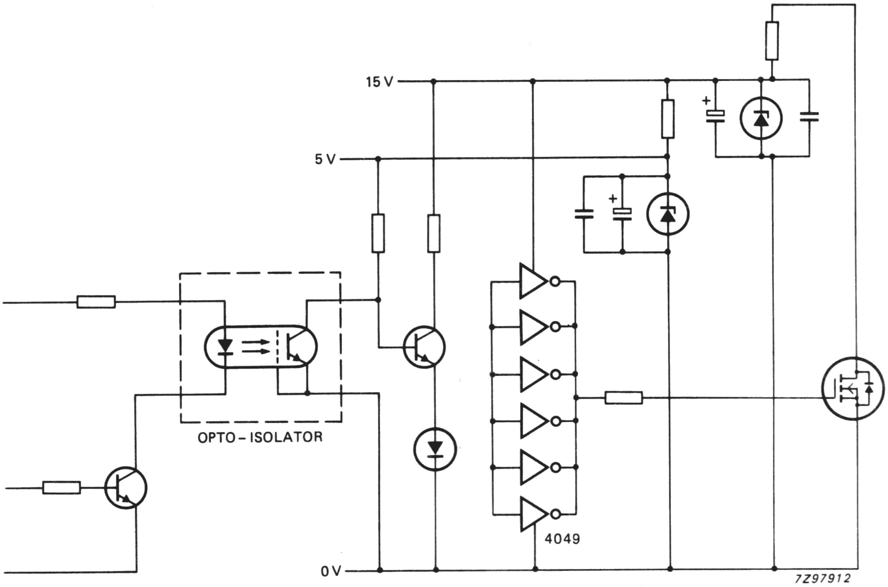


***Fig.16** An opto-isolated drive circuit with the isolated power supply for the secondary derived from the drain source voltage of the MOSFET.*

This is made possible by the low drive power requirements of MOSFETs. Some opto-isolators incorporate an internal screen to improve the common mode transient immunity. Values as high as 1000 V/µs are quoted for common mode rejection which is equivalent to rejecting a 300 V peak-to-peak sinewave.

The faster opto-isolators work off a maximum collector voltage on the secondary side of 5 V so some form of level shifting is required on the secondary side.

(b) Pulse transformers.

A circuit using a pulse transformer for isolation is shown in Fig.17(a).

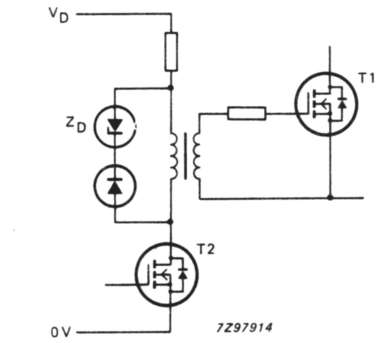


Fig.17(a) Circuit using a pulse transformer for isolation.

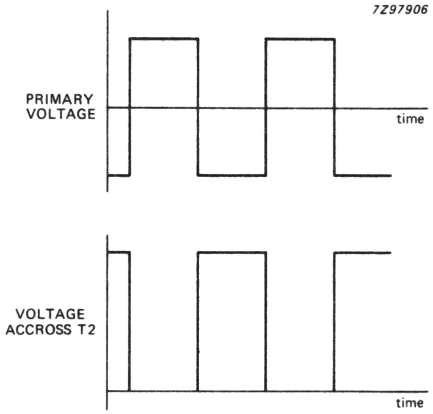


Fig.17(b) Waveforms associated with pulse transformer.

When T2 switches on voltage is applied across the primary of the pulse transformer. The current through T2 consists of the sum of the gate drive current for T1 and the magnetising current of the pulse transformer. From the waveforms of current and voltage around the circuit shown in Fig.17(b) it can be seen that after the turn off of T2 the voltage across it rises to $V_D + V_Z$, where V_Z is the voltage across the zener diode Z_D. The zener voltage V_Z applied across the pulse transformer causes the flux in the core to be reset. Thus the net volt second area across the pulse transformer is zero over a switching cycle. The minimum number of turns on the primary is given by equation (2).

$$N = \frac{Vt}{\hat{B}A_e} \qquad (2)$$

where B is the maximum flux density, A_e is the effective cross sectional area of the core and t is the time that T2 is on for.

The circuit in Fig.17(a) is best suited for fixed duty cycle operation. The zener diode has to be large enough so that the flux in the core will be reset during operation with the maximum duty cycle. For any duty cycle less than the maximum there will be a period when the voltage across the secondary is zero as shown in Fig.18.

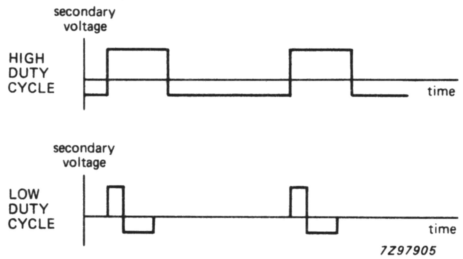


Fig.18 The voltage waveforms associated with the circuit in Fig.17(a) with varying duty cycles.

In Fig.19 a capacitor is used to block the dc component of the drive signal.

Drive circuits using pulse transformers have problems if a widely varying duty cycle is required. This causes widely varying gate drive voltages when the MOSFET is off. In consequence there are variable switching times, varying levels of immunity to dV/dt turn on and immunity to interference. This can be overcome by using the circuit shown in Fig.20.

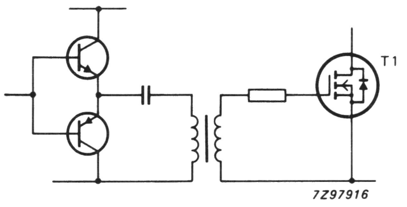


Fig.19 A drive circuit using a capacitor to block the dc component of the drive waveforms.

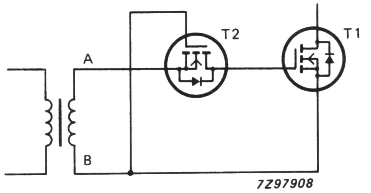


Fig.20 A drive circuit that uses a pulse transformer for isolation which copes well with widely varying duty cycles.

In the circuit shown in Fig.20 when A is positive with respect to B the input capacitance of T1 is charged through the parasitic diode of T2. The voltage across the secondary of the pulse transformer can then fall to zero and the input capacitance of T1 will remain charged. When B becomes positive with respect to

A T2 will turn on and the input capacitance of T2 will be discharged. The noise immunity of the circuit can be increased by using another MOSFET as shown in Fig.21.

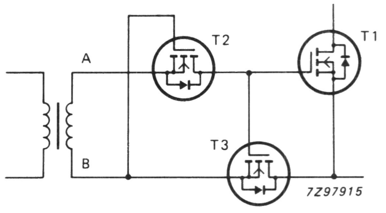


Fig.21 An isolated drive circuit with good performance with varying duty cycles and increased noise immunity.

In Fig.21 the potential at A relative to B has to be sufficient to charge the input capacitance of T3 and so turn T3 on before T1 can begin to turn on.

In Fig.22 the drive signal is ANDed with a hf clock. If the clock has a frequency much higher than the switching frequency of T1 then the size of the pulse transformer is reduced. The hf signal on the secondary of the pulse transformer is rectified. Q1 provides a low impedance path for discharging the input capacitance of T1 when the hf signal on the secondary of the pulse transformer is absent.

One of the components of the impedance of the gate circuit is the leakage inductance of the pulse transformer. The leakage inductance has two main detrimental effects. Firstly it restricts the rate of rise of gate source voltage and so the switching time of the MOSFET. Also the risk of dV/dt turn on is increased since the impedance of the gate drive is increased. To overcome these problems circuits such as those in Fig.23 can be used.

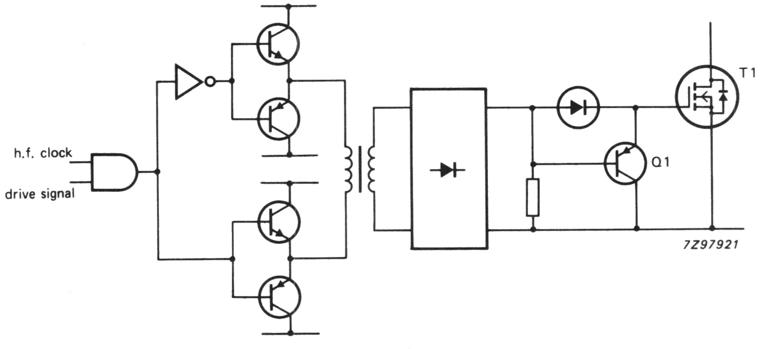


Fig.22 A drive circuit that reduces the size of the pulse transformer.

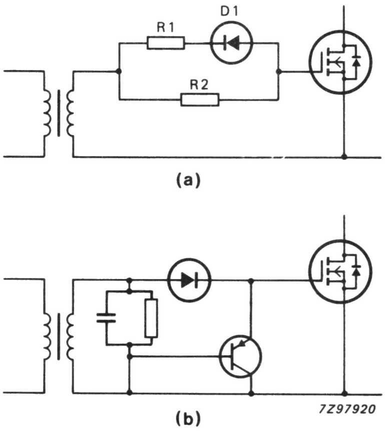


Fig.23 Two circuits that reduce the risk of dV/dt turn on.

The diode in Fig.23(a) reduces the gate drive impedance when the MOSFET is turned off. In Fig.23(b) the drive pulse is taken away the pnp transistor is turned on. When the pnp transistor is on it short-circuits the leakage inductance of the pulse transformer and so reduces the gate drive impedance.

3.4 Parallel operation

Power MOSFETs lend themselves readily to operation in parallel since their positive temperature coefficient of resistance opposes thermal runaway. Since MOSFETs have low gate drive power requirements it is not normally necessary to increase the rating of drive circuit components if more MOSFETs are connected in parallel. It is however recommended that differential resistors are used in the drive circuits as shown in Fig.24.

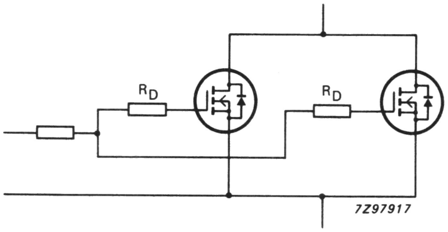


Fig.24 A drive circuit suitable for successful paralleling of Philips MOSFETs incorporating differential resistors.

These differential resistors (R_D) damp down possible oscillations between reactive components in the device and in connections around the MOSFETs with the MOSFETs themselves, which have a high gain even up to 200 MHz.

3.5 Protection against gate-source overvoltages

It is recommended that zener diodes are connected across the gate-source terminals of the MOSFET to protect against voltage spikes. One zener diode or two back-to-back zener diodes are necessary dependent on whether the gate-source drive is unipolar or bipolar, as shown in Fig.25.

The zener diodes should be connected close to the terminals of the MOSFET to reduce the inductance of the connecting leads. If the inductance of the connecting leads is too large it can support sufficient voltage to cause an overvoltage across the gate-source oxide.

In conclusion the low drive power requirement of Philips PowerMOS make provision of gate drive circuitry a relatively straightforward process as long as the few guidelines outlined in this note are heeded.

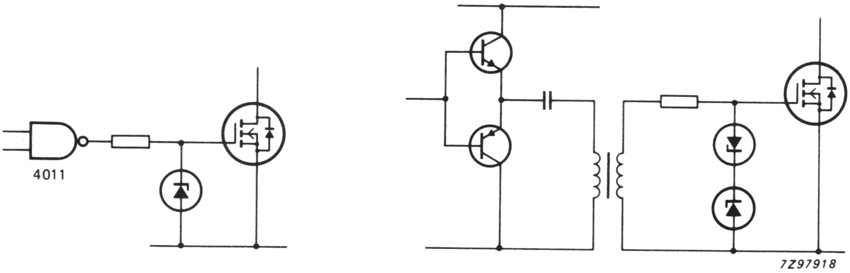


Fig.25 Zener diodes used to suppress voltage spikes across the gate-source terminals of the MOSFET.

4 THE SERIES OF OPERATION OF POWER MOSFETs

The need for high voltage switches can be well illustrated by considering the following examples. In flyback converters the leakage inductance of an isolating transformer can cause a large voltage spike across the switch when it switches off. If high voltage MOSFETs are used the snubber components can be reduced in size and in some cases dispensed with altogether. Industrial equipment normally requires supply voltages of 415 V, 550 V or 660 V to operate. Rectification of these supply voltages produces dc rails of approximately 550 V, 700 V and 800 V. The need for high voltage switches in these cases is clear.

Resonant topologies are being increasingly used in switching circuits. These circuits have advantages of reduced radio frequency interference (rfi) and reduced switching losses. To reduce the size of magnetic components and capacitors the switching frequency of power supplies is increased. Rfi and switching losses become more important at higher frequencies, so resonant topologies become more attractive. Resonant circuits have the disadvantage that the ratio of peak-to-average voltage can be large. For example a parallel resonant power supply for a microwave oven operating off a 240 V supply can be most easily designed using a switch with a voltage rating of over 1000 V.

In high frequency induction heating power supplies, capacitors are used to resonate the heating coil. The use of high voltage switches in the inversion bridge can result in better utilisation of the kVAR capability of these capacitors. This is advantageous since capacitors rated at tens of kVAR above 100 kHz are very expensive.

In most TV deflection and monitor circuits peak voltages of up to 1300 V have to be sustained by the switch during the flyback period. This high voltage is necessary to reset the current in the horizontal deflection coil. If the EHT flashes over, the switch will have to sustain a higher voltage, so 1500 V devices are typically required. The Philips range of PowerMOS includes devices rated at voltages up to 1000 V to cater for these requirements. Series operation can be attractive for the following reasons:

- If a voltage rating higher than 1000 V is needed. The ratio of peak-to-average current carrying capability of Philips PowerMOS is excellent and is typically about four. However the voltage rating of the MOSFET cannot be uprated to the same extent even for very short pulses.
- Series operation allows flexibility as regards on-resistance and so conduction losses.

There are problems that have to be overcome for successful operation of MOSFETs in series. If one device turns off before another it may have to block a voltage greater than its breakdown voltage. This will cause a reduction in the lifetime of the MOSFET. Also there is a requirement for twice as many isolated gate drive circuits in many circuits.

The low drive power requirements of Philips PowerMOS mean that the provision of more isolated gate drive circuits is made easier. Resonant circuits can have advantages in reducing the problems encountered if one MOSFET turns off before another. The current-fed full-bridge inverter is one such circuit and its operation is illustrated in Fig.26.

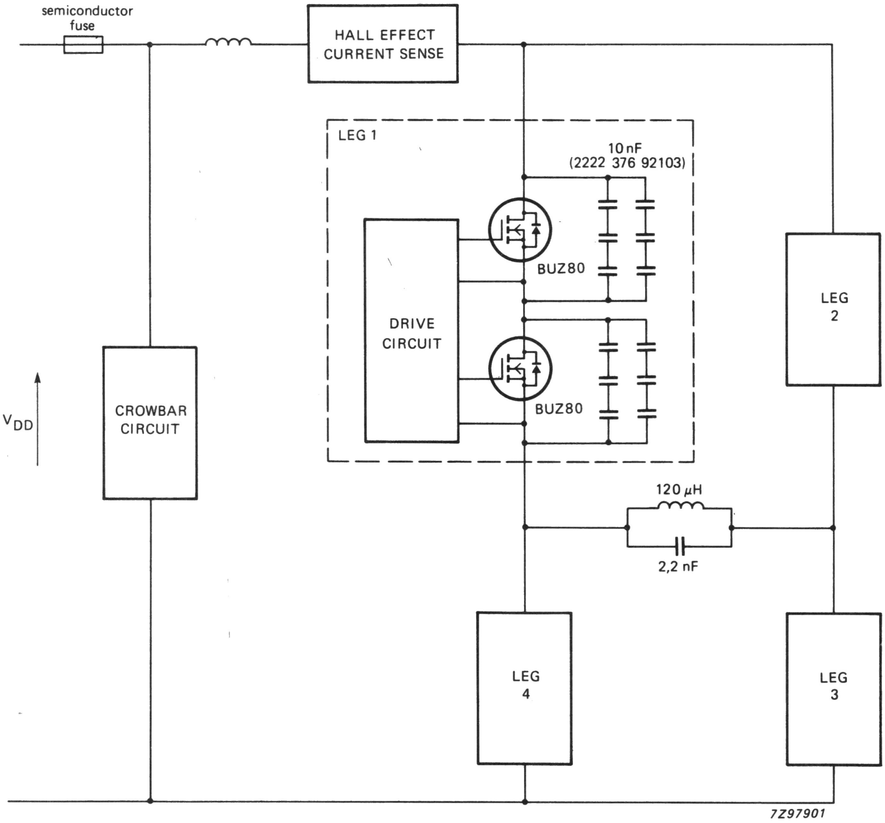


Fig.26 Circuit diagram of the full-bridge current-fed inverter feed a parallel resonant load.

4.1 The Current-fed Inverter

A circuit diagram of the full-bridge current-fed inverter is shown in Fig.26. A choke in the d.c. link smoothes the link current. Switching in the inversion bridge causes a rectangular wave of current to be passed through the load. The load is a parallel resonant tank circuit. Since the Q of the tank circuit is relatively high, the voltage across the load is a sinewave. MOSFETs sustain a half sinusoid of voltage when they are off. Thus series operation of MOSFETs is made easier because if one MOSFET turns off before another it only has to sustain a small voltage. The gate drive to MOSFETs connected in series should be made as similar as possible to achieve the best balance. In particular the zero crossings should be synchonised. The MOSFET drive circuit shown in Fig.27 has been found to be excellent in this respect. For current-fed resonant circuits in which the duty cycle varies over large ranges the circuit in Fig.28 will perform well. A short pulse applied to the primary of the pulse transformer is sufficient to turn MOSFET T4 on. This short pulse can be achieved by designing the pulse transformer so that it saturates during the time that T1 is on. The gate-source capacitance of T4 will remain charged until T2 is turned on. T3 will then be turned on and the gate-source capacitance of T4 will be discharged and so T4 will be turned off. This circuit then overcomes problems of resetting the flux in the core of the pulse transformer for large duty cycles.

A current-fed full-bridge inverter as shown in Fig.26 was constructed. Each leg of the inverter consisted of two MOSFETs, type BUZ80, connected in series. The ideal rating of the two switches in each leg was therefore 1600 V and 2,6 A. The inverter was fed into a parallel resonant circuit with values of L = 120 μH (Q = 24 at 150 kHz) and C = 2,2 nF.

Capacitors were connected across the drain-source terminals of MOSFETs. The value of the capacitor across the drain-to-source of each MOSFET was 6,6 nF. This was composed of six 10 nF polypropylene capacitors, type 2222 376 92103, as shown in Fig.26. This gave a peak voltage rating of about 850 V at 150 kHz for the capacitor combination across each MOSFET. (This voltage rating takes into account that the capacitors will only have to sustain voltage when the MOSFET is off). The function of these capacitors was twofold. Firstly they suppressed spikes caused by switching off current in parasitic lead inductance. Secondly they improved the sharing of voltage between the MOSFETs connected in series. These capacitors are effectively in parallel with the tank circuit capacitor. However only half of the capacitors across MOSFETs are in circuit at any one time. This is because half of the capacitors are shorted out by MOSFETs which have been turned on.

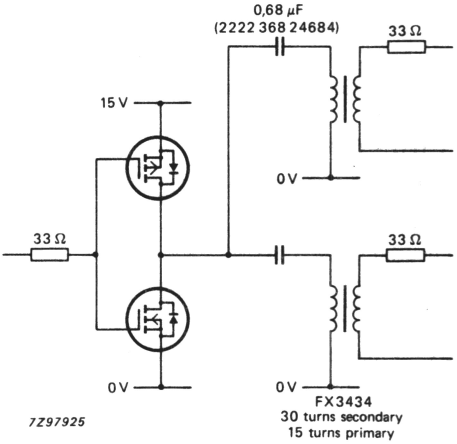

0,68 μF
(2222 368 24684)
33 Ω
15 V
0 V
33 Ω
33 Ω
0 V
0 V
FX3434
30 turns secondary
15 turns primary
7Z97925

Fig.27 The MOSFET drive circuit.

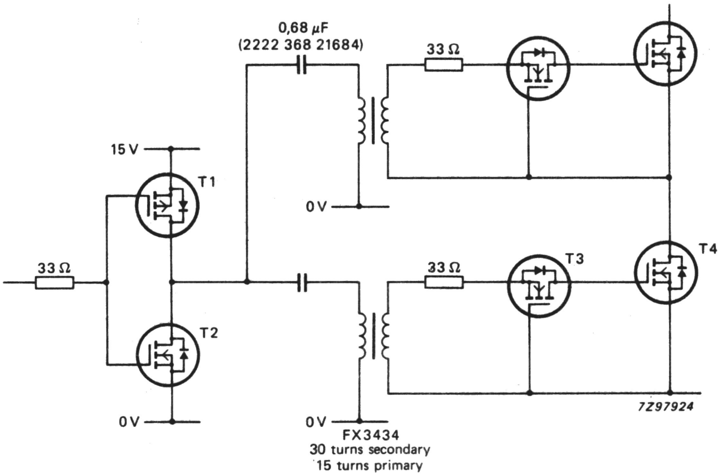

0,68 μF
(2222 368 21684)
33 Ω
15 V
T1
0 V
33 Ω
33 Ω
T3
T4
T2
0 V
0 V
FX3434
30 turns secondary
15 turns primary
7Z97924

Fig.28 Drive circuit with good performance over widely varying duty cycles.

The resonant frequency of the tank circuit and drain-source capacitors is given by Equation 1:

$$f = \frac{1}{2\pi\sqrt{LC_{TOT}}} \qquad (1)$$

where C_{TOT} is the equivalent capacitance of the tank circuit capacitor and the drain-source capacitors (see Equation 2).

$$C_{TOT} = C_T + C_{DS} \qquad (2)$$

Therefore the resonant frequency of the tank circuit was 155 kHz. An expression for the impedance at resonance of the parallel resonant circuit (Z_D) is given in Equation 3.

$$Z_D = \frac{L}{C_{TOT}R} \qquad (3)$$

The Q of the circuit is given by Equation 4.

$$Q = \frac{\omega \cdot L}{R} \qquad (4)$$

Substituting Equation 4 into Equation 3.

$$Z_D = \frac{Q}{\omega \cdot C_{TOT}} \qquad (5)$$

Thus Z_D for the parallel resonant load was 2,7 kΩ.

In a conventional rectangular switching circuit the connection of capacitors across MOSFETs will cause additional losses. These losses are caused when a MOSFET is turned on, allowing energy stored in the drain-source capacitance to dissipate in the MOSFET and in a series resistor. This series resistor is necessary to limit the current spike in the MOSFET at turn-on. These losses are appreciable at 150 kHz, e.g. the connection of 1 nF capacitor across a MOSFET switching 600 V would cause losses of more than 25 W at 150 kHz. In the current-fed inverter described in this chapter, the MOSFETs turn on when the voltage across the capacitor is ideally zero. The supply to the inverter was 470 V rms. This meant that the peak voltage in the dc link was 650 V.

Equating the power flowing in the dc link to the power dissipated in the tank circuit produces an expression for the peak voltage across the tank circuit (V_T) as given in Equation 6.

$$V_T = \frac{\sqrt{2}}{0{,}9} V_{DS} \qquad (6)$$

Therefore the peak-to-peak voltage across the tank circuit was ideally 2050 V. The voltage across each MOSFET should be 512 V.

The results:

The switching frequency was 120 kHz. Thus the load was fed slightly below its resonant frequency. This meant that the load looked inductive and ensured that the MOSFETs did not switch on when the capacitors connected across their drain-source terminals were charged.

The waveforms of the voltage across two MOSFETs in series in a leg of the inversion bridge are shown in Fig.29. It can be seen that the sharing is excellent. The peak voltage across each MOSFET is 600 V. This is higher than 512 V because of ringing between parasitic lead inductance and the drain-source capacitance of MOSFETs when they switch off.

The MOSFETs carry two components of current. The first component is the dc link current. The second component is a fraction of the circulating current of the tank circuit. The size of the second component is dependent on the relative sizes of the drain-source capacitance connected across MOSFETs and the tank circuit capacitor. The value of the second component is given by Equation 7.

$$\hat{I} = \hat{V}_T \cdot \omega \cdot C \qquad (7)$$

The peak value of charging current for drain-source capacitors which is carried by each MOSFET is therefore 4 A. The on-state resistance of the BUZ80 is about 5 Ω at 80 °C. This explains the rise in $V_{DS(ON)}$ of about 20 V seen in Fig.29 just before the turn-off of the MOSFETs.

The sharing of Philips PowerMOS in this configuration is so good that the value of drain-source capacitance is not determined by its beneficial effect on sharing. The minimum value of drain-source capacitance will be selected to reduce ringing. The value is dependent on power output and layout. The increased current levels associated with increased power output make the ringing worse. A higher power output usually involves a larger number of MOSFETs connected in parallel. Therefore a value of drain-source capacitance for each MOSFET can be specified independent of the power output of the supply. A value of between 5 and 10 nF is sufficient if sensible practice as regards layout is adopted e.g. twisting leads to reduce loop inductance.

Conclusions:

It has been shown that MOSFETs can be connected in series to realise a switch that is as high as 90% of the sum of the voltage sustaining capabilities of the individual transistors.

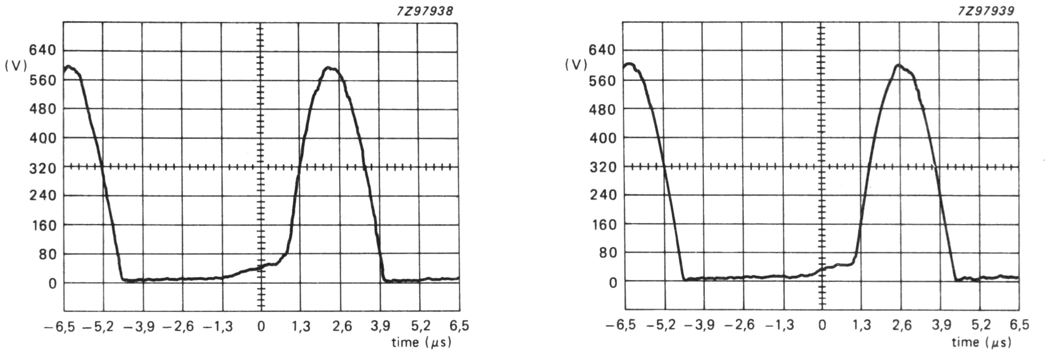


Fig.29 The drain-source voltage waveforms for two MOSFETs connected connected in series in a leg of the inversion bridge. (80 V/div. vert, 1,3 μs/div. hor).

5 THE PARALLEL OPERATION OF PHILIPS' POWER MOSFETs IN SWITCHING CIRCUITS

Power MOSFETs are being increasingly used in preference to other switches because of their excellent high-frequency performance, low drive power requirements, ease of paralleling and very good peak-to-average current carrying capability. The Philips' range of power MOSFETs has benefited from the company's extensive experience in the field of power semiconductors. This publication is a guide to the successful paralleling of Philips' power MOSFETs in switching circuits.

5.1 Advantages of parallel operation of devices

5.1.1 Increased power handling capability

If power requirements exceed those of available devices then increased power levels can be achieved by paralleling devices. The alternative means of meeting the power requirements would be to increase the area of the die. The processing of the larger die would have a lower yield and so the cost of the die would be increased. The larger die may also require a more expensive package.

5.1.2 Standardisation

Paralleling devices can mean that only one package, say the TO220 package, needs to be used. This can result in reduced production costs.

5.1.3 Increased operating frequency

Packages are commercially available which contain typically four die connected in parallel. The switching capabilities of these packages are typically greater than 10 KVA. The parasitic inductances of connections to the paralleled dies are different for each die. This means that the current rating of the package has to be derated at higher frequencies to allow for unequal current sharing. The voltage rating of the multiple die package has to be derated for higher switching speeds. This is because the relatively large inductances of connections within the package sustain appreciable voltages during the switching intervals. This means that the voltages at the drain connections to the dice will be appreciably greater than voltages at the terminals of the package. By paralleling devices these problems can be overcome.

Faster switching speeds are achieved using paralleled devices than using a multiple die package. This is because switching times are adversely affected by the impedance of the gate drive circuit. When devices are paralleled these impedances are paralleled and so their effect is reduced. Hence faster switching times and so reduced switching losses can be achieved.

Faster switching speeds improve paralleling. During switching intervals one MOSFET may carry more current than other MOSFETs in parallel with it. This is caused by differences in electrical parameters between the paralleled MOSFETs themselves or between their drive circuits. The increased power dissipation in the MOSFET which carries more current will be minimised if switching speeds are increased. The inevitable inductance in the source connection caused by leads within the package causes a negative feedback effect during switching. This negative feedback effect reduces the harmful effect of unequal impedances of drive circuit connections to paralleled MOSFETs. The faster the switching speeds then the greater will be the balancing effect of the negative feedback.

If the rate of rise of current in one paralleled MOSFET is greater than in the others, then the voltage drop across inductances in its drain and source terminals will be greater. This will oppose the build-up of current in this MOSFET and so have a balancing effect. This balancing effect will be greater if switching speeds are faster.

Paralleling devices enables higher operating frequencies to be achieved than using multiple die packages. The faster switching speeds made possible by paralleling at the device level promote better current sharing during switching intervals.

5.1.4 Increased power dissipation

If two devices, each rated for half the total required current are paralleled then the sum of their individual power dissipation capabilities will be more than the possible power dissipation in a single device rated for the total required current. This is especially useful for circuits operating above 100 kHz where switching losses predominate.

5.2 Advantages of Power MOSFETs for parallel operation

5.2.1 Reduced likelihood of thermal runaway

If one of the paralleled devices carries more current, then the power dissipation in this device will be greater and its junction temperature will increase. The temperature coefficient of $R_{DS(ON)}$ for power MOSFETs is positive as shown in Fig.30.

Therefore there will also be a rise in $R_{DS(ON)}$ for the device carrying more current. This mechanism will oppose thermal runaway in paralleled devices and also in paralleled cells in the device.

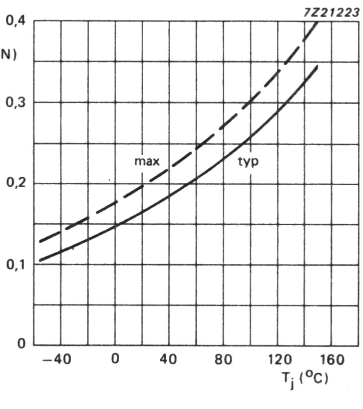


Fig.30 Typical graph of on-state resistance versus temperature for a power MOSFET.

5.2.2 Low drive power requirements

The low drive power requirements of power MOSFETs mean that many devices can be driven from the same gate drive that would be used for one MOSFET.

5.2.3 Very good tolerance of dynamic unbalance

The peak-to-average current carrying capability of power MOSFETs is very good. A device rated at 8 A continuous drain current can typically withstand a peak current of about 30 A. Therefore, for the case of three 8 A devices in parallel, if one of the devices switches on slightly before the others no damage will result since it will be able to carry the full load current for a short time.

5.3 Design points

5.3.1 Derating

Since there is a spread in on-resistance between devices from different batches it is necessary to derate the continuous current rating of paralleled devices by about 20%.

5.3.2 Layout

There are two aspects to successful paralleling; static and dynamic balance. Static balance refers to equal sharing of current between paralleled devices when they have been turned on. Dynamic balance means equal sharing of current between paralleled transistors during switching intervals. Asymmetrical layout of the gate drive circuitry causes dynamic unbalance. Connections between the gate drive circuitry and the MOSFETs need to be kept short and twisted together to reduce their inductance. Also, the connections between the gate drive circuit and paralleled MOSFETs need to be approximately the same length.

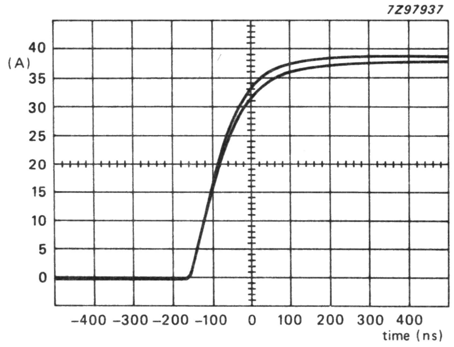


Fig.31 Waveforms of current through two paralleled BUZ71 MOSFETs with symmetrical layout; R_L = 3,9 Ω; V_{DD} = 25 V.

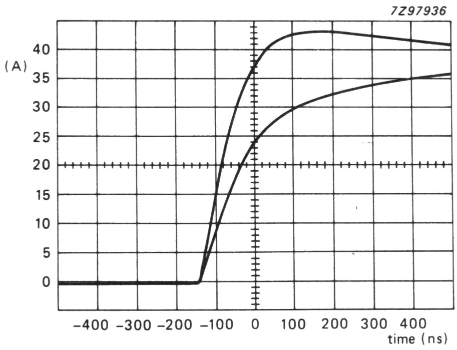


Fig.32 Waveforms of current through two paralleled BUZ71 MOSFETs with 40 nH connected in the source connection of one MOSFET; $R_L = 3{,}9\ \Omega$; $V_{DD} = 25$ V.

Figures 31 and 32 illustrate the effect of asymmetrical layout on the current sharing of two paralleled MOSFETs. The presence of 40 nH in the source connection of one of the two paralleled BUZ71 MOSFETs causes noticeable unbalance. A square-shaped loop of 1 mm diameter wire and side dimension of only 25 mm is sufficient to produce an inductance of 40 nH.

Symmetrical layout becomes more important if more MOSFETs are paralleled, e.g. a MOSFET with an $R_{DS(ON)}$ of 0,7 Ω connected in parallel with a MOSFET of 1 Ω $R_{DS(ON)}$, carries 25% more current than if both MOSFETs had an $R_{DS(ON)}$ of 1 Ω. If the MOSFET with an $R_{DS(ON)}$ of 0,7 Ω were connected in parallel with a hundred MOSFETs of 1 Ω $R_{DS(ON)}$, it would carry 40% more current than if all the MOSFETs had an $R_{DS(ON)}$ of 1 Ω.

5.3.3 Good thermal coupling

There should be good thermal coupling between paralleled MOSFETs. This is achieved by mounting paralleled MOSFETs on the same heatsink or on separate heatsinks which are in good thermal contact with each other.

If poor thermal coupling existed between paralleled MOSFETs and the positive temperature coefficient of resistance was relied on to promote static balance, then the total current carried by the MOSFETs would be less than with good thermal coupling. Some MOSFETs would also have relatively high junction temperatures and so their reliability would be reduced. The temperature coefficient of MOSFETs is not large enough to make poor thermal coupling tolerable.

5.3.4 The suppression of parasitic oscillations

MOSFETs have transition frequencies typically in excess of 200 MHz and parasitic reactances are present both in the MOSFET package and circuit connections so the necessary feedback conditions for parasitic oscillations exist. These oscillations typically occur at frequencies above 100 MHz, so a high bandwidth oscillscope is necessary to investigate them. The likelihood of these parasitic oscillations occuring is very much reduced if small differential resistors are connected in the leads to each paralleled MOSFET. A common gate-source drive resistor of between 10 and 100 Ω with differential resistors of about 10 Ω are recommended, as shown in Fig.33.

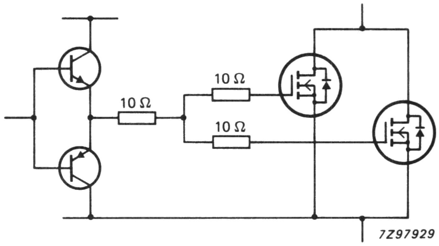


Fig.33 Differential gate drive resistors.

The suppression of parasitic oscillations between paralleled MOSFETs can also be aided by passing the connections from the gate drive circuit through ferrite beads. The effect of these beads below 1 MHz is negligible. The ferrite beads however damp the parasitic oscillations which occur at frequencies typically above 100 MHz. An example of parasitic oscillations is shown in Fig.34.

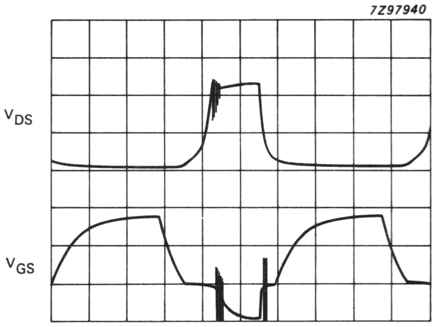


Fig.34 Parasitic oscillations on voltage waveforms of a MOSFET.

If separate drive circuits with closely decoupled power supplies are used for each paralleled device, then parasitic oscillations will be prevented. This condition could be satisfied by driving each paralleled MOSFET from 3 buffers in a CMOS Hex buffer IC.

To take this one stage further, separate push-pull transistor drivers could be used for each MOSFET. A separate base resistor is needed for each push-pull driver to avoid a MOSFET with a low threshold voltage clamping the drive voltage to all the push-pull drivers. This arrangement also has the advantage that the drive circuits can be positioned very close to the terminals of each MOSFET. The impedance of connections from the drive circuits to the MOSFETs will be minimised and so there will be a reduced likelihood of spurious turn-on. Spurious turn-on can occur when there is a fast change in the drain-to-source voltage. The charging current for the gate-drain capacitance inherent in the MOSFET structure can cause a voltage drop across the gate drive impedance large enough to turn the MOSFET on. The gate drive impedance needs to be kept as low as possible to reduce the likelihood of spurious turn-on.

5.3.5 Resonant power supplies

If a resonant circuit is used then there will be reduced interference and reduced switching losses. The reduced interference is achieved because sinusoidal waveforms, rather than rectangular waveforms, are present in resonant circuits. Rectangular waveforms contain large high frequency harmonic components.

MOSFETs are able to switch at a zero crossing of either the voltage or the current waveform and so switching losses are ideally zero. For example, in the case of a current-fed inverter feeding a parallel resonant load, switching can take place at a zero crossing of voltage, so switching losses are negligible. In this case the sinusoidal drain-source voltage sustained by MOSFETs reduces the likelihood of spurious dv/dt turn-on. This is because the peak charging current for the internal gate-to-drain capacitance of the MOSFET is reduced.

5.3.6 The current-fed approach

Switch Mode Power Supplies (SMPS) using the current-fed topology have a d.c. link which contains a choke to smooth the current in the link. Thus a high impedance supply is presented to the inversion stage. Switching in the inversion stage causes a rectangular wave of current to be passed through the load. The current-fed approach has many advantages for SMPS. It causes reduced stress on devices caused by the slow reverse recovery time of the parasitic diode inherent in the structure of MOSFETs.

The current-fed approach can also reduce problems caused by dynamic unbalance. If more than three MOSFETs are paralleled then it is advantageous to use more than one choke in the dc link rather than wind a single choke out of thicker gauge wire. One of the connections of each choke is connected to the output of the rectification stage. The other connection of each choke is connected to a group of three MOSFETs. This means that if one MOSFET switches on before the others it will carry a current less than its peak pulse value even when many MOSFETs are paralleled.

5.3.7 The parallel operation of MOSFETs in the linear mode

The problems of paralleling MOSFETs which are being used in the linear mode are as follows:

- The paralleled devices may have different threshold voltages and transconductances. This leads to poor sharing.
- MOSFETs have a positive temperature coefficient of gain at low values of gate-to-source voltage. This can lead to thermal runaway.

The unbalance caused by differences in threshold voltage and transconductances can be reduced by connecting resistors (R_S) in the source connections. These resistors are in the gate drive circuit and so provide negative feedback. The negative feedback reduces the effect of different values of V_T and g_{fs}. The effective transconductance g_{fs} of the MOSFET is given in Equation 1.

$$g_{fs} = \frac{1}{R_S + 1/g_m} \qquad (1)$$

R_S must be large compared to $1/g_{fs}$ to reduce the effects of difference in g_{fs}. Values of $1/g_{fs}$ typically vary between 0,1 Ω and 1,0 Ω. Therefore values of R_S between 1 Ω and 10 Ω are recommended. Differential heating usually has a detrimental effect on sharing and so good thermal coupling is advisable.

5.3.8 Conclusions

Power MOSFETs can successfully be paralleled to realise higher power handling capability if a few guidelines are followed.

6 POWERMOS TRANSISTORS IN SMPS

When MOS technology was first widely adopted in IC manufacture in the late sixties, its low-power consumption, high switching speed and positive temperature coefficient of resistance were among the main benefits. More than a decade and a half later, the development of PowerMOS devices has made high-voltage/high-power MOS transistors a serious competitor to bipolar devices in many applications. A typical PowerMOS device is made up of thousands of MOS transistors connected in parallel on a single, common, substrate. By current sharing between individual transistors, the entire device can provide a power output of several hundred watts, depending on the particular device being used. This publication describes how PowerMOS transistors can be used in Switch Mode Power Supply (SMPS) design; a selection guide helps you choose the appropriate transistor, and some design hints are given.

First let us look briefly at some of the properties and advantages of the PowerMOS devices:

- High switching speed – as they are majority-carrier devices, there is no delay in switching caused by minority-carrier storage, unlike bipolar devices.
- Simple drive circuits – they need only a capacitor charging current to turn-on and a bias voltage to maintain the on-state. Bipolar devices require more complex drive circuits.
- Low mean gate drive current – typically 4 mA at 100 kHz. A generous SOA (Safe Operating Area) – secondary breakdown does not occur in PowerMOS transistors under normal operating conditions.
- Simple power uprating – power output can be increased by connecting PowerMOS transistors in parallel with separate gate buffers. Load current is shared between the transistors automatically.
- High-voltage operation – drain-source (V_{DS}) ratings of up to 1000 V.
- ON-resistance positive temperature coefficient – prevents current crowding and ensures uniform crystal current density to eliminate the risks of hot-spots. Thermal runaway does not occur in MOS devices.
- Short-duration current/power overload tolerant – PowerMOS transistors can withstand short-duration current surges within peak current rating.

6.1 PowerMOS Structure and Operation

A PowerMOS transistor consists of a cellular array of individual transistors called source cells. These cells are connected in parallel with hundreds of thousands on a single chip, depending on its size. Fig.35 shows a cross-section through two source cells of an n-channel enhancement PowerMOS device.

Source cells are formed by a double-diffusing n+ and p+ zones into a lightly doped n-type epitaxial layer, the drain, deposited on an n+ substrate. A polysilicon gate pattern overlaps the source cells but is isolated from them by a layer of silicon dioxide. A metallised layer connects the source cells in parallel through windows in the gate pattern. Contact to the gate is made by a small metallised area on the chip.

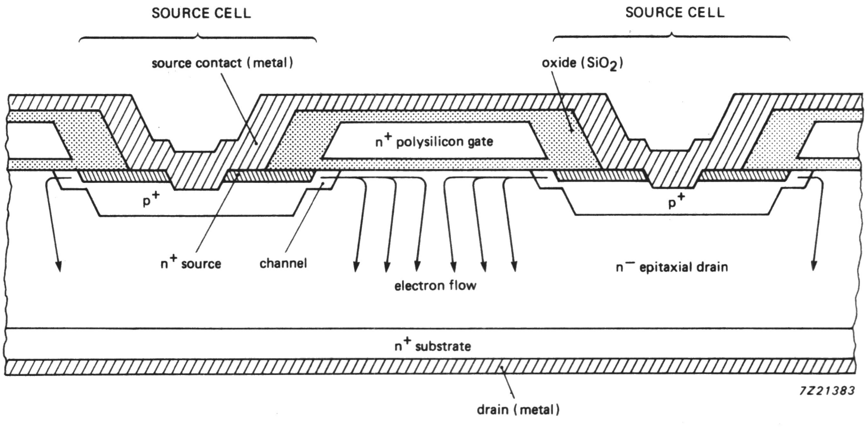


Fig.35 Cross-section through a PowerMOS transistor.

Like all FETs, a PowerMOS transistor is a voltage-controlled device in which the maximum drain current can be controlled by the voltage applied to the gate. The device is biased ON when a positive voltage greater than the threshold voltage $V_{GS(TO)}$ is applied to the gate. An n-type inversion layer then forms in the p+ region beneath the gate, enabling electrons to flow from source to drain. The magnitude of V_{GS} controls the depth of the inversion layer and, therefore, the maximum current which can flow. Conventional current flows verttically from the drain through the bulk of the device and then horizontally through the channel to the source. In the on-state, the drain-source resistance can be as low as 30 mΩ; the exact value depends on the device type, voltage rating and the chip area.

When zero volts are applied to the gate and the gate capacitance is discharged, the transistor is in the off-state, because there is no inversion channel layer. The drain-source resistance is then several MΩ and only a small leakage current flows.

The positive temperature coefficient (PTC) of resistance of MOS devices prevents the formation of hot-spots and ensures an even temperature distribution. When a single source cell is at a higher temperature than its neighbours, its higher resistance causes it to draw a smaller current and the cell cools down. The PTC characteristic of PowerMOS devices makes them inherently self-regulating and it enables the designer to connect PowerMOS devices together in simple parallel circuit configurations.

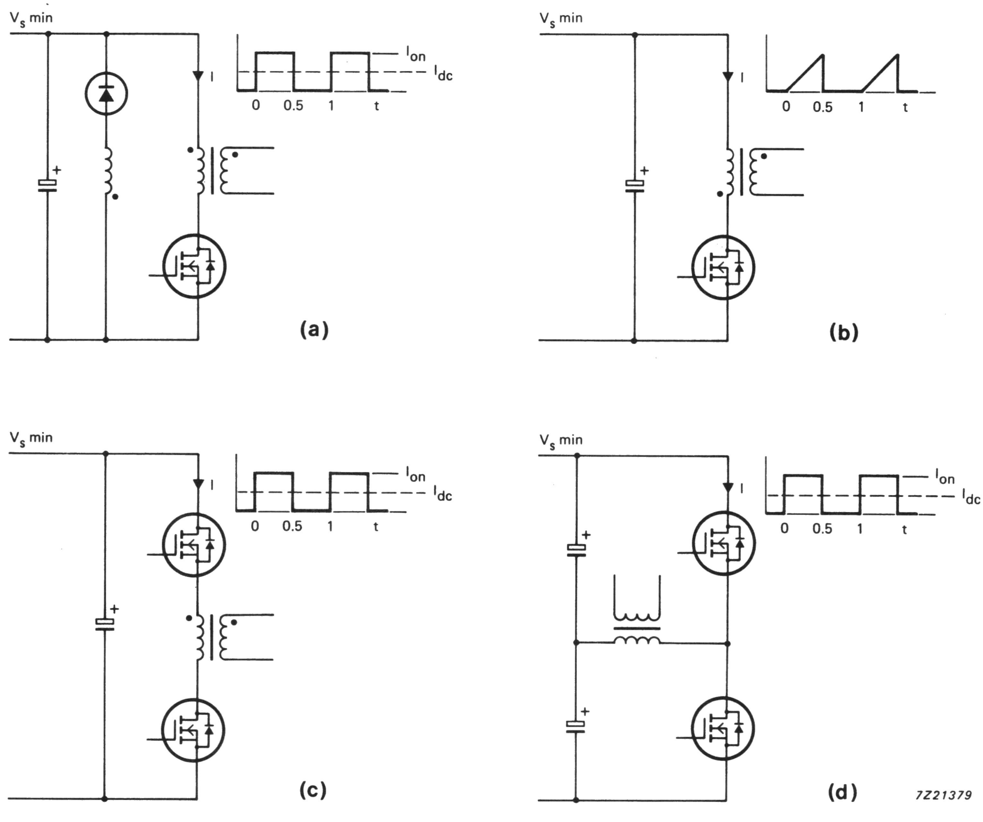


Fig.36 Simplified SMPS circuits using PowerMOS transistors.
(a) forward converter
(b) flyback converter
(c) two-transistor forward converter
(d) half-bridge push-pull converter.

6.2 PowerMOS and SMPS

For the SMPS designer, high switching frequencies offer two major benefits; smaller, less expensive wound components can be used and fast response to load changes is possible with increased bandwidth. The high switching speed of PowerMOS devices enables them to operate efficiently within the 20 to 500 kHz range used in SMPS. Although a PowerMOS device is capable of operating at much higher frequencies, increasing power losses and the possible effects of radio-frequency interference (rfi) make it impractical to do so. If the designer wants to explore the trade-off between switching losses and rfi in an SMPS, he can vary the switching speed simply by changing the value of a resistance connected in series with the gate. A fixed resistor can then be selected when the optimum switching speed has been identified.

With the right switching speed and frequency, switching losses in PowerMOS transistors can be very low. The dominant power loss is the (I^2R) loss in the on-resistance $R_{DS(ON)}$. This is easily calculated when the current waveform of the transistor is known. Fig.36 shows simplified versions of the most common SMPS circuit configuration with PowerMOS transistors, the ideal waveform being shown in each case. The power loss from $R_{DS(ON)}$ and the throughout power for a given efficiency can be calculated from the values of $R_{DS(ON)}$, transistor supply voltage and the waveform for each circuit (see Appendix).

6.3 Selection guide

You can use Fig.37 and Table 1 to select a suitable PowerMOS transistor for a power supply design. This data assumes that the total power loss in the transistor is 5% of the input power. See the Appendix for more details.

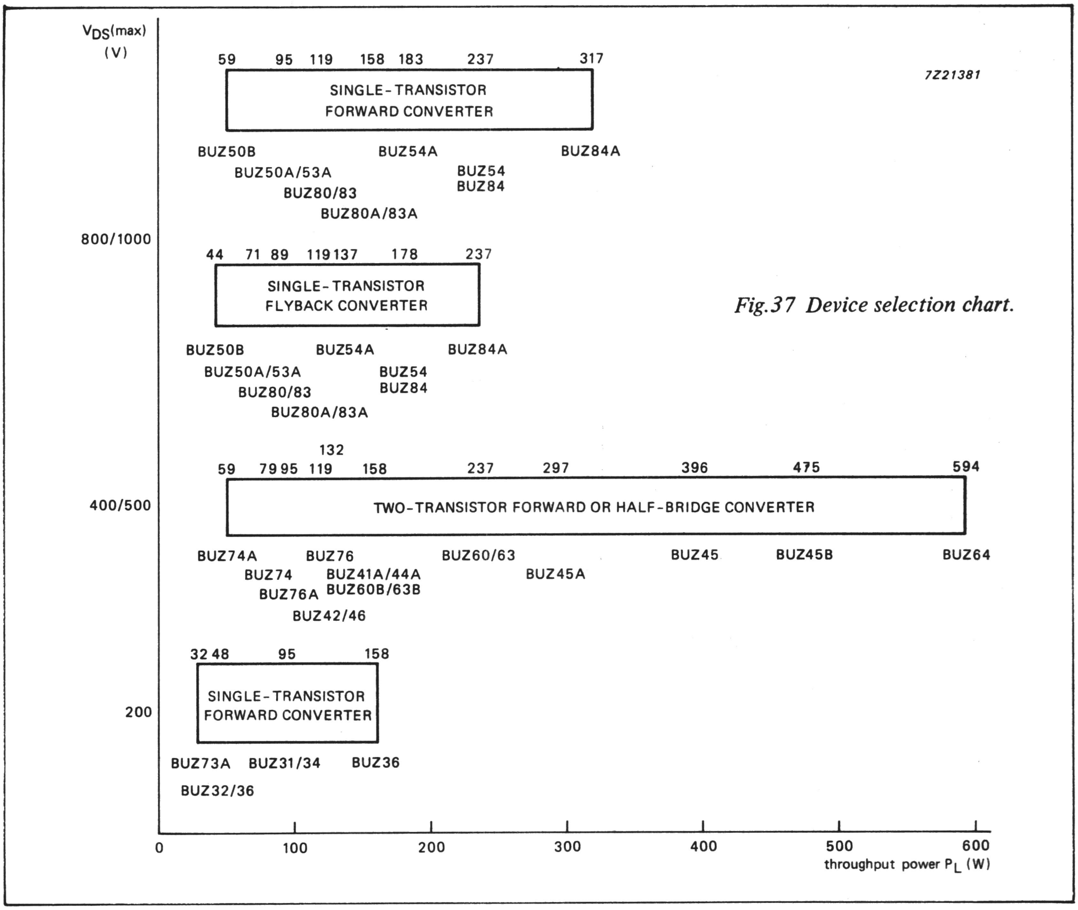


Fig.37 Device selection chart.

Mains-input single-transistor SMPS

	V_{DS} max	$R_{DS(ON)}$ (25 °C)	THROUGHPUT POWER, P_o		LOSS (5% OF P_{in})	
			FORWARD	FLYBACK	FORWARD	FLYBACK
	V	Ω	W	W	W	W
BUZ84A	800	1,5	317	237	16,7	12,5
BUZ84	800	2,0	237	178	12,5	9,4
BUZ54	1000	2,0	237	178	12,5	9,4
BUZ54A	1000	2,6	183	137	9,6	7,2
BUZ80A/83A	800	3,0	158	119	8,3	6,2
BUZ80/83	800	4,0	119	89	6,2	4,7
BUZ50A/53A	1000	5,0	95	71	5,0	3,7
BUZ50B	1000	8,0	59	44	3,1	2,3

Mains-input 2-transistor forward or half-bridge push-pull converter

	V_{DS} max V	$R_{DS(ON)}$ Ω	THROUGHPUT POWER P_o W	LOSS (5% OF P_{in}) W
2 × BUZ64	400	0,4	594	2 × 15,6
2 × BUZ45B	500	0,5	475	2 × 12,5
2 × BUZ45	500	0,6	396	2 × 10,4
2 × BUZ45A	500	0,8	297	2 × 7,8
2 × BUZ60/63	400	1,0	237	2 × 6,2
2 × BUZ60B/63B	400	1,5	158	2 × 4,2
2 × BUZ41A/44A	500	1,5	158	2 × 4,2
2 × BUZ76	400	1,8	132	2 × 3,5
2 × BUZ42/46	500	2,0	119	2 × 3,1
2 × BUZ64A	400	2,5	95	2 × 2,5
2 × BUZ74	500	3,0	79	2 × 2,1
2 × BUZ74A	500	4,0	59	2 × 1,6

P.T.T. 50/60 V input single-transistor forward converter

	V_{DS} max V	$R_{DS(ON)}$ Ω	THROUGHPUT POWER, P_o W	LOSS (5% OF P_{in}) W
BUZ36	200	0,12	158	7,9
BUZ31/34	200	0,2	95	4,8
BUZ73	200	0,4	48	2,4
BUZ32/35	200	0,4	48	2,4
BUZ73A	200	0,6	32	1,7

A 5% power loss in transistor is usually a good compromise between device cost, circuit efficiency and heatsink size. However, power loss is proportional to the square of the throughout power. It is halved by operating at 71% ($1\sqrt{2}$) of the stated throughput power, or doubled by operating at 14% ($\sqrt{2}x$) throughput power. (In most designs, devices will be run within the range 71 to 141% of the throughput power given in the Table). For example, because transistors with more than 10 W loss require large heatsinks, the first type in the Table (BUZ84A) with a stated power of 317 W in a forward converter and a loss of 16,7 W, can be operated at 0,71 of this power (224 W) with the same heatsink, the loss being halved to 8,4 W. Conversely, the last type in the Table (BUZ73A) with a stated throughout power of 32 W and a loss of 1,7 W can be operated at 1,41 X 32 = 42 W with a loss of 3,4 W. Alternatively, the designer could use a pair of BUZ73As with a total power output of 64 W and still only incur a total loss of 3,4 W, assuming that both devices can be mounted on the same heatsink. It would not be possible to connect two bipolar transistors in parallel in this way, because of the risk of thermal runaway.

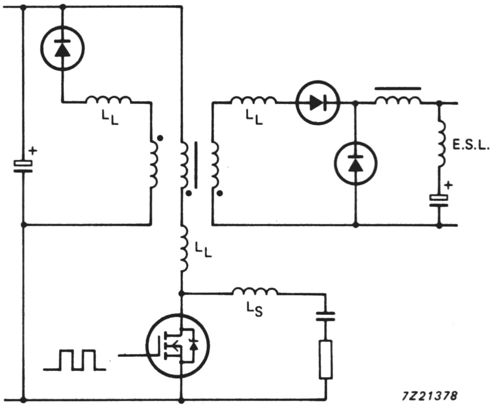


Fig.38 Forward converter with stray inductances included.

6.4 Designing with PowerMOS

PowerMOS transistors are FETs fabricated by established MOS technology. To ensure efficient use of the power rating, the designer should be aware of the following points.

6.4.1 Switching frequency

The highest practical operating frequency is limited by factors such as:

- Stray circuit inductance L_S (Fig.38) and transformer leakage inductance L_L which can cause serious voltage overshoot and ringing on the transistor drain waveform. Voltage overshoot can cause $V_{(BR)DS}$ to be exceeded – with the risk of device failure. Ringing can produce radio frequency interference (rfi).
- Switching losses in the PowerMOS transistor and damping networks.
- HF core losses and winding resistance loss, which can limit reductions in transformer size.
- Equivalent series inductance ESL in output smoothing capacitors (Fig.38) can limit the reduction in output choke size at higher frequencies.

SMPS power rating is also important in determining operating frequency. Below 50 W, transformer windings are thin and hf resistance losses can be ignored, even for frequencies above 100 kHz. At higher output power, hf resistance is significant for frequencies as low as 25 kHz.

For silent operation, frequencies below 20 kHz should never be used. Currently, the highest frequencies used in SMPS are around 500 kHz.

Influence of input voltage on optimum switching frequency

For a given power rating, the current to be switched varies inversely with the converter's operating input voltage. This means that optimum switching frequency also varies with input voltage.

As an example, consider a 100 W power supply operating on a 60 V input in the range 50 to 100 kHz. If it is redesigned to operate on a 12 V input, the stray inductances remain virtually unchanged, but the transistor switching current increases fivefold, resulting in a five times greater voltage overshoot. Reducing the supply voltage by a factor of five increases the percentage voltage overshoot by a factor of twenty five. Switching frequency should be the minimum possible (20 kHz to avoid audible noise from wound components) to give longer switching times without excessive switching losses.

Similarly, if the original power supply is redesigned to operate on a 300 V input, the overshoot problems would be twenty five times less severe. This suggests that the operating frequency could be increased twenty five times. However, as we have already stated, 500 kHz is normally the maximum switching frequency used, mainly because of power losses and problems caused by rfi.

6.4.2 Switching-loss equation

PowerMOS turn-off dissipation must be limited for efficient operating. Turn-on dissipation is normally than that at turn-off because leakage inductance between the output transformer primary and secondary limits the rate of rise of drain current. Switching losses can be calculated for idealised resistive and inductive switching waveforms shown in Figs 39(a) and 39(b) respectively. For example, the switching loss P_{SW}, illustrated for turn-off in Fig.39, is given by:

$$P_{SW} = \frac{I_D \cdot V_D \cdot t \cdot f}{6} \quad \text{(for resistive loads),}$$

or:

$$P_{SW} = \frac{I_D \cdot V_D \cdot t \cdot f}{2} \quad \text{(for inductive loads),}$$

where:

I_D = maximum drain current, V_D = maximum drain voltage, t = transition time, f = switching frequency (= 1/T), T = switching period.

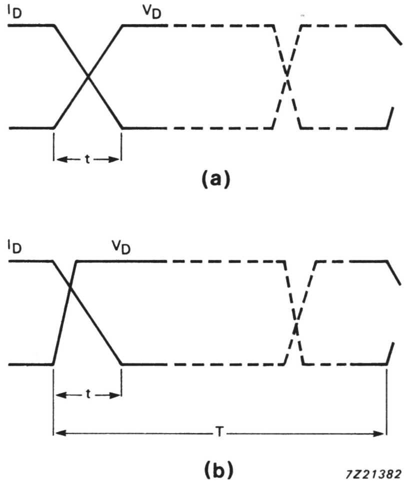


Fig.39 Idealised drain switching waveforms.

Note that with an RC damping network in parallel with the transistor, the switching waveform resembles that for a resistive load.

6.4.3 Circuit configuration options with PowerMOS

Alternative configurations to the single-transistor forward converter shown in Fig.40(a) are the two-transistor forward converter Fig.40(b) or the half-bridge push-pull converter Fig.40(c).

In making valid comparisons between these circuits, the same number of transistors (two) of the same crystal size should be used. The single-transistor forward converter, Fig.40(a), can be implemented as two standard size transistors in parallel, see Fig.41(a). In a mains-input SMPS, 800 V transistors are employed, while those in Fig.41(b), which are equivalent to the circuits of Figs 40(b) and 40(c), require 400 V ratings. Both circuits take the same current (I) from the supply.

For equal losses, the total on-resistance in each circuit must be the same; then:

$$\frac{R_{DS(ON)}\,(800\,\text{V})}{2} = R_{DS(ON)}\,(400\,\text{V}) \times 2$$

that is:

$$R_{DS(ON)}\,(800\,\text{V}) = 4 \times R_{DS(ON)}\,(400\,\text{V}).$$

Therefore, an 800 V, 4 Ω BUZ80 has the same efficiency at the same throughput power as a 400 V, 1 Ω BUZ60.

Ignoring current concentrations determined by the channel spacing, the theoretical on-resistance should be proportional to the breakdown voltage raised to the power 2,5. If this were true in practice, an 800 V transistor would have 40% greater loss than a 400 V device. However, analysis of practical transistors shows that the exponent of 2,5 is not correct for devices between 100 V and 400 V because of existing limits of lithography, the actual figure being between 1,5 and 2. Similarly, for 'equal area' 400 V and 800 V transistor types, the on-resistance of 800 V types is rated 3 to 4 times that for 400 V devices. This gives an exponent value of between 1,6 and 2. Manufacturers are endeavouring to improve the performance of lower voltage devices with improved MOS technology.

Since device performance per unit area is similar for 800 V and 400 V transistors, selection of one of the three circuits in Fig.40 is governed by the cost of other components. The cost of gate drive transformers, additional diodes and other components for Fig.40(b) and 40(c) can be expected to exceed the cost of the demagnetising winding on the output transformer needed for Fig.40(a). Hence two transistors in parallel in the circuit of Fig.40(a) would be fully competitive with two transistors in the circuits of Fig.40(b) and 40(c). When a single transistor can supply the required power, the circuit of Fig.40(a) is clearly the most economical of the three circuits. Available PowerMOS transistors for this circuit can handle power in the range 50 to 300 W at an efficiency of 95%.

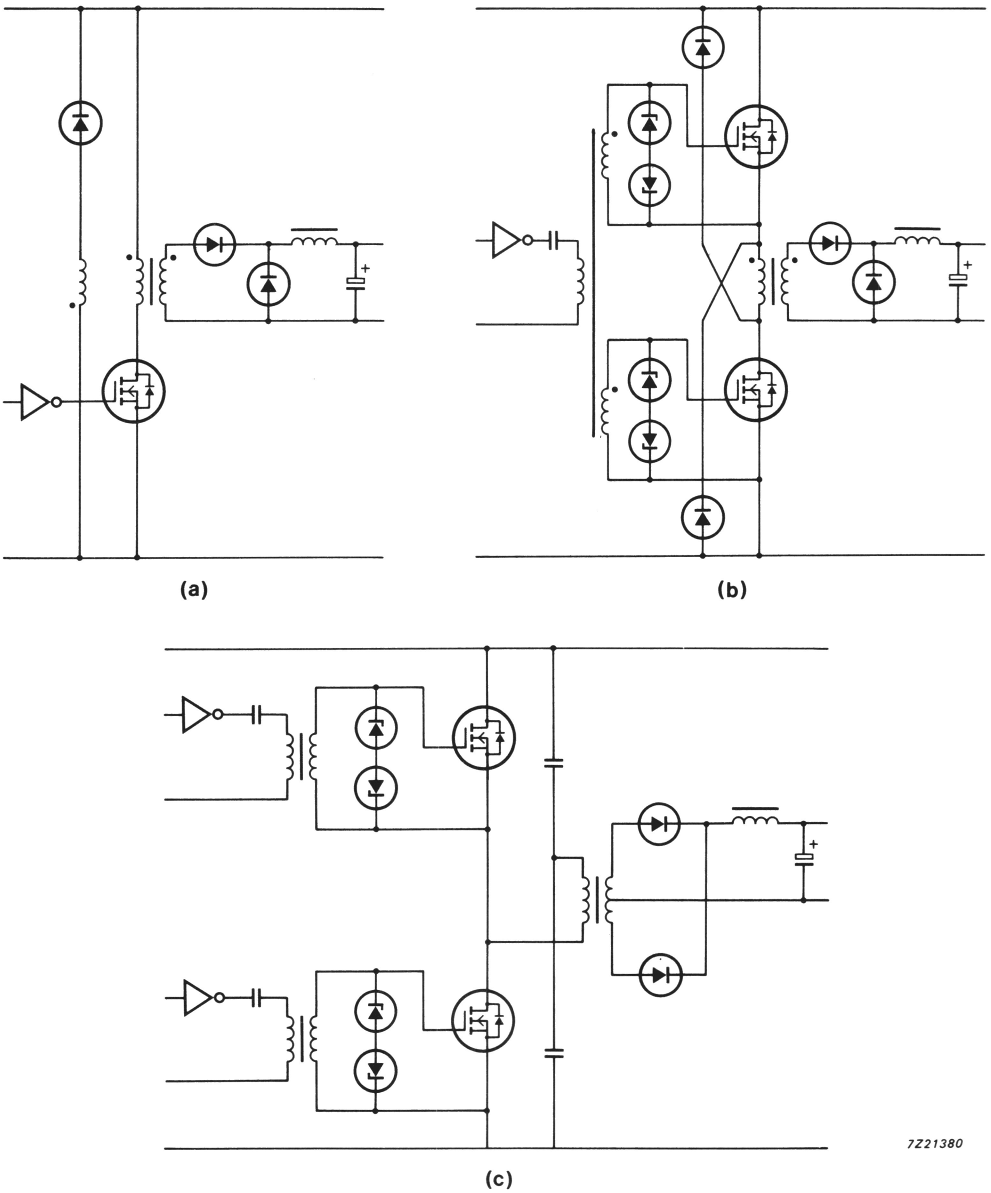

+
(a)
(b)
(c)
7Z21380

Fig.40 Alternative converter configurations.

The main selection criteria for choosing between 400 V and 800 V PowerMOS transistors in forward and flyback mains input SMPS are summarised below:

	400 V transistors	800 V transistors
Number of transistors	2	1
Total silicon area	1	1
Number of diodes	2	1
Demagnetising winding	no	yes
Control and drive circuit	complex	simple

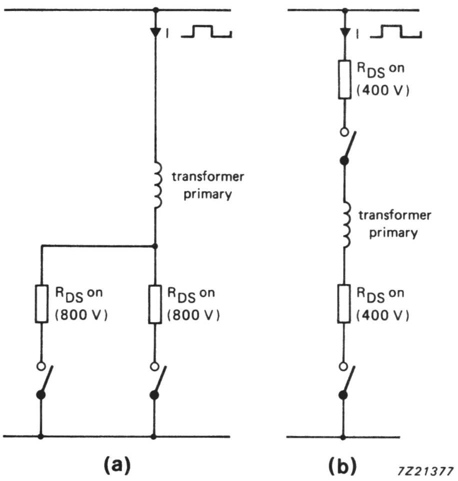


Fig.41 Simplified circuits.

6.4.4 Paralleling PowerMOS transistors

A major advantage of PowerMOS, is that a gate-drive circuit can drive a range of transistors with practically any voltage and current ratings. In addition, the stability offered by the PTC characteristic of PowerMOS devices makes it easy to uprate power supplies by placing PowerMOS transistors in parallel. For example, to modify a power supply design for 41% more power, another PowerMOS transistor of the same type could be added in parallel with the existing one on the same heatsink. (The only proviso is that the second transistor may require matched transfer characteristics with similar $R_{DS(ON)}$ and threshold voltage). For 100% more power, the size of the heatsink required by the additional transistor would need to be doubled. The drive circuit will then require a further gate drive input via a series resistor.

Since uprating an existing PowerMOS SMPS only requires alterations to the power circuit component values, it is very simple and economical to implement.

APPENDIX: Calculation of Table values

The throughput powers given in the Table are calculated for a power loss in $R_{DS(ON)}$ equal to 5% of the input power when $T_j = 125\,^\circ C$. The supply voltage V_{Smin} is a notional minimum d.c. input voltage corresponding to a PowerMOS switch duty factor D = 0,5. V_{Smin} is assigned a value of 200 V d.c. for mains-input converters and 40 V for PTT input converters (postal and telecommunication applications).

Let I_{rms} = the rms value of the current in $R_{DS(ON)}$. The loss in $R_{DS(ON)}$ is given by:

$$\begin{aligned} \text{Loss}R_{DS(ON)} &= I_{rms}^2\, R_{DS(ON)}\,(125\,^\circ C),\\ &= K^2\, I_{dc}^2\, R_{DS(ON)}\,(125\,^\circ C), \end{aligned}$$

where I_{dc} is the input current and $K = I_{rms}/I_{dc}$.

For 5% loss:

$$\begin{aligned} K^2 I_{dc}^2 R_{DS(ON)}\,(125\,^\circ C) &= 0{,}05\, P_{in},\\ &= 0{,}05\, I_{dc}\, V_{Smin}. \end{aligned}$$

Therefore:

$$I_{dc} = \frac{0{,}05\, V_{Smin}}{K^2 R_{DS(ON)}\,(125\,^\circ C)}.$$

Throughput power P_o is given by:

$$\begin{aligned} P_o &= 0{,}95\, P_{in},\\ &= 0{,}95\, I_{dc}\, V_{Smin},\\ &= 0{,}95\, \frac{0{,}05\, V_{Smin}^2}{K^2 R_{DS(ON)}\,(125\,^\circ C)},\\ &= 0{,}0475\, \frac{V_{Smin}^2}{K^2 R_{DS(ON)}\,(125\,^\circ C)}. \end{aligned}$$

For a mains-input single transistor forward converter:

$V_{Smin} = 200$ V, $K = 1{,}414$,

$R_{DS(ON)}\,(125\,^\circ C) = 2\, R_{DS(ON)}\,(25\,^\circ C)$.

Therefore:

$$\begin{aligned} P_o &= 0{,}0475\, \frac{200^2}{1{,}414^2 \times 2 \times R_{DS(ON)}\,(25\,^\circ C)}.\\ &= \frac{475}{R_{DS(ON)}\,(25\,^\circ C)}. \end{aligned}$$

For a mains-input single transistor flyback converter:

$V_{Smin} = 200$ V, $K = 1{,}633$,

$R_{DS(ON)}\,(125\,^\circ C) = 2\, R_{DS(ON)}\,(25\,^\circ C)$.

Therefore:

$$\begin{aligned} P_o &= 0{,}0475\, \frac{200^2}{1{,}633^2 \times 2 \times R_{DS(ON)}\,(25\,^\circ C)},\\ &= \frac{365}{R_{DS(ON)}\,(25\,^\circ C)}. \end{aligned}$$

For a mains-input two-transistor forward or half-bridge push-pull converter:

$V_{Smin} = 200\,V$, $K = 1{,}414$,

$R_{DS(ON)}\ (125\,^{\circ}C) = 4\ R_{DS(ON)}\ (25\,^{\circ}C)$.

Therefore:

$$P_o = 0{,}0475\,\frac{200^2}{1{,}414^2 \times 4 \times R_{DS(ON)}\ (25\,^{\circ}C)},$$

$$= \frac{237{,}5}{R_{DS(ON)}\ (25\,^{\circ}C)\ \text{of one transistor}}.$$

For a PTT-input single-transistor forward converter:

$V_{Smin} = 40\,V$, $K = 1{,}414$,

$R_{DS(ON)}\ (125\,^{\circ}C) = 2\ R_{DS(ON)}\ (25\,^{\circ}C)$.

Therefore:

$$P_o = 0{,}0475\,\frac{40^2}{1{,}414^2 \times 2 \times R_{DS(ON)}\ (25\,^{\circ}C)},$$

$$= \frac{19{,}0}{R_{DS(ON)}\ (25\,^{\circ}C)}.$$

7 HIGH-SPEED MOSFET DRIVE CIRCUITS

In order to turn a power MOSFET on, the input capacitance between the gate and the source terminals needs to be charged up. The input capacitance is typically 1 or 2 nF and has to be charged up to about 10 V for the device to be fully on. The following drive circuits can charge the gate-source capacitance particularly speedily and so realise extremely fast switching speeds. Switching losses are directional proportional to the switching frequency and greater than conduction losses above a frequency of about 500 kHz, although this crossover frequency is dependent on circuit configuration. Thus for operation above 500 kHz it is important to have fast transition times.

At frequencies below 500 kHz the circuit in Fig.42 is often used. Above 500kHz the use of the IC DS0026 instead of the 4049 is recommended. The DS0026 has a higher current sinking and sourcing capability which is 1,5 A. It is a device capable of charging a capacitance of 1000 pF in as short a time as 25 ns.

In Fig.43 the value of capacitor C1 is made approximately equal to the input capacitance of the driven MOSFET. Thus the RC time constant for the charging circuit is approximately halved. The disadvantage of this arrangement is that a drive voltage of 30 V instead of 15 V is needed because of the potential divider action of C1 and the input capacitance of the driven MOSFET. A small value of C1 would be ideal for a fast turn-on time and a large value of C1 would produce a fast turn-off.

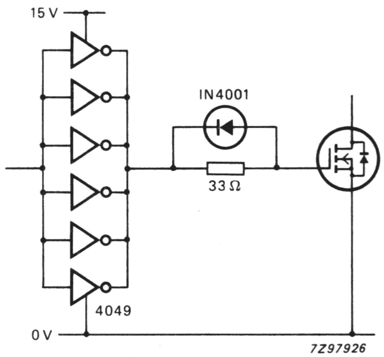


Fig.42 A MOSFET drive circuit using a hex CMOS buffered inverter IC.

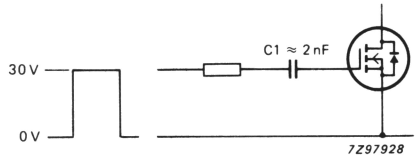


Fig.43 A simple drive circuit with reduced effective input capacitance.

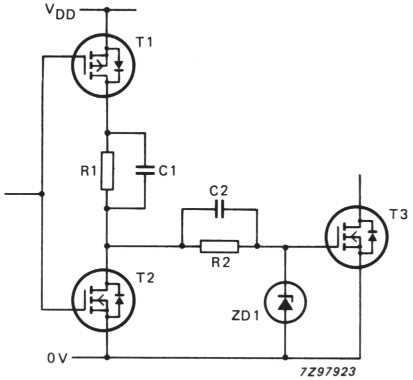


Fig.44 A drive circuit with reduced effective input capacitance and prolonged reverse bias at turn-off.

The circuit in Fig.44 replaces C1 by two capacitors and enables fast turn-on and fast turn-off. When T1 is turned on the driven MOSFET T3 is driven initially by a voltage V_{DD} feeding three capacitors in series, namely C1, C2 and the input capacitance of T3. Since the capacitors are in series their equivalent capacitance will be low and so the RC time constant of the charging circuit will be low. The value of C1 is low to ensure a very fast turn-on time.

The voltage across C2 will then settle down to $(V_D - V_{ZD1}) \cdot R2/(R1 + R2)$. Therefore the inclusion of resistors R1 and R2 means that C2 can be made larger than C1 and still have a large voltage across it before the turn-off of T3. Thus C2 can sustain a reverse voltage across the gate-source of T3 for the whole of the turn-off time. When T2 is turned on and T1 is off the discharge circuit will be as shown in Fig.45. The initial discharging current will be given by Equation 1:

$$I = V_{ZD1} + \frac{R2(V_{DD} - V_{ZD1})}{(R1 + R2)} \; R_{stray} \qquad (1)$$

as opposed to V_{ZD1}/R_{STRAY} without C2.

Making V_{DD} large will make turn-on and turn-off times very small.

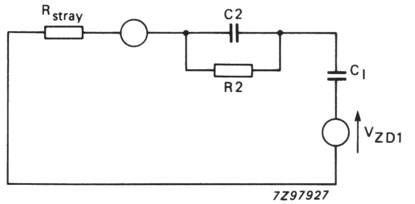


Fig.45 The discharge path for the input capacitance of a MOSFET driven by the circuit in Fig.44.

There may well be some advantages in charging the input capacitance of the MOSFET from a constant current source rather than a constant voltage source.

For a given drain-source voltage a fixed amount of charge has to be transferred to the input capacitance of a MOSFET to turn it on. As illustrated in Fig.46, this charge can be transferred more quickly with a constant current of magnitude equal to the peak current from a constant voltage source.

One circuit which could be used to realise a constant current source is that shown in Fig.47 along with the switching sequence. When MOSFETs T1 and T2 are on, current builds up in the inductor as shown in Equation 2.

$$\Delta I = \frac{V_{DD}\Delta t}{L} \qquad (2)$$

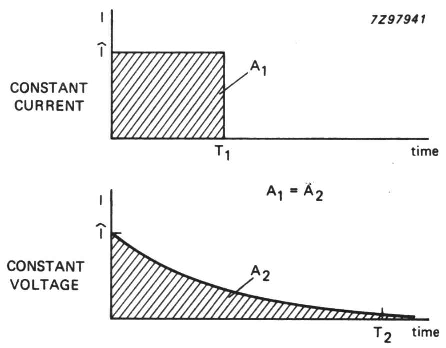


Fig.46 Comparison of switching times for MOSFETs driven from constant current and constant voltage sources.

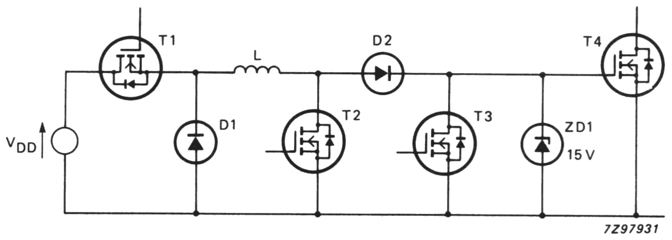


Fig.47 A constant current drive circuit.

Diode D2 prevents the input capacitance of the MOSFET T4 being discharged when T2 is on. When T2 is on, current freewheels through D1 and T2. When all the MOSFETs are off the inductor current flows into the input capacitance of the MOSFET T4. The time taken to turn the MOSFET T4 on is given by Equation 3:

$$\text{Turn-on time} = \frac{q_g}{I} \qquad (3)$$

where q_g is the gate charge associated with the drain-source voltage across the MOSFET just before it is turned on. When the gate-source voltage reaches 15 V then zener diode ZD1 clamps the gate-source voltage. The inductor current then flows through ZD1 until T2 turns on, when it freewheels.

The disadvantages of this circuit are that there is a need for logic to implement the switching sequence. It also has three MOSFETs. The drive circuit to T1 needs to be isolated from 0 V.

To achieve fast switching speeds the bi-polar push-pull circuit shown in Fig.48 can be replaced by a MOSFET equivalent as shown in Fig.49. The positions of p and n channel MOSFETs may be interchanged and connected as shown in Fig.50. However it is likely that one MOSFET will turn on faster than the other turns off, and so the circuit in Fig.50 may cause a current spike during the switching interval. The peak-to-average current rating of Philips PowerMOS is excellent so this current spike does not cause damage. Reliability will be impaired however. In Fig.49 the input capacitance of the driven MOSFET is charged up to $V_{DD} - V_T$, where V_T is the threshold voltage, at which point the MOSFET turns off. Therefore when M2 turns on there is no current spike. The following points are worth noting when discussing very fast drive circuits:

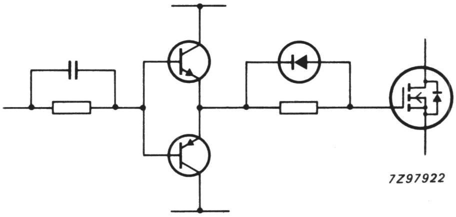


Fig.48 A push-pull drive circuit using bipolar transistors.

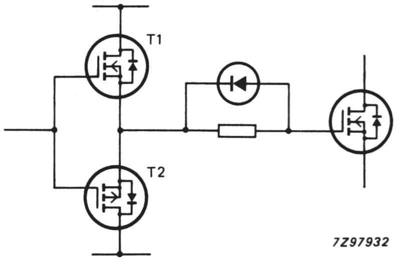


Fig.49 A push-pull drive circuit using MOSFETs in the common drain connection.

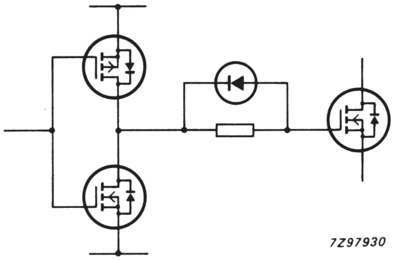


Fig.50 A push-pull drive circuit using MOSFETs in the common source connection.

- SMPS working in the 1 - 15 MHz range sometimes use resonant drive circuits. These SMPS are typically the QRC (Quasi-Resonant Circuits). The resonant drive circuits do not achieve faster switching by the fact that they are resonant. By being resonant they recoup some of the drive energy and reduce the gate drive power. There are two main types of QRC – zero voltage and zero current switching circuits. In one of these types fall times are not critical and in the other rise times are not critical. On the critical switching edge a normal fast switching edge is provided by using the circuits above or similar types. For the non-critical edge there is a resonant transfer of energy. Thus drive losses of $q_g \cdot V_{GS} \cdot f$ become $0{,}5 \cdot q_g \cdot V_{GS} \cdot f$.

- It is usual to provide overdrive of the gate-source voltage. This means charging the input capacitance to a voltage which is more than sufficient to turn the MOSFET fully on. This has advantages in achieving lower on-resistance and increasing noise immunity. The gate power requirements are increased however when overdrive is applied. It may well be a good idea therefore to drive the gate with only 12 V instead of 15 V. This could be looked on as trading off reduced gate drive losses for increased conduction losses.
- It is recommended that a zener diode be connected across the gate-source terminals of a MOSFET to protect against overvoltage. This zener can have a capacitance which is significant compared to the input capacitance of smaller MOSFETs. The zener can thus affect switching times.

It can be seen that by taking note of the above points discussed, switching times of tens of ns can be achieved using Philips PowerMOS.

8 THE PROTECTION OF PHILIPS POWERMOS AGAINST ELECTROSTATIC DISCHARGE

Charge accumulates on insulating bodies and voltages as high as 20 kV can be developed e.g. by walking across a nylon carpet. Electrically the insulator can be represented by many capacitors and resistors connected as shown in Fig.51. The value of these resistor is large and consequently it is not possible to discharge an insulator by connecting it straight to ground. An ion source is necessary to discharge an insulator.

Since MOSFETs have a very high input impedance, typically > 10^9 Ω at dc, there is a danger of static electricity building up on the gate-source capacitance of the MOSFET. This can lead to damage to the thin gate oxide. There are two ways in which the voltage across the gate-source terminals of a MOSFET can be increased to its breakdown voltage by static electricity. Firstly the charged object can be brought in contact with the MOSFET terminals or with tracks electrically connected to the terminals. This is represented electrically by Fig.52.

$$V_{GS} = \frac{Q_{In}}{C_{In} + C_{GS}} = \frac{Q_{In}}{C_{In} + \frac{A\epsilon_o \cdot \epsilon_{Si}}{d}}$$

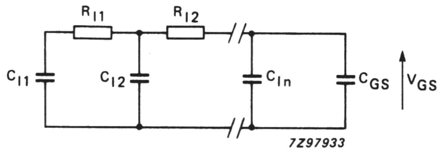


Fig.52 The gate-source terminals of a MOSFET connected to a charged insulator.

Secondly, charge can be induced onto the terminals of the MOSFET. Electrically this can be represented by the circuit in Fig.53.

$$V_{GS} = \frac{Q_{In}}{C_{In} \quad \frac{C_T \cdot C_{GS}}{C_T + C_{GS}}} \cdot \frac{C_T}{C_T + C_{GS}}$$

From Figs 52 and 53 it can be seen that as the total area of the gate-source region increases then the sensitivity of the devices to Electro-Static Discharge (ESD) will decrease. Hence power MOSFETs are less prone to ESD than CMOS devices. Also, for a given voltage rating, MOSFETs with a larger die area (i.e. the devices with lower on-resistance) are less prone to ESD than smaller dice.

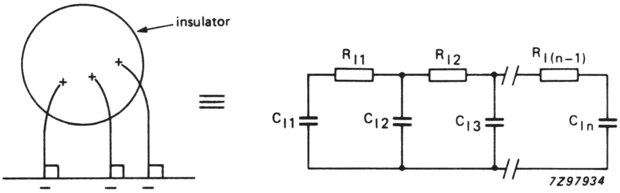


Fig.51 An electrical representation of a charged insulator.

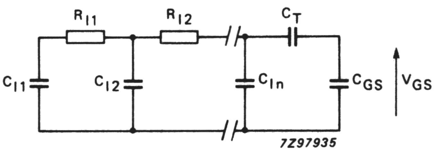


Fig.53 A charged insulator inducing charge on the terminals of a MOSFET.

To prevent the destruction of MOSFETs through ESD a two-pronged approach is necessary. Firstly it is important to minimise the build-up of static electricity. Secondly, measures need to be taken to prevent the charging up of the input capacitance of MOSFETs by static electric charges.

In the Philips manufacturing facilities many precautions are taken to prevent ESD damage and these are summarised as follows:

- It is important to ensure that personnel working with MOSFETs are aware of the problems and procedures that have to be followed. This involves the training of staff. Areas in which MOSFETs are handled are designated Special Handling Areas (SHA) and are clearly marked. Monthly checks are made to ensure that anti-static rules are being rigorously implemented.
- Some materials are more prone to the build-up of static electricity than others (e.g. polyester is worse than cotton). Therefore it is important to minimise the use of materials that enhance the likelihood of build-up of static electricity. Materials best avoided are acetate, rayon and polyester. The wearing of overclothing made from polycotton with 1% stainless steel fibre is one solution. In cleanrooms nylon overalls which have been antistatically treated are worn. The use of insulating materials should be avoided.
- Work benches and floors should be covered in a static dissipative material and connected to a common earth. A highly conductive material is not used since it would create an electric shock hazard and cause too rapid a discharge of charged material. From the point of view of ESD, materials can be classified according to their conductivity as follows:

  Insulator ($> 10^{14}$ Ω/square)
  Antistatic ($10^{9} - 10^{14}$ Ω/square)
  Static dissipative ($10^{5} - 10^{9}$ Ω/square)
  Conductor ($< 10^{5}$ Ω/square)

- Conducting straps are used to electrically connect personnel to the point of common earthing. This prevents the build-up of static charge on staff. The connection is static dissipative to prevent an electric shock hazard.
- Air plays an important part in the build-up of static electricity. This is particularly troublesome in a dry atmosphere.

Many of the techniques mentioned above are referred to in BS5783.

The following precautions should be taken to prevent damage to MOSFETs by electrostatic build-up of charge:

- When MOSFETs are being transported or stored they should be in antistatic containers. These containers should be totally enclosed to prevent charges being induced onto the terminals of devices.
- If MOSFETs have to be left out on the bench, e.g. during a test sequence, they should be in sockets which have the gate and source pins electrically connected together.

The precautions that should be taken at the customers' premises are the same as above. It should be remembered that whenever a MOSFET is touched by someone there is a danger of damage. The precautions should be taken in every area in which MOSFETs are tested or handled. In addition where devices are soldered into circuits with a soldering iron an earthed bit should always be used.

The probability of device destruction caused by ESD is low even if only the most rudimentary precautions are taken. Without such precautions however, a few failures would be inevitable taking into account the large numbers of Philips PowerMOS devices now being designed into equipment. The adoption of the precautions outlined above will mean that ESD will no longer be a problem.

9 PHILIPS POWERMOS QUALITY AND RELIABILITY

9.1 PowerMOS quality

The quality of semiconductor components is an increasingly important aspect of the electronics industry. Users of semiconductors operate in highly competitive markets and are constantly striving for ways to offer better value for money to their customers. The manufacturers of semiconductor components can help their customers by supplying good quality parts. The broad concept of 'good quality' can be narrowed to the twin concepts of conformance and reliability. The conformance of a product is its ability to meet the customer's requirement at the time that the customer receives it. A product with good conformance will enable the user to reduce his costs by reducing incoming inspection and by obtaining better first time yields in his manufacturing process (i.e. lower fall-off rate). The reliability of a product is its ability to continue to operate satisfactorily over a long period of time. Again, a product with good reliability enables cost reduction because of reduced in-warranty repairs, but moreover generates customer satisfaction because of reduced down-time.

Within the Philips PowerMOS operation, we recognize the quality requirements of our customers, and this article describes how we achieve them.

9.2 PowerMOS Wafer Fab.

The operational policy of the PowerMOS Wafer Fab. is one of strong cleanroom disciplines, statistical process control and low throughput times. This policy leads to good yields and good quality.

The PowerMOS Wafer Fab. is housed in a purpose-built, state-of-the-art Class 100 cleanroom which in practice achieves close to Class 10 conditions. This is the result of the cleanroom disciplines and a strong emphasis on contamination control including particle measurements in air, in liquids and on silicon plus regular checks to monitor levels of metallic contamination. Statistical process control is being operated, covering all aspects of Wafer Fab. processing. Low throughput times are achieved through close operational controls and specialised logistics systems. Incoming materials and vendor information are inspected by the Quality Department who also perform regular process audits.

9.3 Process controls

Details of the PowerMOS process controls in the Wafer Fab. and in Assembly are shown below:

POWERMOS WAFER FAB. PROCESS CONTROLS

PROCESS	CONTROL PARAMETERS INSPECTED
Oxidation	thickness, particle control
Photolith	dimensions and particulate contamination, defect density
Oxidation	thickness
Implant	sheet resistivity
Diffusion and Oxidation	thickness, sheet resistivity, junction depth
Photolith	dimensions and particle contamination, defect density
Oxidation	thickness
Polysilicon deposition	thickness, sheet resistivity
Implant	sheet resistivity
Photolith	dimensions and particulate contamination, defect density, gate oxide Breakdown Voltage
Implant and Oxidation	oxide thickness and junction depth
Implant and Diffusion	sheet resistivity and junction depth
Low temperature oxidation	thickness, particle control
Photolith	dimensions and particulate contamination, defect density
Front metal	thickness
Photolith	dimensions and particulate contamination, defect density
Plasma Nitride	thickness
Photolith	dimensions
Back metal	thickness
Probe test and ink	100% electric measurements, pass/fail
Visual inspection	each batch, visual defects

POWERMOS ASSEMBLY PROCESS CONTROLS AND INSPECTION PROCEDURES

PROCESS	INSPECTION
SLICE SAWING	alignment, width, chipping, depth
DIE BOND WIRE BOND	damage, orientation, wetting, temperature position, shape, pull (destructive 100% marking of defective devices and non-destructive
PRE-ENCAP INSPECTION	damage, wetting, wirebonding sample from each batch. Failure results in 100% inspection.
ENCAPSULATION	correct plastic, holes, damage to legs and tabs
DEFLASH	flash and holes
CROP 1	burrs, damage to legs
DIP SOLDER	solder position and wetting quality
CROP 2	damage to tabs, legs, burrs, removal of marked reject devices
100% TEST (Electrical)	
FINAL Q.C.	sample from each batch – marked rejects, damage, burrs, holes, diptinning, dirt, staining
PRINT	correct print, legible
100% TEST (Electrical)	
SAMPLE TEST AND INSPECT	independent electrical and visual sample inspection on every batch
PACK AND SHIP	paperwork, labelling, quantity

9.4 Conformance assurance

The conformance to specification of a Philips PowerMOS device is assured by the product design and the process controls previously mentioned. A particular point to note is that each and every device is electrically tested twice, once before print and once after print. This serves two purposes:

a) it protects against the possibility of mixing at the print stage and

b) it protects against the possibility of a mistested device from the first test being delivered.

After the second 100% test a sample electric and visual test is done by the Quality department (independent of production). A sampling scheme is used which provides assurance to a 0,1% AQL. The conformance requirements we place upon our products are much more stringent than an inspection sampling scheme can provide. Our target is to achieve less than 50 inoperatives in every 1 million products (i.e.< 50 ppm) 50 ppm expressed as a percentage is 0,005%.

9.5 Reliability assurance

The reliability of a PowerMOS device in a customer's application depends on the design of the device manufacturing process and on the design of the application itself and of course on the precision with which the manufacture of those designs are carried out. The device manufacturing process has been designed so that an application which uses the device within its published ratings will have extremely high reliability. In order to assess a new product design or a potential improvement to an existing product a series of reliability tests are carried out which stress the devices to levels beyond those that will be experienced in the actual application. Feedback from these tests to the product design ensures that only designs with proven reliability will reach our customers. The reliability proving tests that are used for PowerMOS products are described below.

9.5.1 High temperature dc blocking

The purpose of this test is to assess the leakage current stability at the extremes of voltage and temperature. It is a sensitive and searching test which will reveal the presence of contamination within the structure of the devices. It is a good indicator of the long term reliability of the product.

Typical test conditions: $V_{DS} = V_{DS\,max}$
$T_j = 150\,°C$
V_{GS} shorted

9.5.2 High temperature storage

This is another test to assess device stability. The high temperature accelerates any chemical reactions that might take place within the device under normal operating conditions. Electrical measurements are performed periodically in order to detect any changes.

Typical test condition: $T_a = 150\,°C$

9.5.3 Temperature cycling

The component parts of a semiconductor device have differing coefficients of thermal expansion and they are mechanically stressed because of the package assembly process. Temperature cycling between temperature extremes sets up additional stresses because of the different coefficients of expansion, and enables the ability of the device to withstand the repeated extremes of stress to be assessed.

Typical test condition: $T_{a\,min} = -55\,°C$
$T_{a\,max} = 150\,°C$

9.5.4 Thermal fatique (or power cycling)

The thermal fatique test simulates the self heating and cooling which a device experiences in operation. The device is heated by passing a current through it and then cooled by passing water through its heatsink. The relative movement of the components of any semiconductor device during heating and cooling cycles will eventually cause it to fail through fatique. The thermal fatique test is used to ensure that the construction of the device is such that it can withstand many more cycles of heating and cooling than will be required by its normal operation.

Typical test conditions: $T_{j\,min} - T_{j\,max} = \Delta T_j = 100\,°C$

9.5.5 High temperature gate bias

This is a test of the gate oxide. The gate is biased with respect to the source which is shorted to the drain. The maximum rated voltage is applied to the gate. Defects or contamination in the gate oxide can lead to failure (I_{gss} short circuit).

Typical test conditions: $V_{gss} = 20\,V$; $T_a = 150\,°C$

9.5.6 Humidity with clocking voltage

Because of the possibility that the presence of water molecules coupled with voltage on a semiconductor device may cause it to become electrically unstable, a combined humidity and blocking voltage test is used.

Typical test conditions: 85 °C; 85% RH; $V_{DS\,max}$

9.5.7 Autoclave

The autoclave test subjects devices to water vapour at 121 °C and a pressure of +1 atmosphere. This test assesses the passivation properties of a device under extremely humid conditions.

10 EXPLANATION OF THE DATA SHEET PARAMETERS

10.1 MOS handling

- The input (gate-source) must be protected against voltages at ±20 V for power transistors. Even short-term voltages in excess of this level can destroy transistors.
- MOSFETs have to be protected against electrostatic charges. The general handling regulations for electrostatic-discharge sensitive (ESDs) devices should be observed. This sensitivity of the devices increases with decreasing chip area and the resulting smaller input capacitance C_{iss}.
- To protect such transistors against electrostatic charge during shipping, they are packed in anti-static containers. When PowerMOS transistors are assembled, the same regulations should be observed as those which generally apply the MOS devices.
- In circuit design, it should be observed that the transistor is not operated with open-circuit terminals.

10.2 Use of subscripts

10.2.1 Voltages

Two subscripts are used, defining the points between which a voltage is measured. Positive potentials of the point defined by the first subscript correspond to positive values of the voltage referred to the point defined by the second subscript (reference point), e.g. V_{GS}.

10.2.2 Currents

At least one subscript is used. Positive currents that appear in the component at the point defined by the first subscript correspond to positive values of current, e.g. I_{GS}.

10.3 Absolute maximum ratings

The limits stated in the data sheets are absolute limit values. Exceeding one of these limits can lead to the destruction of the component, even if the other limits are not fully utilized. If not otherwise specified, the maximum ratings apply to 25 °C.

10.3.1 Drain-source voltage V_{DS}

Maximum permissible value of the voltage between drain and source.

10.3.2 Drain-gate voltage V_{DGR}

Maximum permissible value of the voltage between drain and gate, when bridging gate-source connections with a predefined resistance.

10.3.3 Continuous drain current I_D

Maximum permissible value of the direct current at the drain connection.

10.3.4 Pulsed drain current I_{DM}

Maximum permissible peak value of the drain current during pulse operation as specified in the diagram 'safe operating area' for a repetitive pulse width and duty cycle.

10.3.5 Gate-source voltage V_{GS}

Maximum permissible value of the voltage between gate and source.

10.3.6 Maximum power dissipation P_D

Maximum permissible power dissipation of the transistor.

10.3.7 Operating temperature range T_j

The range of the permissible chip temperature, within which the transistor may be operated continuously.

10.3.8 Storage temperature range T_{stg}

The temperature range within which the transistor may be stored or transported without electrical load.

10.3.9 Maximum soldering temperature T_{sold}

The maximum permissible temperature during soldering at the terminals of the component, at a specified distance from the case and for a specified length of time. (see Soldering data on Power transistors).

10.3.10 Thermal resistance $R_{th\,j\text{-}mb}$

Thermal resistance between chip and mounting base at thermal equilibrium.

10.3.11 Thermal resistance $R_{th\,j\text{-}a}$

Thermal resistance between chip and ambient air at thermal equilibrium.

10.4 Electrical characteristics

The values stated under 'electrical characteristics' are to be taken as typical values. In many cases, these electrical characteristics are supplemented by limit values.
The values apply to 25 °C if no other temperature is specified.

10.4.1 Drain-source breakdown voltage $V_{(BR)DSS}$

The voltage between the drain and source at a specified drain current; gate and source short-circuited.

10.4.2 Gate threshold voltage $V_{GS(TO)}$

The value of the gate-source voltage at a specified drain current and at a specified drain-source voltage.

10.4.3 Zero gate voltage drain current I_{DSS}

The value of the drain current at a specified drain-source voltage and short-circuited gate-source. This value applies to 25 °C and a specified higher chip temperature.

10.4.4 Gate-source leakage current I_{GSS}

The value of the gate leakage current at a specified gate-source voltage and short-circuited drain-source.

10.4.5 Drain-source on-state resistance $R_{DS(ON)}$

The value of the resistance between the drain and source at a specified gate-source voltage and drain current.

10.4.6 Forward transconductance g_{fs}

Ratio between the change in drain current and a given change in gate-source voltage at specified drain-source voltage and specified drain current.

10.4.7 Input capacitance C_{iss}

That capacitance measured between gate and source connections with drain-source connections short-circuited for ac voltage. The values of the dc voltage between gate-source and drain-source connections, as well as the measuring frequency are specified.

10.4.8 Output capacitance C_{oss}

That capacitance measured between the drain and source connections with the gate-source connections short-circuited for ac voltages. The values of the dc voltage between gate-source and drain-source connections, as well as the measuring frequency are specified.

10.4.9 Reverse transfer capacitance C_{rss}

That capacitance measured between drain and gate with the source connected to ground. The values of the dc voltage between gate-source and drain-source, as well as the measuring frequency are specified.

10.4.10 Turn-on time $t_{on} = t_{d(on)} + t_r$

Sum of:
the turn-on delay time $t_{d(on)}$ measured between the 10% value of the gate-source voltage and the 90% value of the drain-source voltage swing and the rise time t_r measured between the 90% value and the 10% value of the drain-source voltage swing. Circuitry and parameters are specified.

10.4.11 Turn-off time $t_{off} = t_{d(off)} + t_f$

Sum of:
the turn-off delay time $t_{d(off)}$ measured between the 90% value of the gate-source voltage and the 10% value of the drain-source voltage swing and the fall time t_f measured between the 10% value and the 90% value of the drain-source voltage swing. Circuitry and parameters are specified.

Definition of switching times.

10.5 Reverse diode characteristics

10.5.1 Continuous reverse drain current I_{DR}

Maximum permissible value of the dc forward current at specified mounting base temperature T_{mb} and ambient temperature T_A.

10.5.2 Pulsed reverse drain current I_{DRM}

Maximum permissible peak value of the reverse diode current for pulse operation. The duty cycle is the same as the one specified for the transistor.

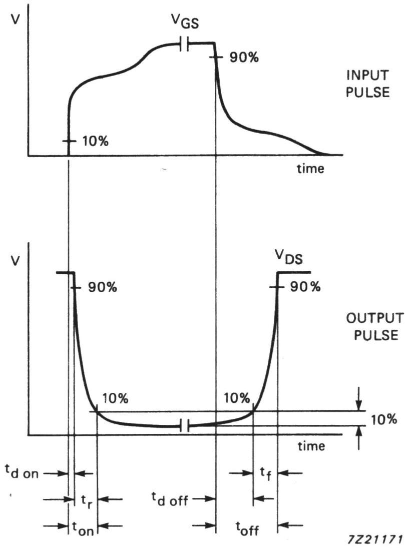
10.5.3 Diode forward on-voltage V_{SD}

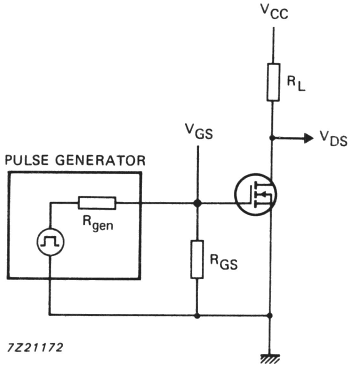
Diode forward voltage between source and drain in the on-state. The forward current I_F, the voltage V_{GS} and the chip temperature T_j are specified.

10.5.4 Reverse recovery time t_{rr} and reverse recovery charge Q_{rr}

Respectively stated is a typical value for the test and auxiliary conditions specified in the data sheet. For FREDFET*, maximum values have been specified.

* FREDFET = Fast-Recovery-Epitaxial-Diode-Field-Effect-Transistors with a fast switching reverse diode.



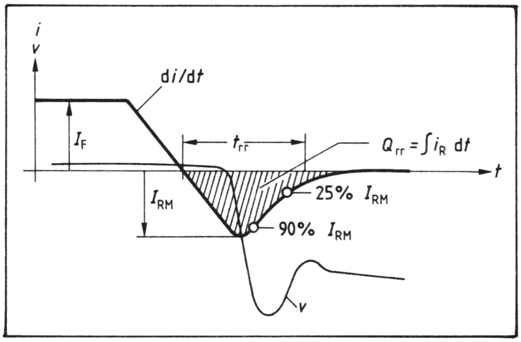


Test circuit for measuring the switching time.

t	Time axis
$t_{d(off)}$	Turn-off delay time
$t_{d(on)}$	Turn-on delay time
t_f	Fall time
t_{on}	Turn-on time
t_{off}	Turn-off time
t_r	Rise time
V	Voltage axis
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage

10.5.5 Repetitive peak reverse current I_{RRM}

The typical value for the repetitive peak reverse current of the reverse diode is specified in the data sheets for FREDFETs.



10.6 Diagrams

10.6.1 Power dissipation $P_D = f(T)$

The maximum permitted dissipated power is given versus ambient temperature (T_A) or mounting base temperature (T_{mb}).

10.6.2 Typical output characteristic $I_D = f(V_{DS})$

The typical dependence of the drain current I_D on the drain-source voltage V_{DS} is plotted at a specified gate-source voltage V_{GS}. Mounting base temperature and pulse width are also specified.

10.6.3 Safe operating area $I_D = f(V_{DS})$

The maximum permitted drain current I_D is shown versus drain-source voltage V_{DS} for loads of continuous dc current and pulses of various widths with the specified duty cycle. The maximum permitted mounting base temperature is specified. Within this area all values of I_D and V_{DS} are permitted, if the transistor is not thermally overloaded by these conditions. The $R_{DS(ON)}$ limit is only attainable with gate voltages ⩾ 10 V.

10.6.4 Typical transfer characteristic $I_D = f(V_{GS})$

The diagram shows the typical dependence of the drain-current I_D on the gate-source voltage V_{GS}, where the chip temperature T_j, the pulse width and the drain-source voltage V_{DS} are specified.

10.6.5 Typical on-state resistance $R_{DS(ON)} = f(I_D)$

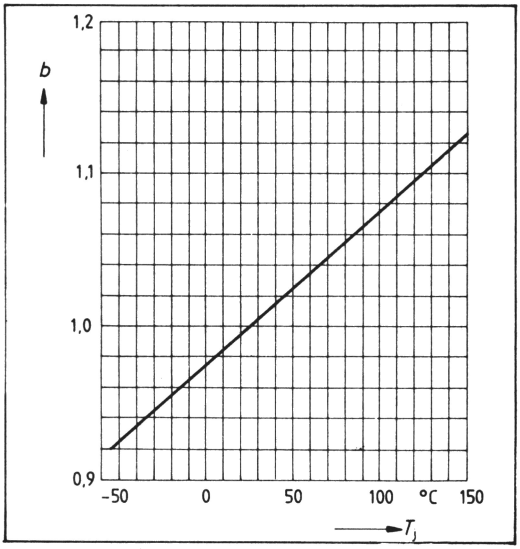
The typical on-state resistance $R_{DS(ON)}$ is plotted, versus the drain current I_D at $T_j = 25\,°C$ and at various gate-source voltages.

10.6.6 On-state resistance $R_{DS(ON)} = f(T_j)$

The on-state resistance is shown versus chip temperature over the permitted operating range.

10.6.7 Drain-source breakdown voltage $V_{(BR)DSS}$

A constant 'b' is given versus chip temperature over the permitted operating temperature range, where the following mathematical relationship applies: $V_{(BR)DSS}(T_j) = b \times V_{(BR)DSS}(25\,°C)$. The voltage $V_{(BR)DSS}(25\,°C)$ is the stated data sheet value.



10.6.8 The typical transconductance, $g_{fs} = f(I_D)$

The typical transconductance curve is shown versus drain current. The pulse width, the drain-source voltage V_{DS} and the chip temperature T_j are specified.

10.6.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$

The diagram shows the spread of gate threshold voltage $V_{GS(TO)}$ versus chip temperature T_j at the following conditions: $V_{DS} = V_{GS}$ and I_D.

10.6.10 Typical capacitances $C = f(V_{DS})$

The typical characteristics of the input capacitance C_{iss}, output capacitance C_{oss} and the reverse transfer capacitance C_{rss} are shown versus the drain-source voltage V_{DS} at a frequency f = 1 MHz and a gate-source voltage $V_{GS} = 0\,V$.

10.6.11 Drain current $I_D = f(T)$

The maximum permitted dc drain current is shown versus mounting base temperature T_{mb} with a fully turned-on transistor, i.e. $V_{GS} \geqslant 10\,V$.

10.6.12 Typical and maximum forward characteristics of the 'reverse diode' $I_F = f(V_{SD})$

The pulsed dc current of the reverse diode I_{DR} versus reverse diode forward voltage (V_{SD}) is shown. The pulse width and the chip temperature T_j are specified.

10.6.13 *Transient thermal resistance $Z_{th\,j\text{-}mb} = f(t)$*

The diagram shows the curve of transient thermal resistance $Z_{th\,j\text{-}mb}$ at the specified duty cycle $D = t_p/T$ versus the load time (pulse width).

10.6.14 *Typical gate-source voltage $V_{GS} = f(Q_{gate})$*

The diagram shows the typical characteristic of the required gate with the given gate-source and drain-source voltages in order to switch on the corresponding PowerMOS transistor to the specified current. The gate charge comprises the charge Q_{GS} that is required to charge up the gate-source capacitance C_{GS}. During this phase – after the gate threshold voltage $V_{GS(TO)}$ has been reached – the drain current increases to its specified value and the drain-source voltage then decreases. However, until this voltage V_{DS} has decreased to its residual level, the gate-drain capacitance (Miller capacitance) must be discharged. This charge portion is defined as gate-drain charge Q_{GD}. The charge $Q_G = Q_{GS} + Q_{GD}$ is not enough to switch the transistor fully on, because the residual voltage and the drain-source on-state resistance have not yet reached a minimum. It is only with a charge corresponding to a gate-source voltage V_{GS} of 10 V that the on-state resistance and hence the static losses are optimized. This total charge $Q_{G(tot)}$ is dependent on the drain-source voltage to be switched; the level of the drain-current to be switched has only a small influence on the total charge required.
The diagram was produced for measurements according to the test circuit shown in para 10.7.8 with constant current, e.g. 1,5 mA. This gives the user the possibility, according to $Q = i \times t$, of setting the charging current or the on-time as required, or of correspondingly dimensioning the drive circuit.

Example

A 100 kHz switched-mode power supply is to be switched by a BUZ71A:

Given:

Voltage V_{DS} = 40 V
On-time t_{on} = 100 ns
Frequency f = 100 kHz
Current I_{DM} = 18 A
Drive voltage V_{GS} = 10 V

Required:

Drive current I_{drive}
Drive power P_{drive}

1st calculation:

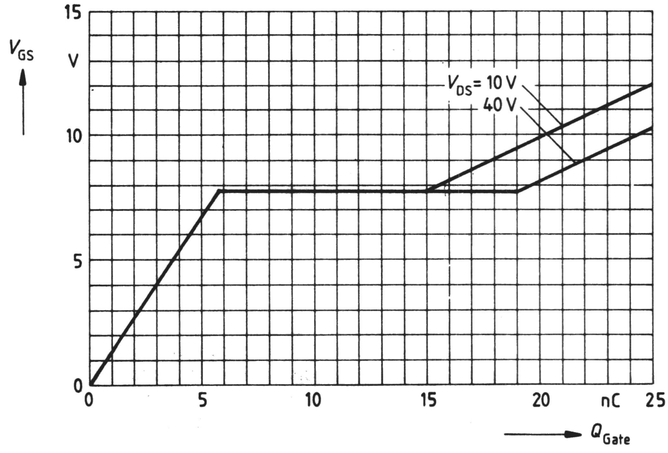
$Q_{tot} = 24{,}5\ \text{nC}$

$$I_{drive} = \frac{24{,}5\ \text{nC}}{100\ \text{ns}} = 245\ \text{mA}$$ 1)

For the turn-on process the average drive power is:

2nd calculation

$$P_{drive} = Q_{Gtot} \times V_{GS} \times f = 24{,}5\ \text{nC} \times 10\ \text{V} \times 100\ \text{kHz} = 245\ \text{mW}$$



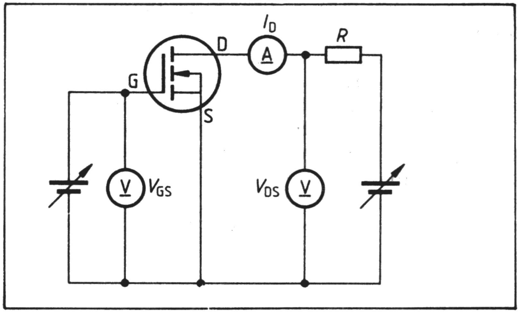
Typical gate charge in the BUZ71A example; parameter I_{DM} = 18 A.

1) The drive power must be designed for this.

10.7 Test circuits (according to IEC 147-2G and DIN 41792, sheet 6).

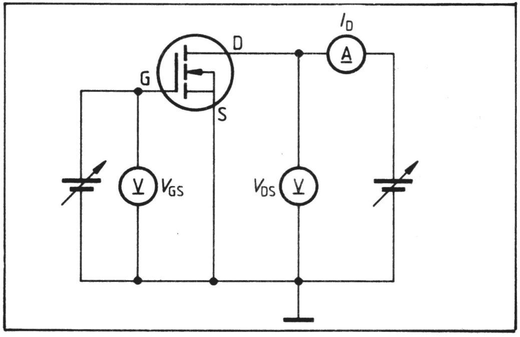
The temperature values for the specified parameters, stated in the data sheets, are to be adhered to during the respective measurements.

10.7.1 Drain current I_D, I_{DSS}



Basic circuit diagram for measurement of the drain current I_D and the zero gate voltage drain current I_{DSS}.
R serves as protective resistor. The specified gate-source voltage V_{GS} is set. If V_{GS} is specified to be 0 V, gate and source must be short-circuited.

10.7.2 Drain-source on-state resistance $R_{DS(ON)}$

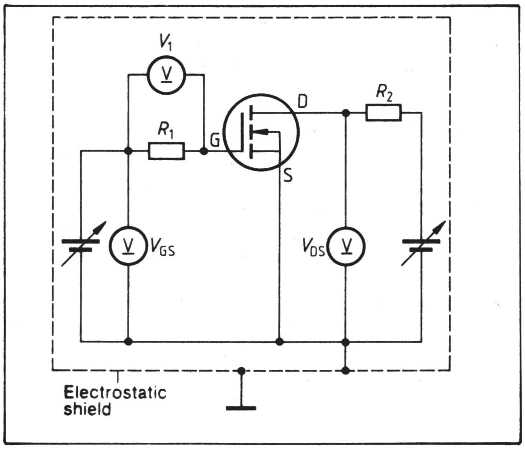


Schematic circuit diagram to measure the drain-source on-state resistance $R_{DS(ON)}$.
Generally, the drain-source on-state resistance $R_{DS(ON)}$ is measured in the ohmic or linear regions. The internal resistance of the voltmeter V_{DS} must be considerably higher than the on-resistance $R_{DS(ON)}$.

10.7.3 Gate threshold voltage $V_{GS(TO)}$

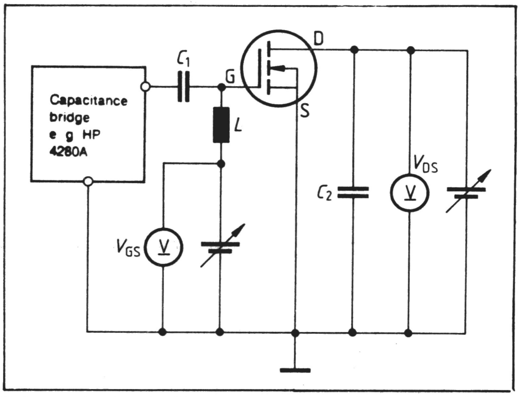
(See basic circuit diagram for measuring the drain current I_D). The gate-source voltage, equal in value to the drain-source voltage V_{DS}, is increased slowly from zero until the specified drain current I_D is reached.

10.7.4 Gate-source leakage current I_{GSS}



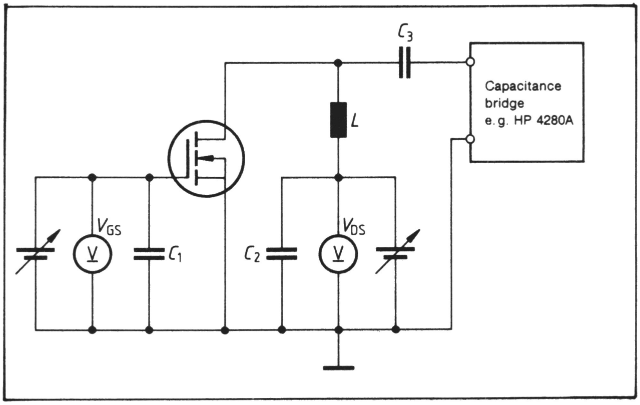
Schematic circuit diagram to measure the gate-source leakage current I_{GSS}. R_1 and R_2 serve as protective resistors. The value of R_1 should be lower than $V_{GS}/100I_{GSS}$. V_1 is a very sensitive voltmeter with an internal resistance of at least 100 times the value of R_1. The leakage current is given by $I_{GSS} = V_1/R_1$. The circuit must be electrostatically shielded. Care must be taken that measurement is not falsified by leakage currents that may be caused by the circuit layout.

10.7.5 Input capacitance C_{iss}



Schematic circuit diagram to measure input capacitance C_{iss} using a bridge without dc passage. The capacitors C_1 and C_2 must form a short circuit at the measuring frequency. The inductor L decouples the dc supply.

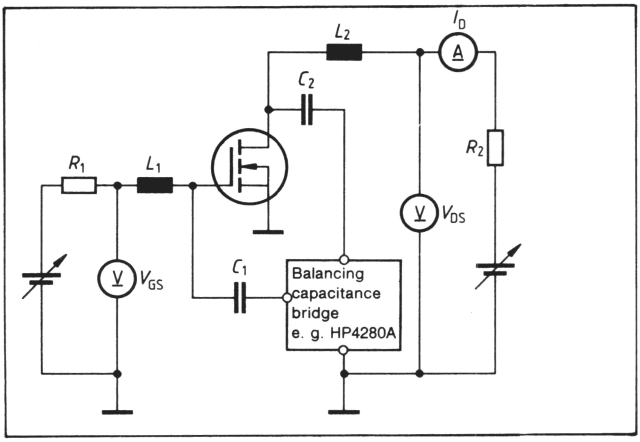
10.7.6 *Output capacitance C_{oss}*



C3
Capacitance bridge e.g. HP 4280A
L
VGS
V
C1
C2
VDS
V

Schematic circuit diagram to measure the output capacitance C_{oss} when using a bridge without dc passage. The capacitors C_1, C_2 and C_3 must form a short circuit at the measuring frequency. The inductor L decouples the dc supply.

10.7.7 *Reverse transfer capacitance C_{rss}*

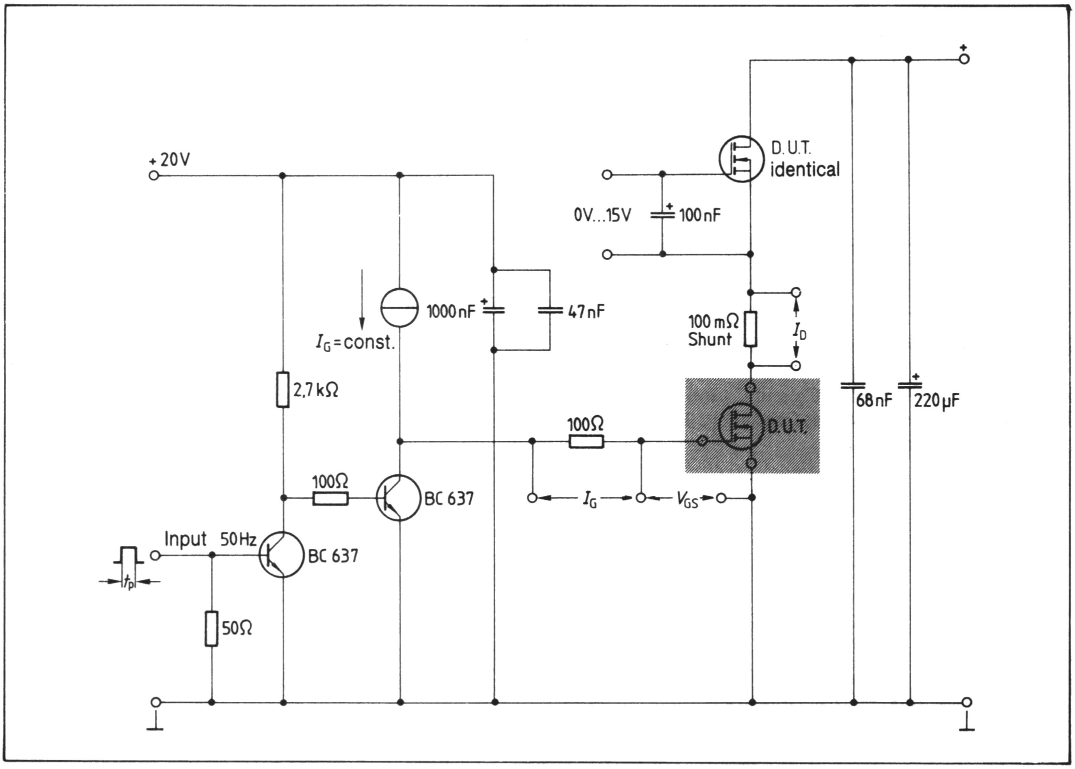


L2
ID
A
C2
R2
R1
L1
V
VDS
C1
V
VGS
Balancing capacitance bridge e. g. HP4280A

Schematic circuit diagram to measure the reverse transfer capacitance C_{rss} when using a bridge without dc passage. The capacitors C_1 and C_2 must form a short circuit at the measuring frequency. The inductors L_1 and L_2 decouple the dc supply.

10.7.8 Gate charge Q_{gate}

Basic circuit diagram for measurement of the gate charge.


+20V
I_G=const.
1000nF
47nF
2,7kΩ
100Ω
BC 637
Input 50Hz
t_p
BC 637
50Ω
0V...15V
100nF
D.U.T.
identical
100 mΩ
Shunt
I_D
100Ω
D.U.T.
I_G
V_{GS}
68nF
220µF
+

11 SOLDERING INSTRUCTIONS

Every semiconductor is extremely sensitive to the exceeding of its maximum permissible chip temperature. When soldering semiconductors, care must be taken that the components will not be thermally overloaded. The chip temperature may not exceed 200 °C during soldering (max. 1 minute). The leads must not be subject to high mechanical stress during soldering. The requirements of the solderability tests according to DIN IEC 68-2-20 are satisfied.

11.1 Soldering data for the metal case TO-3

Soldering temperature	Lead length 2 mm	Lead length 5 mm
245 °C	15 s	20 s
260 °C	12 s	15 s
300 °C*	10 s	15 s

11.2 Soldering data for the plastic packages TO218, TO220

Soldering temperature	Lead length 1,6 mm	Lead length 5 mm
245 °C	7 s	10 s
260 °C	7 s	7 s
300 °C*	4 s	7 s

* The values apply to iron soldering. The lead length is measured form the soldering point.

12 TYPE DESIGNATION

12.1 Pro Electron type designation code for semiconductor devices

This type designation code applies to discrete semiconductor devices – as opposed to integrated circuits –, multiples of such devices and semiconductor chips.

'Although not all type numbers accord with the Pro Electron system, the following explanation is given for the ones that do'.

A basic type number consists of:
TWO LETTERS FOLLOWED BY A SERIAL NUMBER

12.1.1 First letter

The first letter gives information about the material used for the active part of the devices.

A. GERMANIUM or other material with band gap of 0,6 to 1,0 eV
B. SILICON or other material with band gap of 1,0 to 1,3 eV
C. GALLIUM-ARSENIDE or other material with band gap of 1,3 eV or more
R. COMPOUND MATERIALS (e.g. Cadmium-sulphide)

12.1.2 Second letter

The second letter indicates the function for which the device is primarily designed.

A. DIODE; signal, low power
B. DIODE; variable capacitance
C. TRANSISTOR; low power, audio frequency ($R_{th\,j\text{-}mb} > 15$ K/W)
D. TRANSISTOR; power, audio frequency ($R_{th\,j\text{-}mb} \leqslant 15$ K/W)
E. DIODE; tunnel
F. TRANSISTOR; low power, high frequency ($R_{th\,j\text{-}mb} > 15$ K/W)
G. MULTIPLE OR DISSIMILAR DEVICES – MISCELLANEOUS; e.g. oscillator
H. DIODE; magnetic sensitive
L. TRANSISTOR; power, high frequency ($R_{th\,j\text{-}mb} \leqslant 15$ K/W)
N. PHOTO-COUPLER
P. RADIATION DETECTOR; e.g. high sensitivity phototransistor
Q. RADIATION GENERATOR; e.g. light-emitting diode (LED)
R. CONTROL AND SWITCHING DEVICE; e.g. thyristor, low power ($R_{th\,j\text{-}mb} > 15$ K/W)
S. TRANSISTOR; low power, switching ($R_{th\,j\text{-}mb} > 15$ K/W)
T. CONTROL AND SWITCHING DEVICE; e.g. thyristor, power ($R_{th\,j\text{-}mb} \leqslant 15$ K/W)
U. TRANSISTOR; power, switching ($R_{th\,j\text{-}mb} \leqslant 15$ K/W)
X. DIODE; multiplier, e.g. varactor, step recovery
Y. DIODE; rectifying, booster
Z. DIODE; voltage reference or regulator (transient suppressor diode, with third letter W)

The remainder of the type number is a serial number indicating a particular design or development and is one of the following two groups:

(a) A serial number consisting of three figures from 100 to 999.
(b) A serial number consisting of one letter (Z, Y, X, W, etc) followed by two figures.

12.1.3 Range numbers

Where there is a range of variants of a basic type of rectifier diode, thyristor or voltage regulator diode the type number as defined above is often used to identify the range; further letters and figures are added after a hyphen to identify associated types within the range. These additions are as follows:

RECTIFIER DIODES, THYRISTORS AND TRIACS

A group of figures indicating the rated repetitive peak reverse voltage, V_{RRM}, or the rated repetitive peak off-state voltage, V_{DRM}, whichever value is lower, in volts for each type.

The final letter R is used to denote a reverse polarity version (stud-anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

REGULATOR DIODES

A first letter indicating the nominal percentage tolerance in the operating voltage V_Z.

A. 1% (according to IEC 63: series E96)
B. 2% (according to IEC 63: series E48)
C. 5% (according to IEC 63: series E24)
D. 10% (according to IEC 63: series E12)
E. 20% (according to IEC 63: series E6)

A group of figures indicating the typical operating voltage V_Z for each type at the nominal operating current I_Z rating of the range.

The letter V is used to denote a decimal sign.

The final letter R is used to denote a reverse polarity version (stud anode) where applicable. The normal polarity version (stud cathode) has no special final letter.

Examples:

BYX38-600	Silicon rectifier in the BYX38 range with 600 V maximum repetitive peak voltage, normal polarity, stud connected to cathode.
BZY91-C7V5	Silicon voltage regulator diode in the BZY91 range with 7,5 V operating ±5% tolerance, normal polarity, stud connected to cathode.

13 RATING SYSTEMS

The rating systems described are those recommended by the International Electrotechnical Commission (IEC) in its Publication 134.

13.1 Definitions of terms used

Electronic device. An electronic tube or valve, transistor or other semiconductor device.

Note
This definition excludes inductors, capacitors, resistors and similar components.

Characteristic. A characteristic is an inherent and measurable property of a device. Such a property may be electrical, mechanical, thermal, hydraulic, electro-magnetic, or nuclear, and can be expressed as a value for stated or recognized conditions. A characteristic may also be a set of related values, usually shown in graphical form.

Bogey electronic device. An electronic device whose characteristics have the published nominal values for the type. A bogey electronic device for any particular application can be obtained by considering only those characteristics which are directly related to the application.

Rating. A value which establishes either a limiting capability or a limiting condition for an electronic device. It is determined for specified values of environment and operation, and may be stated in any suitable terms.

Note
Limiting conditions may be either maxima or minima.

Rating system. The set of principles upon which ratings are established and which determine their interpretation.

Note
The rating system indicates the division of responsibility between the device manufacturer and the circuit designer, with the object of ensuring that the working conditions do not exceed the ratings.

13.2 Absolute maximum rating system

Absolute maximum ratings are limiting values of operating and environmental conditions applicable to any electronic device of a specified type as defined by its published data, which should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking no responsibility for equipment variations, environmental variations, and the effects of changes in operating conditions due to variations in the characteristics of the device under consideration and of all other electronic devices in the equipment.

The equipment manufacturer should design so that, initially and throughout life, no absolute maximum value for the intended service is exceeded with any device under the worst probable operating conditions with respect to supply voltage variation, equipment component variation, equipment control adjustment, load variations, signal variation, environmental conditions, and variations in characteristics of the device under consideration and of all other electronic devices in the equipment.

13.3 Design maximum rating system

Design maximum ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under the worst probable conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device, taking responsibility for the effects of changes in operating conditions due to variations in the characteristics of the electronic device under consideration.

The equipment manufacturer should design so that, initially and throughout life, no design maximum value for the intended service is exceeded with a bogey device under the worst probable operating conditions with respect to supply voltage variation, variation in characteristics of all other devices in the equipment, equipment control adjustment, load variation, signal variation and environmental conditions.

13.4 Design centre rating system

Design centre ratings are limiting values of operating and environmental conditions applicable to a bogey electronic device of a specified type as defined by its published data, and should not be exceeded under normal conditions.

These values are chosen by the device manufacturer to provide acceptable serviceability of the device in average applications, taking responsibility for normal changes in operating conditions due to rated supply voltage variation, equipment component variation, equipment control adjustment, load variation, signal variation, environmental conditions, and variations in the characteristics of all electronic devices. The equipment manufacturer should design so that, initially, no design centre value for the intended service is exceeded with a bogey electronic device in equipment operating at the state normal supply voltage.

14 LETTER SYMBOLS

Letter symbols for currents, voltages and powers

Basic letters: – The basic letters to be used are:
I, i = current; V, v = voltage;
P, p = power

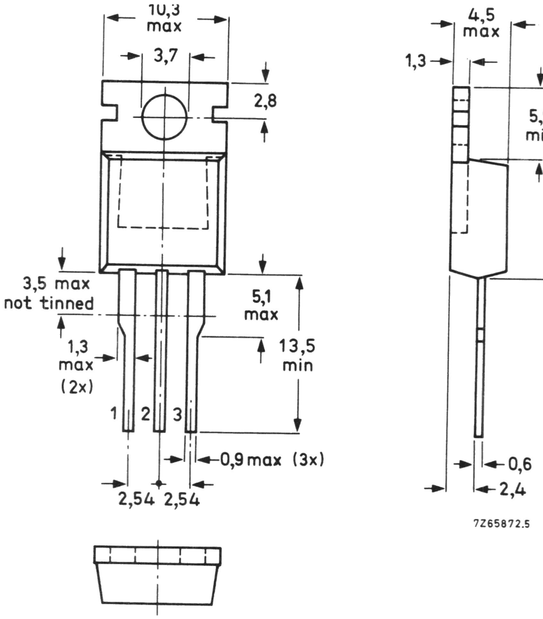
Lower-case basic letters shall be used for the representation of instantaneous values which vary with time. In all other instances uppercase letters shall be used.

Subscripts

amb	Ambient
(AV), (av)	Average value
(BO)	Breakover
(BR)	Breakdown
case	Case
C	Controllable
D, d	Forward off-state*, non-triggered (gate voltage or current)
F, f	Forward*, fall
G, g	Gate terminal
H	Holding
I, i	Input
J, j	Junction
L	Latching
M, m	Peak or crest value
min	Minimum
O, o	Output, open circuit
(OV)	Overload
P, p	Pulse
Q, q	Turn-off
R, r	As first subscript: reverse, rise As second subscript: repetitive, recovery
(RMS), (rms)	R.M.S. value
S, s	As first subscript: storage, stray, series, source switching As second subscript: non-repetitive
stg	Storage
T, t	Forward on-state*, triggered (gate voltage or current)
th	Thermal
(TO)	Threshold
tot	Total
W	Working
Z	Reference or regulator (i.e. zener)

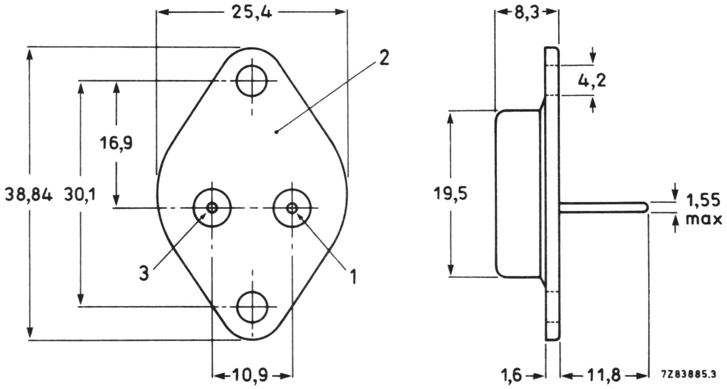
POWERMOS SELECTION GUIDE

PowerMOS Selection Guide


10,3
max
3,7
2,8
3,5 max
not tinned
5,1
max
1,3
max
(2x)
13,5
min
1
2
3
0,9 max (3x)
2,54
2,54
4,5
max
1,3
5,9
min
15,8
max
0,6
2,4
7Z65872.5

In plastic package TO220AB

TYPE	$V_{DS(max)}$ V	$I_{D(max)}$ A	$R_{DS(ON)(max)}$ Ω	$P_{D(max)}$ W	PAGE
N-channel enhancement types					
BUZ10	50	23	0,07	75	67
BUZ11	50	30	0,04	75	74
BUZ11A	50	26	0,055	75	81
BUZ71	50	14	0,1	40	88
BUZ71A	50	13	0,12	40	95
BUZ20	100	12	0,2	75	102
BUZ21	100	21	0,085	75	109
BUZ72	100	10	0,2	40	116
BUZ72A	100	9,0	0,25	40	123
BUZ31	200	13	0,2	75	130
BUZ32	200	9,5	0,4	75	137
BUZ73	200	7,0	0,4	40	144
BUZ73A	200	5,8	0,6	40	151
BUZ60	400	5,5	1,0	75	158
BUZ76	400	3,0	1,8	40	165
BUZ76A	400	2,6	2,5	40	172
BUZ41A	500	4,5	1,5	75	179
BUZ42	500	4,0	2,0	75	186
BUZ74	500	2,4	3,0	40	193
BUZ74A	500	2,0	4,0	40	200
BUZ90	600	4,0	2,0	75	207
BUZ90A	600	3,5	2,5	75	214
BUZ78	800	1,5	8,0	40	221
BUZ80	800	2,6	4,0	75	228
BUZ80A	800	3,0	3,0	75	235
BUZ50A	1000	2,5	5,0	75	242
BUZ50B	1000	2,0	8,0	75	249
BUZ50C	1000	2,3	6,0	75	256

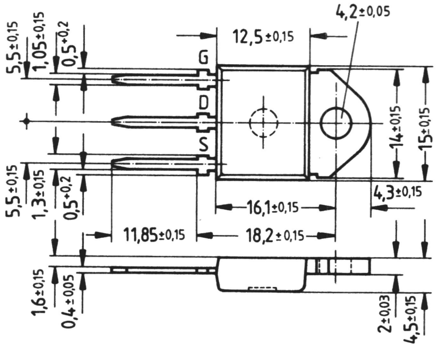


In metal case TO-3

TYPE	$V_{DS(max)}$ V	$I_{D(max)}$ A	$R_{DS(ON)(max)}$ Ω	$P_{D(max)}$ W	PAGE
N-channel enhancement types					
BUZ14	50	39	0,04	125	263
BUZ15	50	45	0,03	125	270
BUZ23	100	10	0,2	78	277
BUZ24	100	32	0,06	125	284
BUZ25	100	21	0,085	78	291
BUZ34	200	14	0,2	78	298
BUZ35	200	9,9	0,4	78	305
BUZ36	200	22	0,12	125	312
BUZ63	400	5,9	1,0	78	319
BUZ64	400	11,5	0,4	125	326
BUZ45	500	9,6	0,6	125	333
BUZ45A	500	8,3	0,8	125	340
BUZ45B	500	10	0,5	125	347
BUZ211*	500	9,0	0,8	125	354
BUZ94	600	7,8	0,9	125	361
BUZ83	800	2,9	4,0	78	368
BUZ83A	800	3,4	3,0	78	375
BUZ84	800	5,3	2,0	125	382
BUZ84A	800	6,0	1,5	125	389
BUZ53A	1000	2,6	5,0	78	396
BUZ54	1000	5,3	2,0	125	403
BUZ54A	1000	4,6	2,6	125	410

* FREDFET, power transistor with fast-recovery reverse diode.

PowerMOS Selection Guide


4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

In plastic package TO218AA

TYPE	$V_{DS(max)}$ V	$I_{D(max)}$ A	$R_{DS(ON)(max)}$ Ω	$P_{D(max)}$ W	PAGE
N-channel enhancement types					
BUZ347	50	42	0,03	125	417
BUZ348	50	39	0,04	125	424
BUZ349	100	32	0,06	125	431
BUZ350	200	22	0,12	125	438
BUZ326	400	9,5	0,5	100	445
BUZ351	400	11,5	0,4	125	452
BUZ330	500	9,5	0,6	125	459
BUZ331	500	8,0	0,8	125	466
BUZ384	500	10,5	0,6	125	473
BUZ385	500	9,0	0,8	125	480
BUZ307	800	3,0	3,0	75	487
BUZ308	800	2,6	4,0	75	494
BUZ355	800	6,0	1,5	125	501
BUZ356	800	5,0	2,0	125	508
BUZ310	1000	2,5	5,0	75	515
BUZ311	1000	2,3	6,0	75	522
BUZ357	1000	5,0	2,0	125	529
BUZ358	1000	4,5	2,6	125	536

POWERMOS DEVICE DATA

PowerMOS transistor BUZ10

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

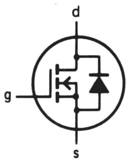
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	23	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,07	Ω

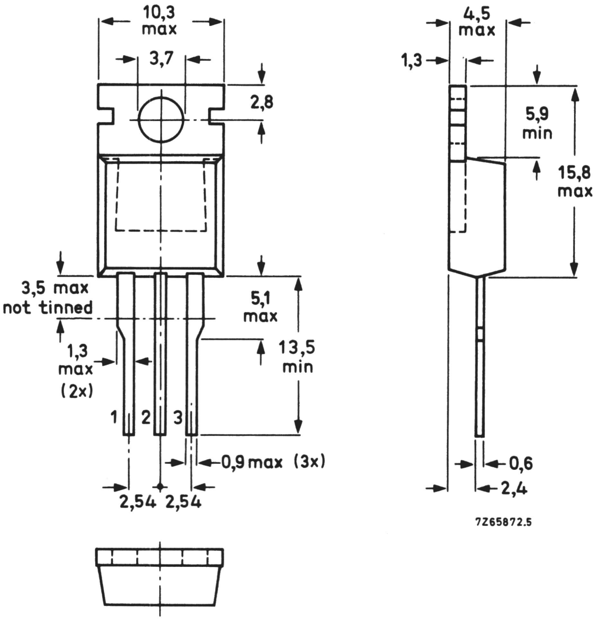
MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source





10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	23	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	14,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	92	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 15 A	–	0,06	0,07	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 15 A	8,0	13,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	940	1250	pF
C_{oss}	Output capacitance		–	500	750	pF
C_{rss}	Feedback capacitance		–	180	270	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	60	90	ns
$t_{d\ off}$	Turn-off delay time		–	100	130	ns
t_f	Turn-off fall time		–	75	95	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	23	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	92	A
V_{SD}	Diode forward on-voltage	I_F = 46 A; V_{GS} = 0 V	–	1,5	2,0	V
t_{rr}	Reverse recovery time	I_F = 23 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	150	–	ns
Q_{rr}	Reverse recovery charge		–	1,0	–	μC

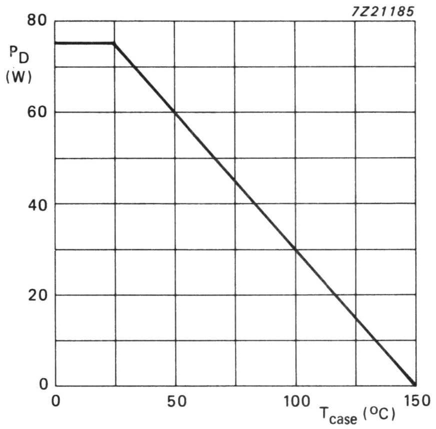


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

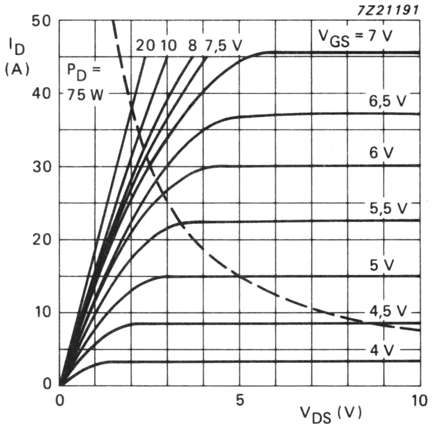


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

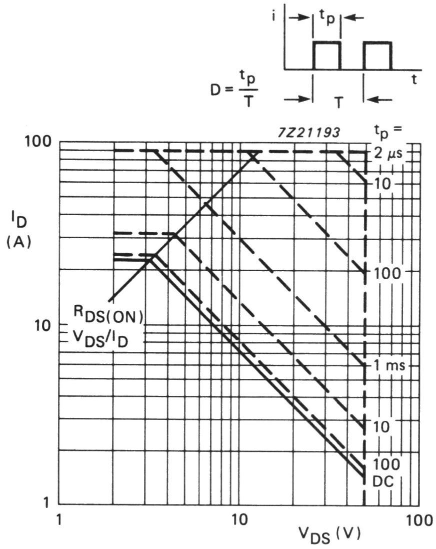


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

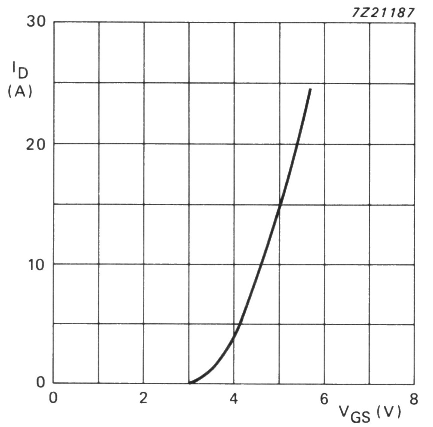


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

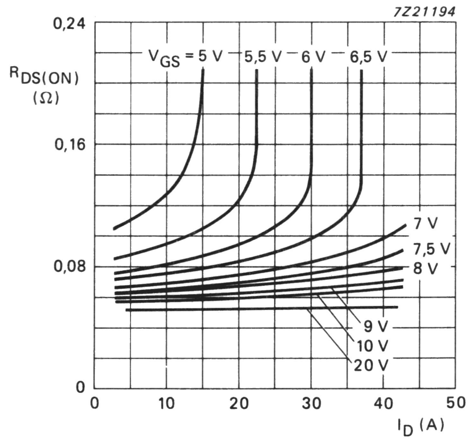


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

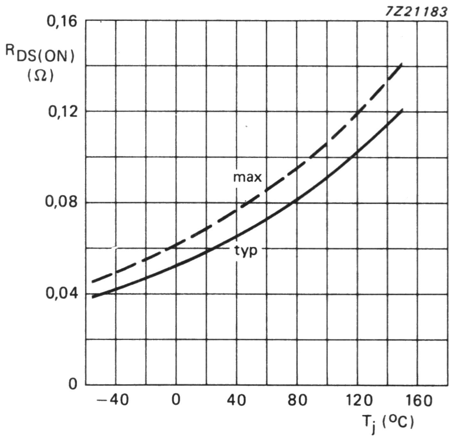


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 15 A; V_{GS} = 10 V.

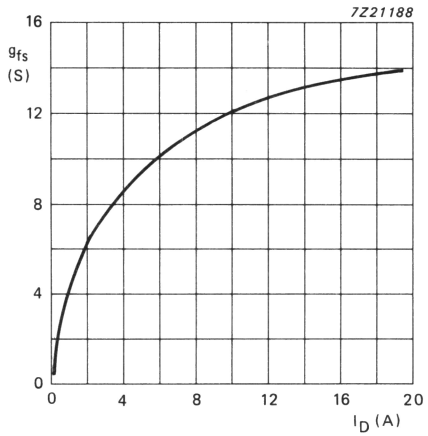


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

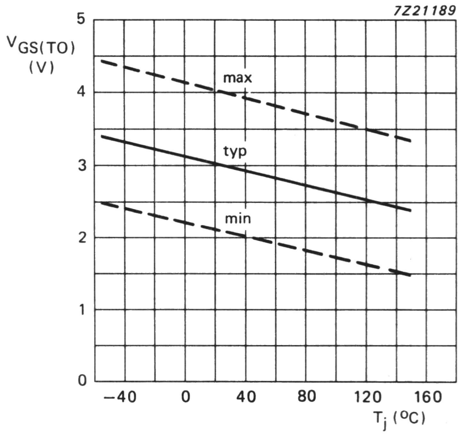


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 10 mA.

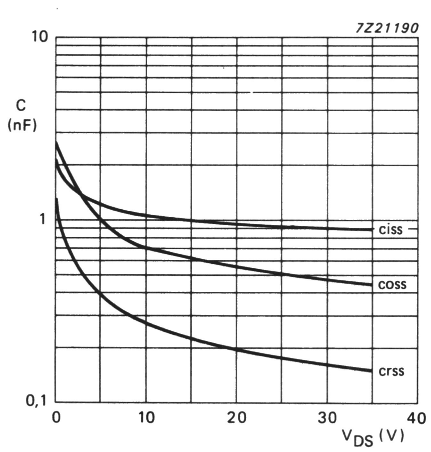


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

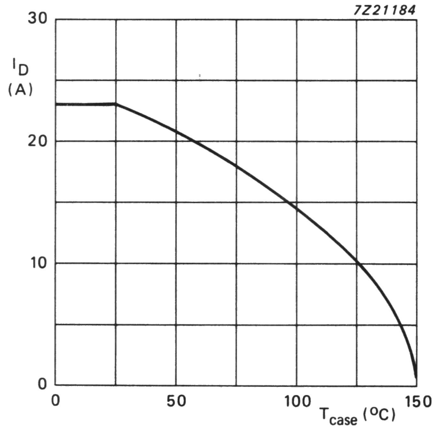


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

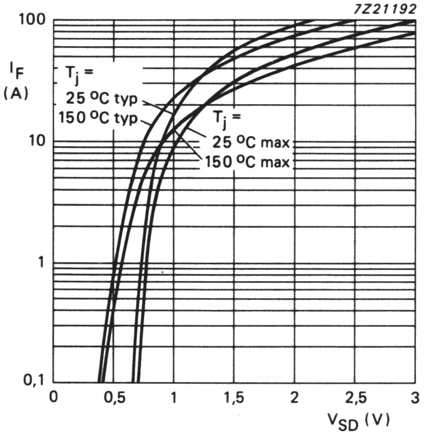


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

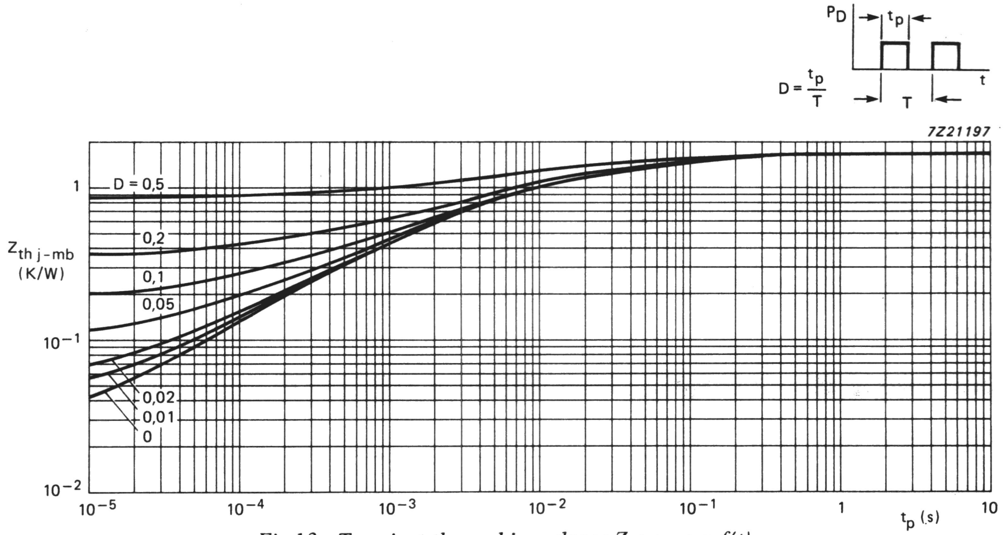


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

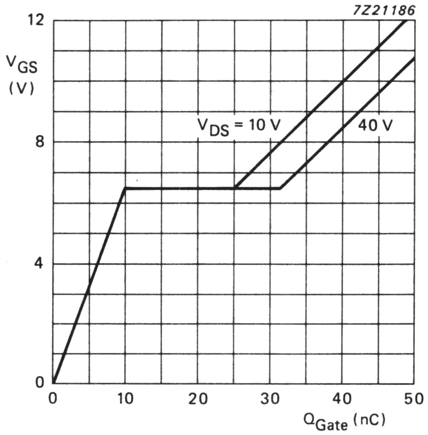


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 45$ A.

PowerMOS transistor BUZ11

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

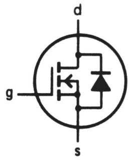
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	30	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,04	Ω

MECHANICAL DATA

Dimensions in mm

Pinning:
1 = Gate
2 = Drain
3 = Source



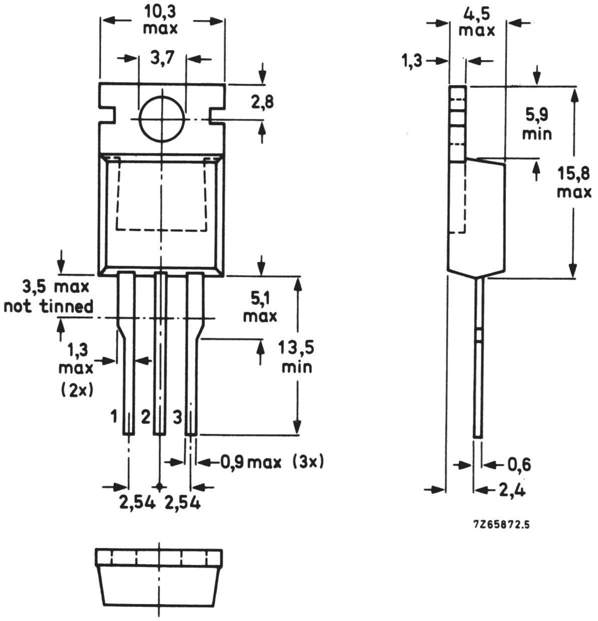

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20$ kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 30$ °C	–	30	A
I_D	Drain current (d.c.)	$T_{mb} = 100$ °C	–	19,4	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25$ °C	–	120	A
P_{tot}	Total power dissipation	$T_{mb} = 25$ °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb} = 1{,}67$ K/W
From junction to ambient	$R_{th\,j\text{-}a} = 75$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0{,}25$ mA	50	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 50$ V; $V_{GS} = 0$ V; $T_j = 25$ °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 50$ V; $V_{GS} = 0$ V; $T_j = 125$ °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 15$ A	–	0,03	0,04	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25$ °C unless other wise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 15$ A	8,0	13,5	–	S
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	750	1100	pF
C_{rss}	Feedback capacitance		–	250	400	pF
$t_{d\,on}$	Turn-on delay time	$V_{DD} = 30$ V; $I_D = 3$ A; $V_{GS} = 10$ V; $R_{GS} = 50$ Ω $R_{gen} = 50$ Ω	–	30	45	ns
t_r	Turn-on rise time		–	70	110	ns
$t_{d\,off}$	Turn-off delay time		–	180	230	ns
t_f	Turn-off fall time		–	130	170	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse train current	T_{mb} = 25 °C	–	–	30	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	120	A
V_{SD}	Diode forward on-voltage	I_F = 60 A; V_{GS} = 0 V		1,7	2,6	V
t_{rr}	Reverse recovery time	I_F = 30 A;	–	200	–	ns
		$-dI_F/dt$ = 100 A/µs;				
		V_{GS} = 0 V. V_R = 30 V	–	0,25	–	µC

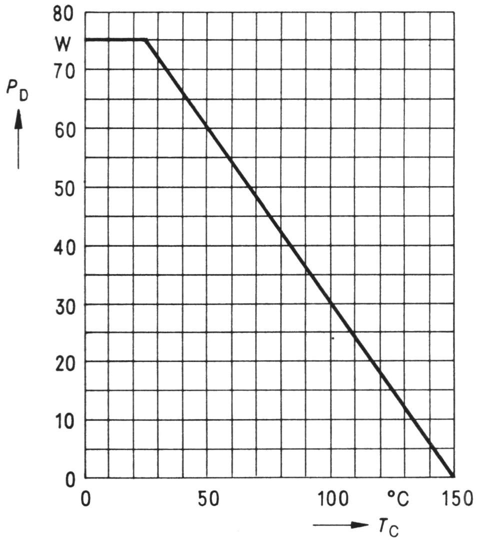


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

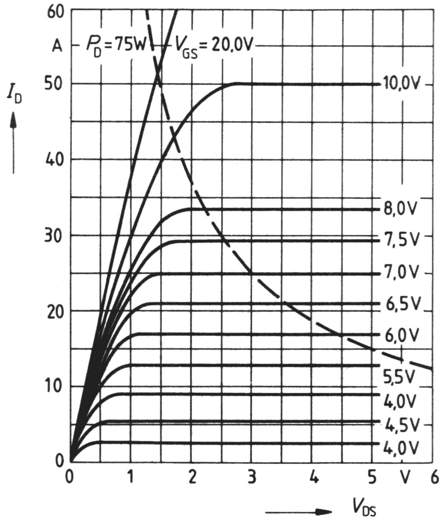


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{DS}; 80 µs pulse test:
$T_{mb} = 25\,°C$.

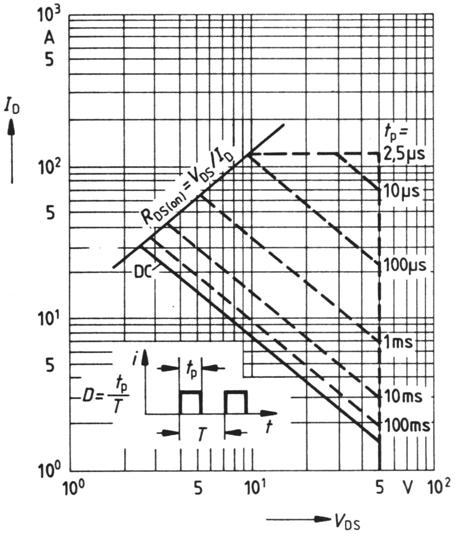


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$.
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\,°C$.

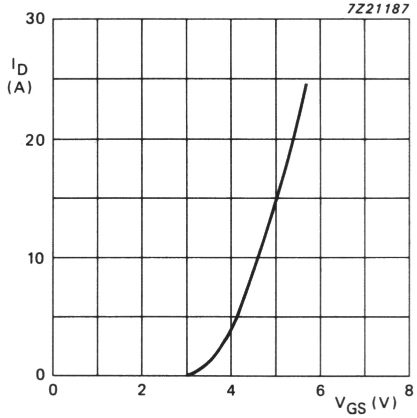


Fig.5 *Typical transfer charactetistic $I_D = f(V_{GS})$.*
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V, $T_{mb} = 25\,°C$.

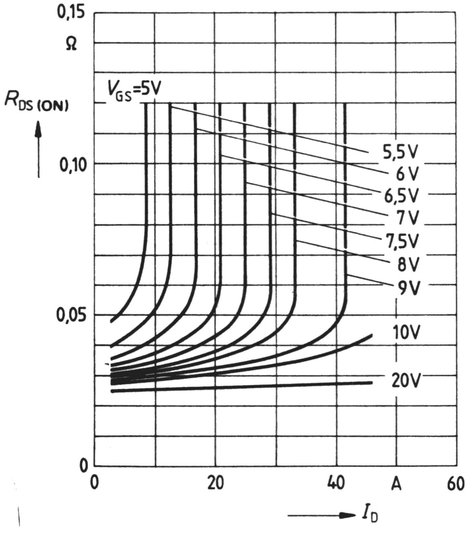


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

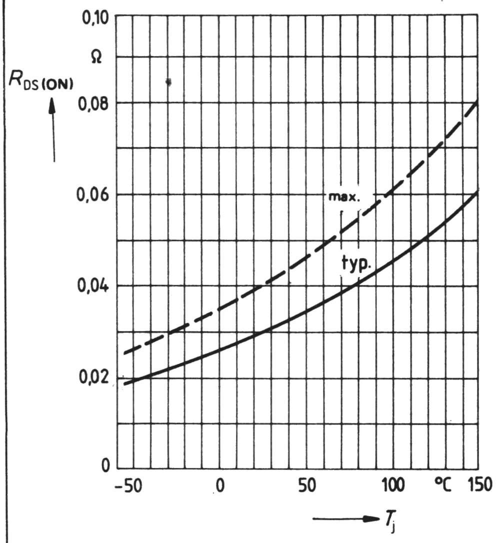


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 15\,A$; $V_{GS} = 10\,V$.

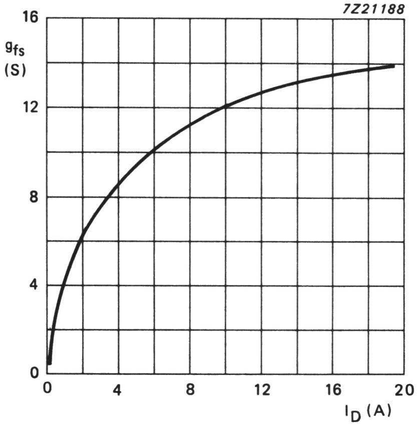


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\,V$; $T_j = 25\,°C$.

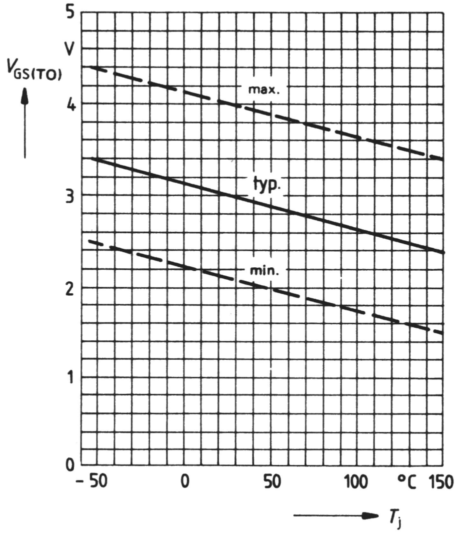


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

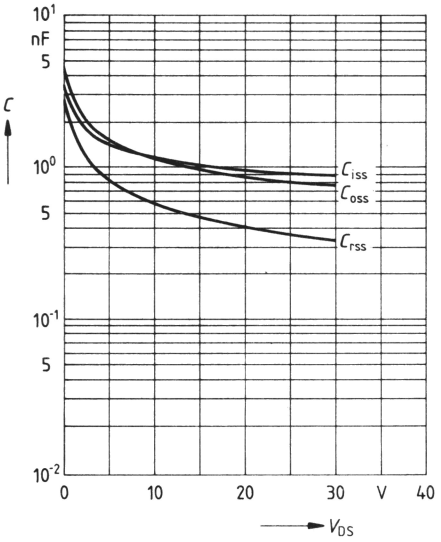


Fig.10 *Typical capacitance $c = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

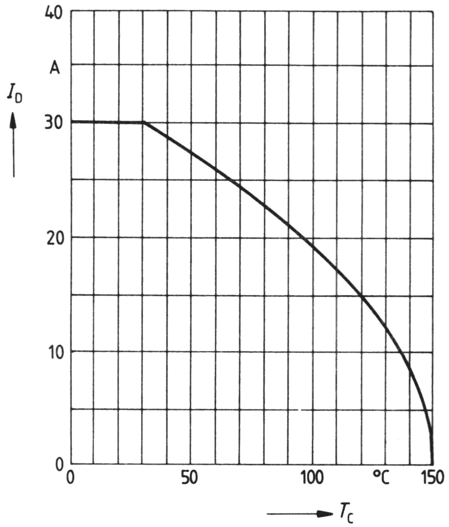


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

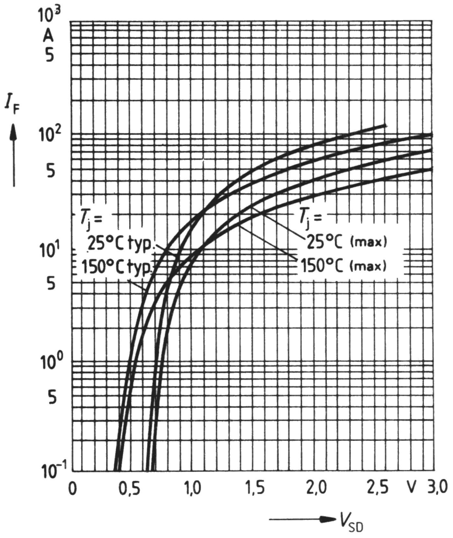


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

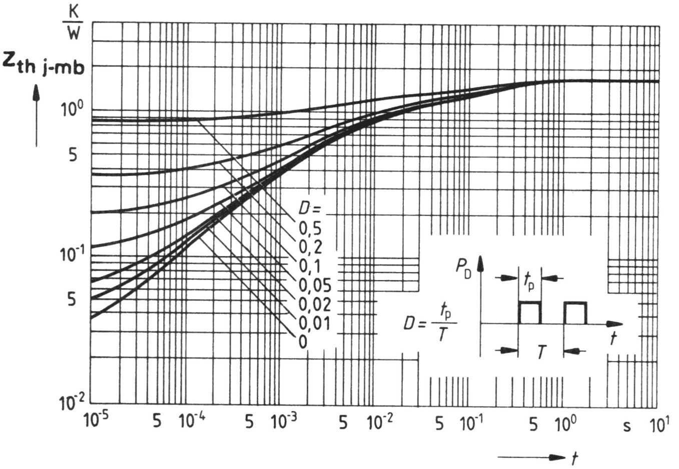


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

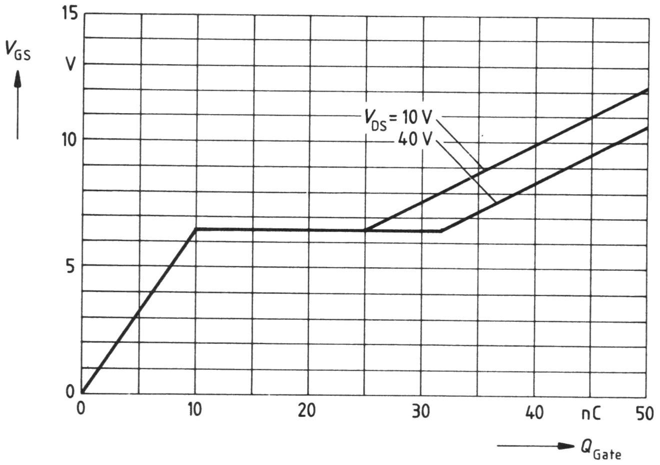


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 45$ *A.*

PowerMOS transistor BUZ11A

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

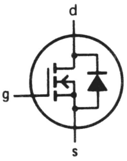
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	26	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,055	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



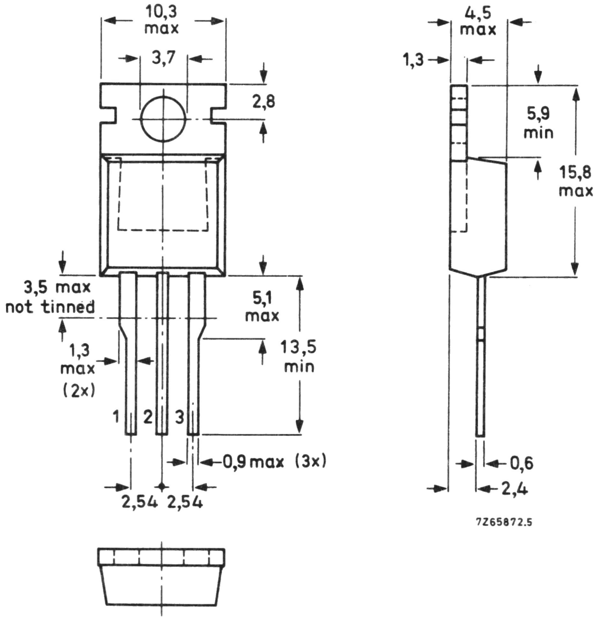

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	26	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	16,4	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	104	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 16 A	–	0,048	0,055	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 16 A	8,0	13,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1000	1300	pF
C_{oss}	Output capacitance		–	500	800	pF
C_{rss}	Feedback capacitance		–	200	300	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	60	90	ns
$t_{d\ off}$	Turn-off delay time		–	125	160	ns
t_f	Turn-off fall time		–	100	130	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	26	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	104	A
V_{SD}	Diode forward on-voltage	I_F = 52 A; V_{GS} = 0 V	–	1,5	2,0	V
t_{rr}	Reverse recovery time	I_F = 26 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	100	–	ns
Q_{rr}	Reverse recovery charge		–	0,2	–	μC

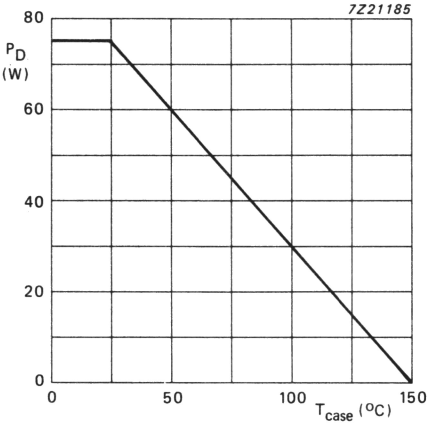


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

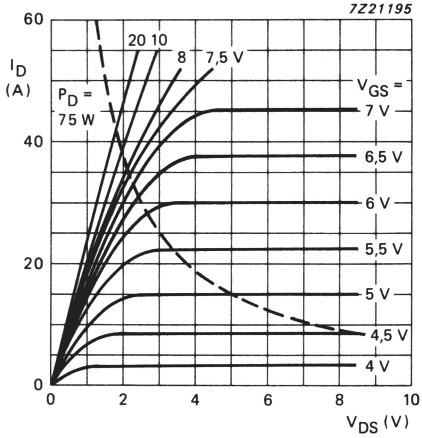


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

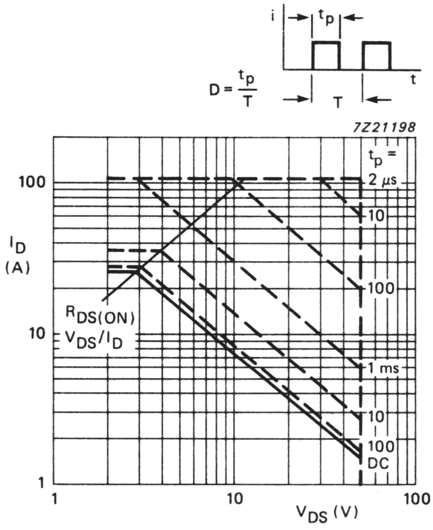


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

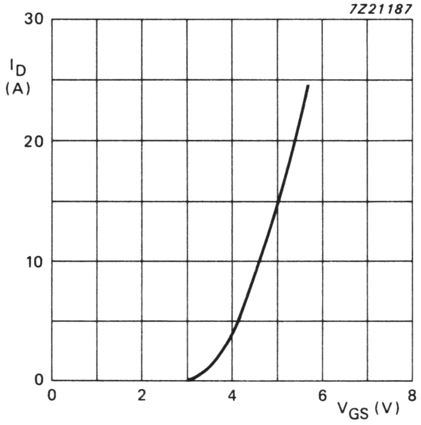


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

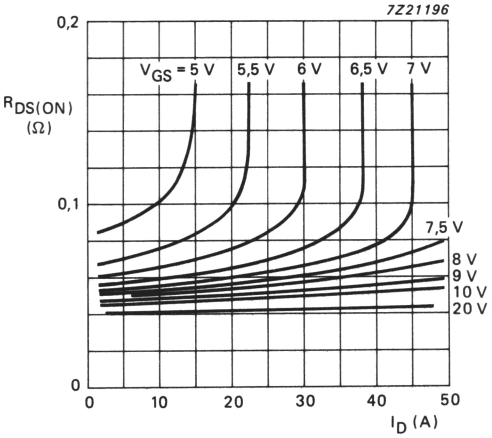


Fig.6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\ °C$.

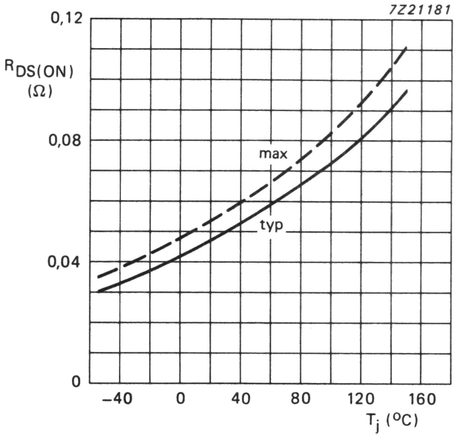


Fig.7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 16\ A$; $V_{GS} = 10\ V$.

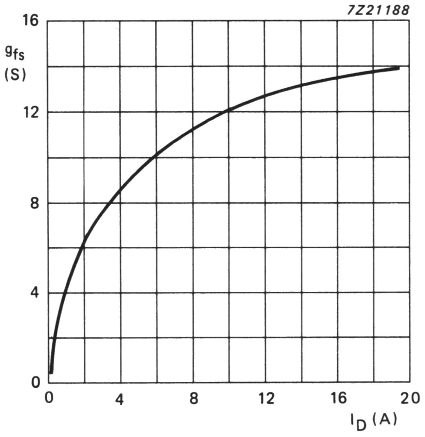


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\ °C$.

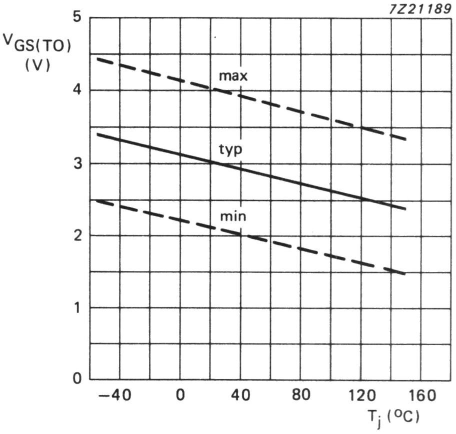


Fig.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 10\ mA$.

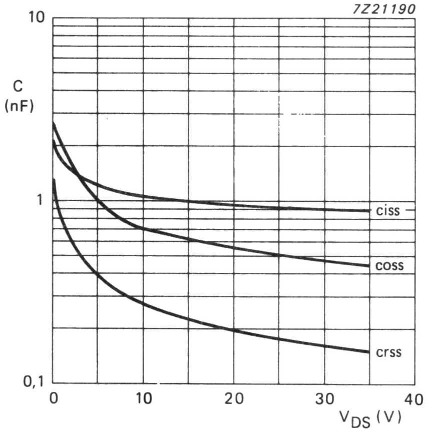


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

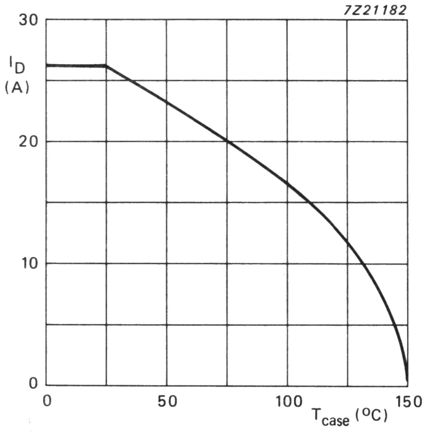


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

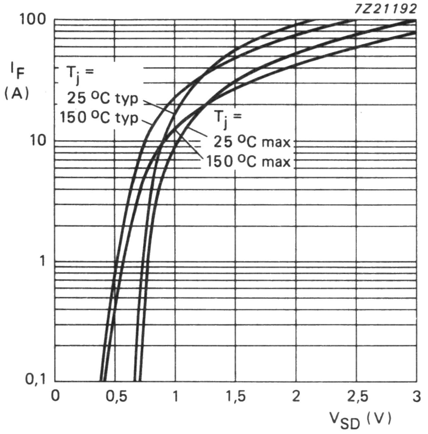


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

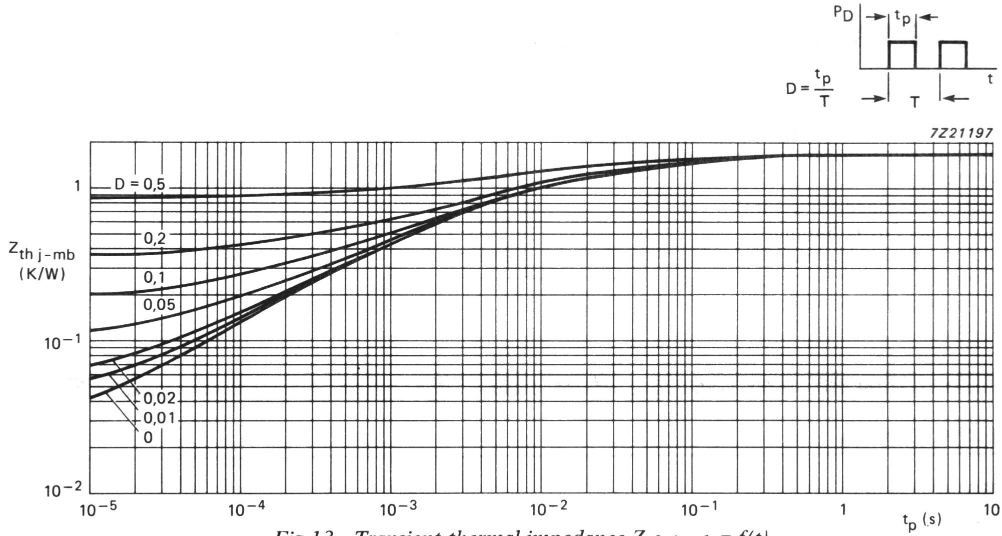


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

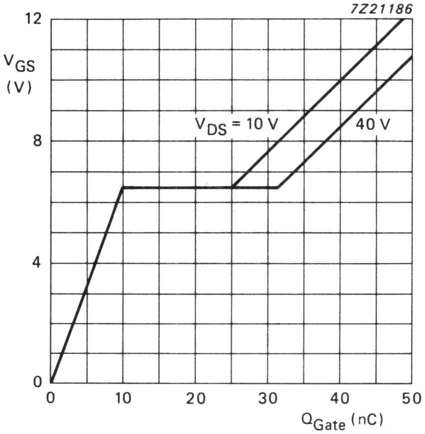


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 45\ A$.

PowerMOS transistor BUZ71

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

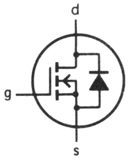
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	14	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,1	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



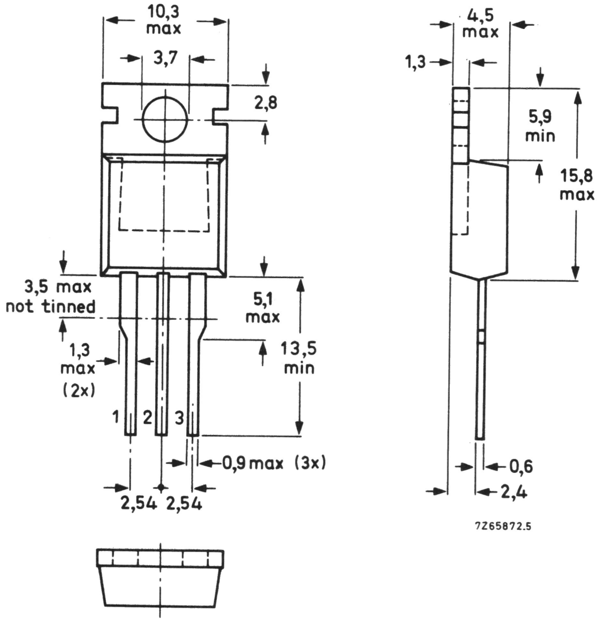

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	14	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	9,0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	56	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 9 A	–	0,09	0,1	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 9 A	3,0	5,2	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	480	650	pF
C_{oss}	Output capacitance		–	280	450	pF
C_{rss}	Feedback capacitance		–	160	280	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	20	30	ns
t_r	Turn-on rise time		–	55	85	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	14	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	56	A
V_{SD}	Diode forward on-voltage	I_F = 28 A; V_{GS} = 0 V	–	1,6	1,8	V
t_{rr}	Reverse recovery time	I_F = 14 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 30 V	–	120	–	ns
Q_{rr}	Reverse recovery charge		–	0,15	–	µC

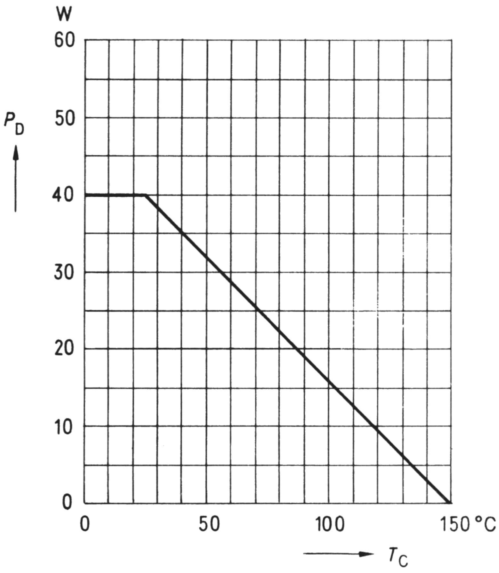


Fig. 2 Power dissipation $P_D = f(T_{mb})$.

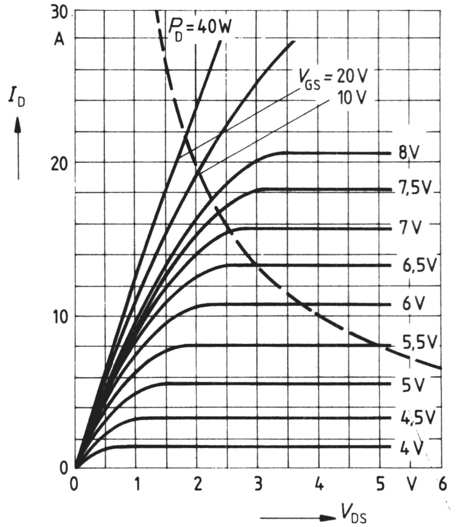


Fig. 3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

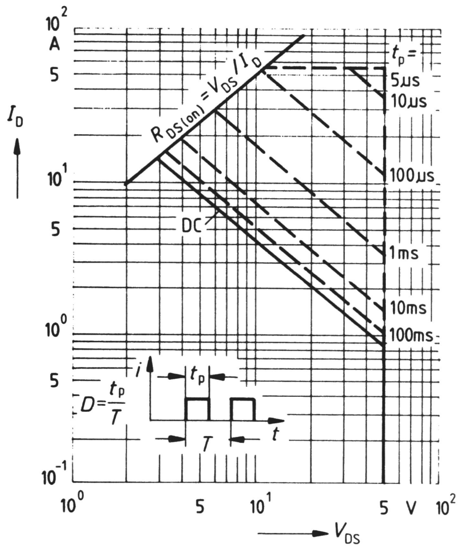


Fig. 4 Safe operating area $I_D(DC)$ and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

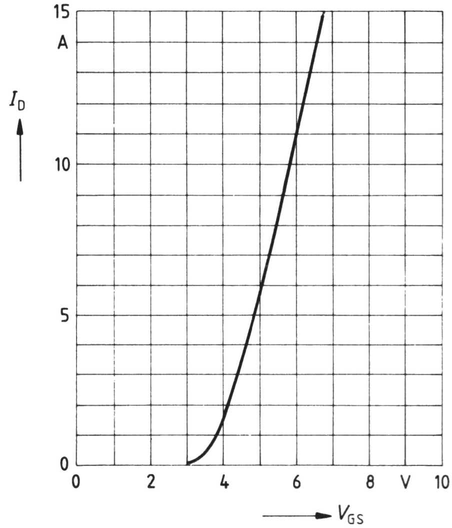


Fig. 5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

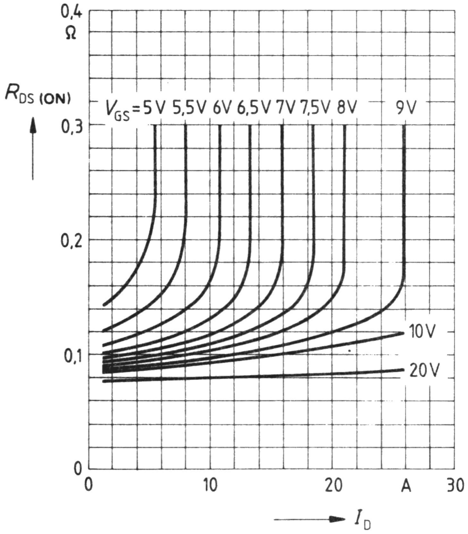


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

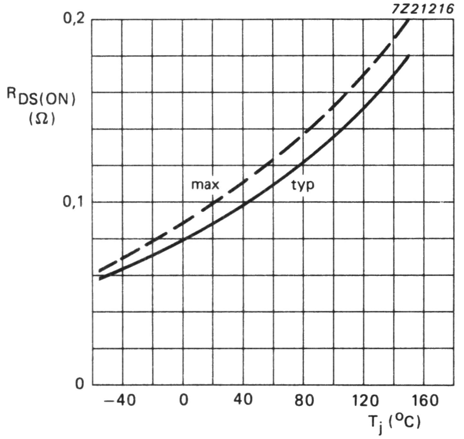


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 9 A; V_{GS} = 10 V.

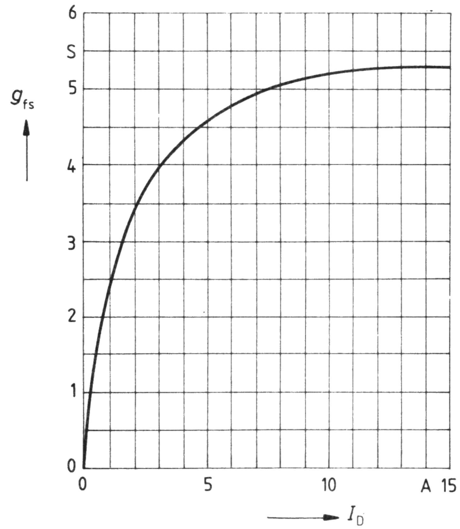


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

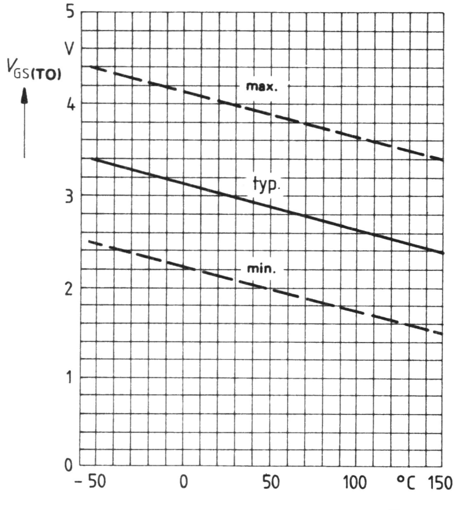


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

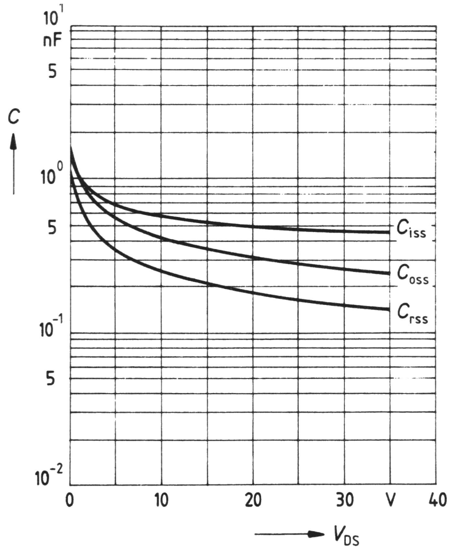


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

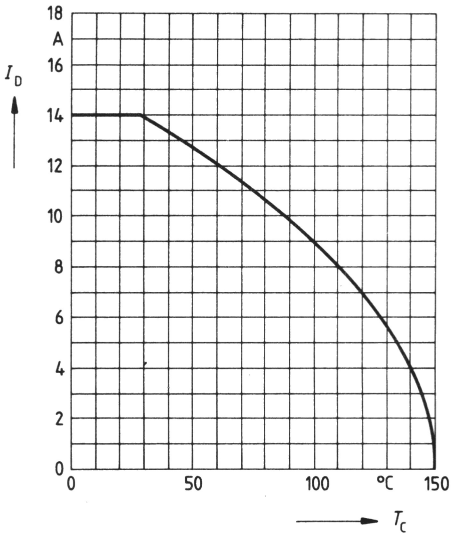


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

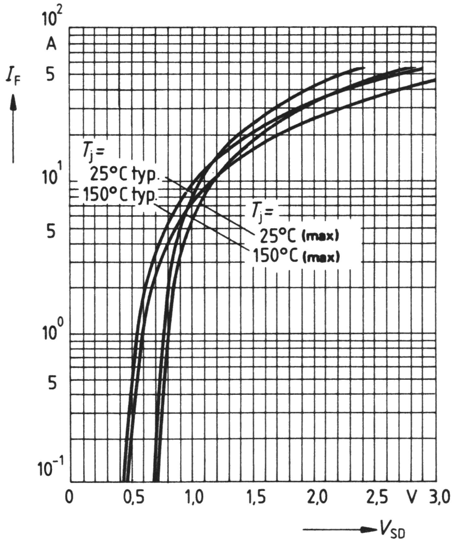


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

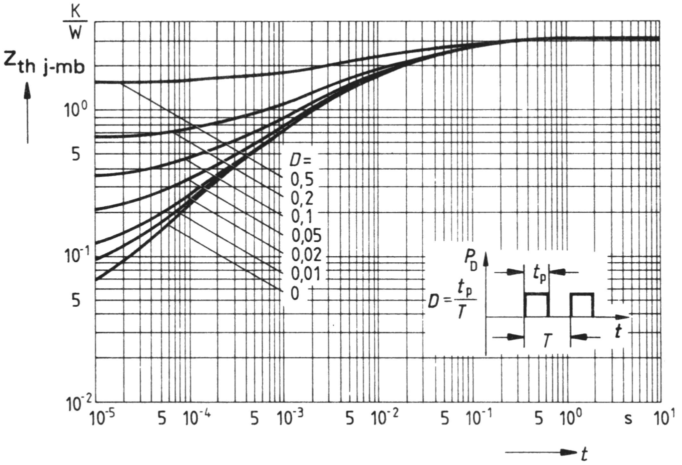


*Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.*

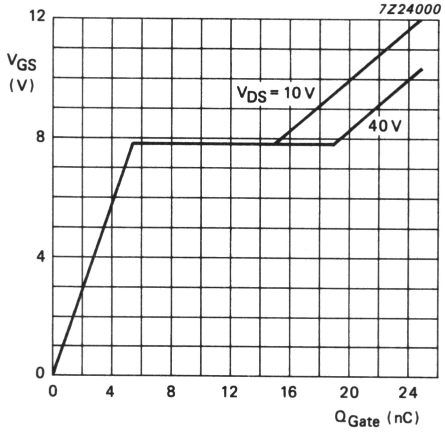


*Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 18\text{ A}$.*

PowerMOS transistor BUZ71A

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

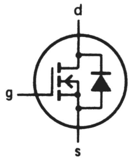
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	13	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,12	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



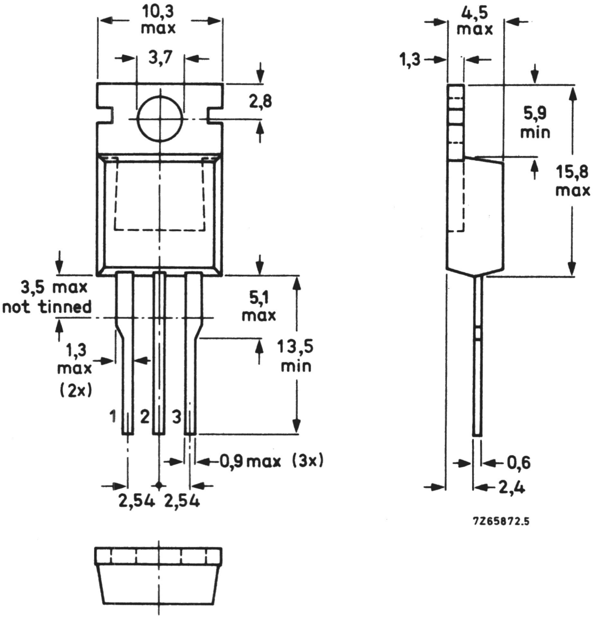

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	13	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	8,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	48	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 9 A	–	0,11	0,12	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 9 A	3,0	5,2	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	480	650	pF
C_{oss}	Output capacitance		–	280	450	pF
C_{rss}	Feedback capacitance		–	160	280	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	20	30	ns
t_r	Turn-on rise time		–	55	85	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	13	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	52	A
V_{SD}	Diode forward on-voltage	I_F = 26 A; V_{GS} = 0 V	–	1,6	2,2	V
t_{rr}	Reverse recovery time	I_F = 13 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 30 V	–	120	–	ns
Q_{rr}	Reverse recovery charge		–	0,15	–	µC

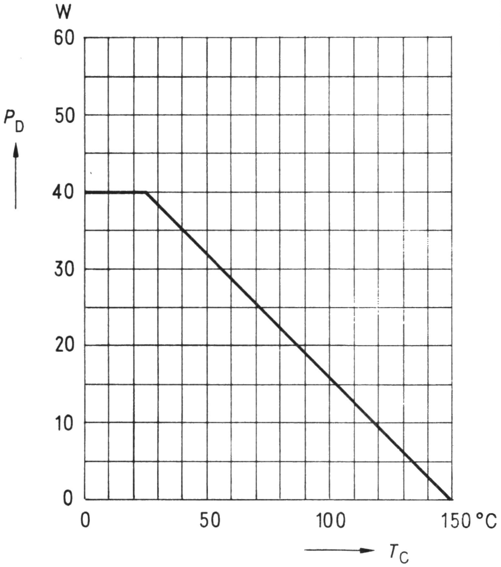


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

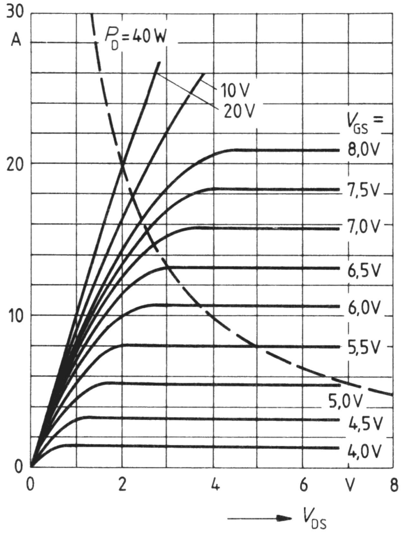


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

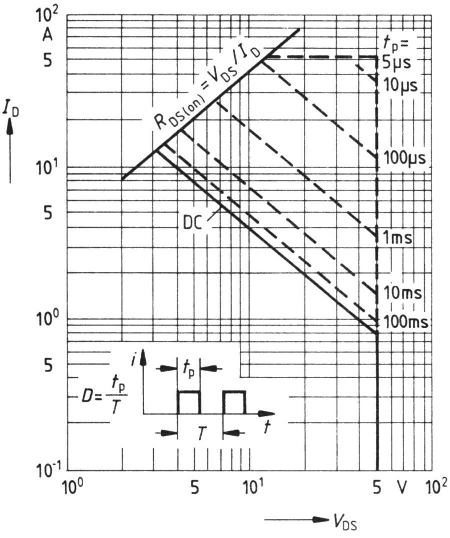


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

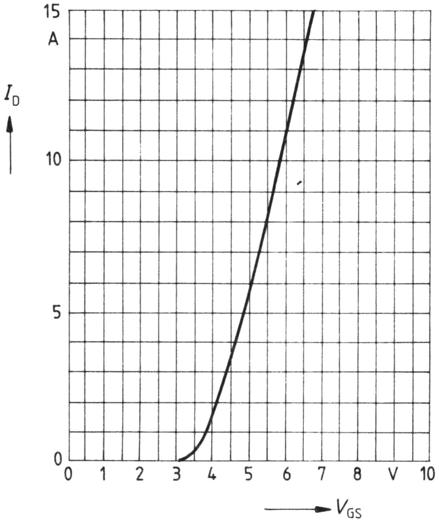


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

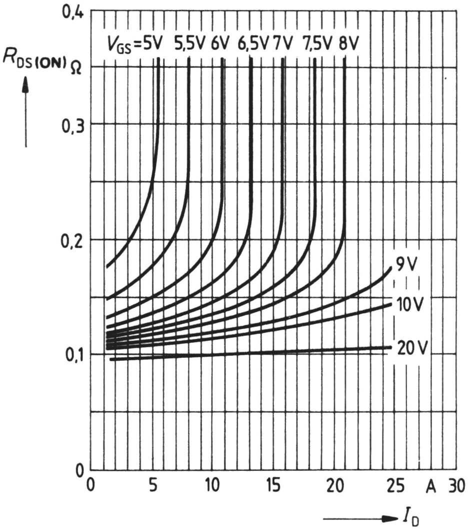


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; T_j = 25 °C.*

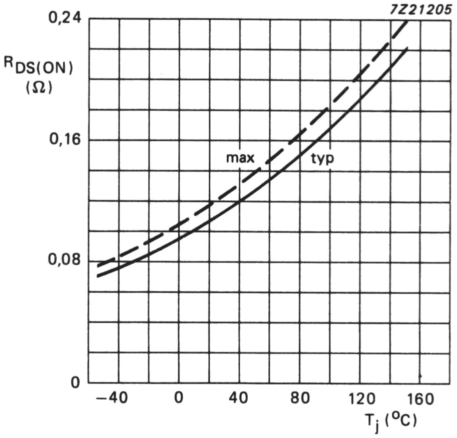


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: I_D = 9 A; V_{GS} = 10 V.*

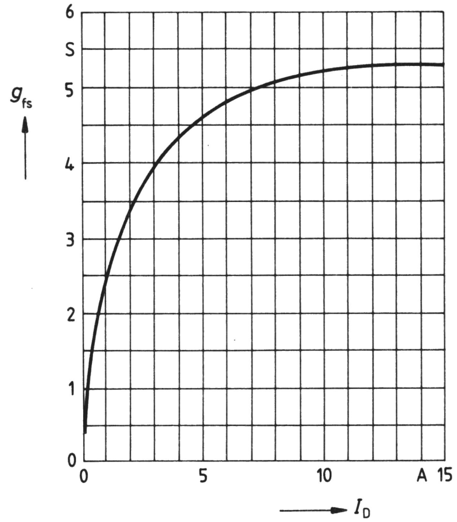


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 μs pulse test; V_{DS} = 25 V; T_j = 25 °C.*

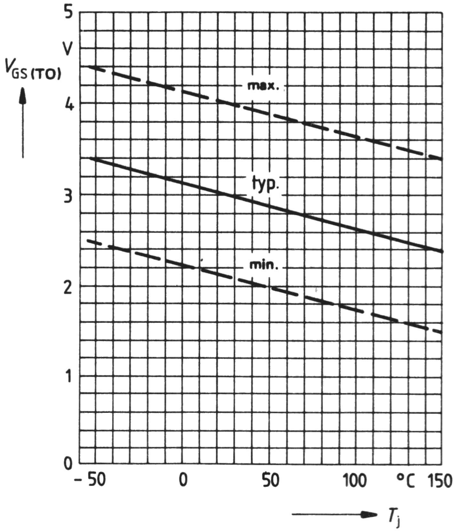


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.*

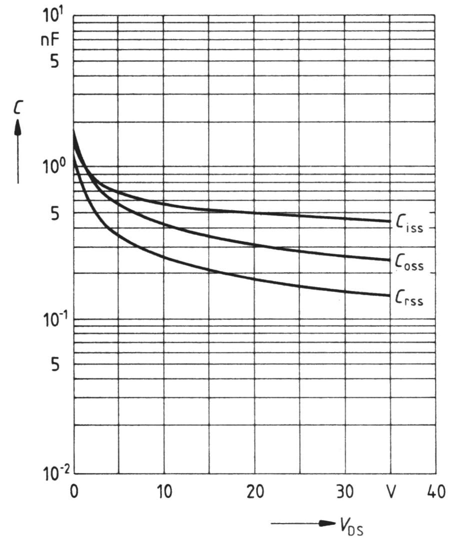


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

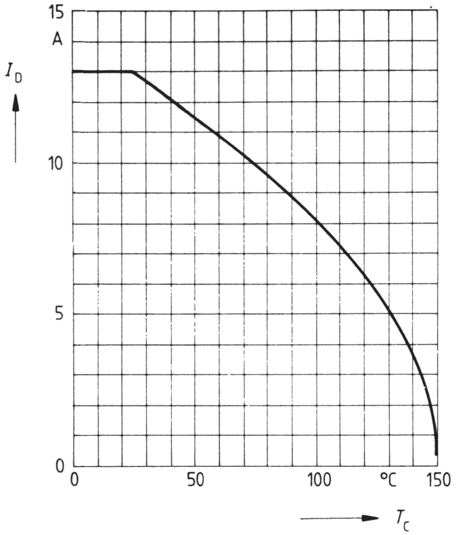


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

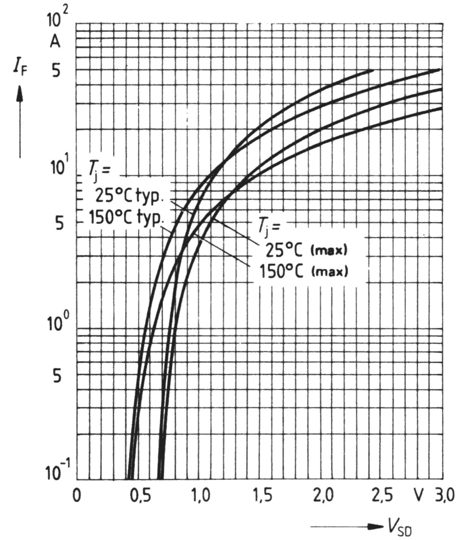


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

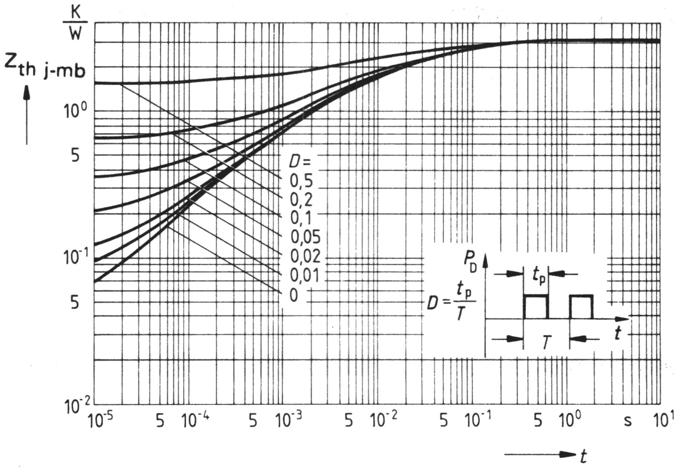


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

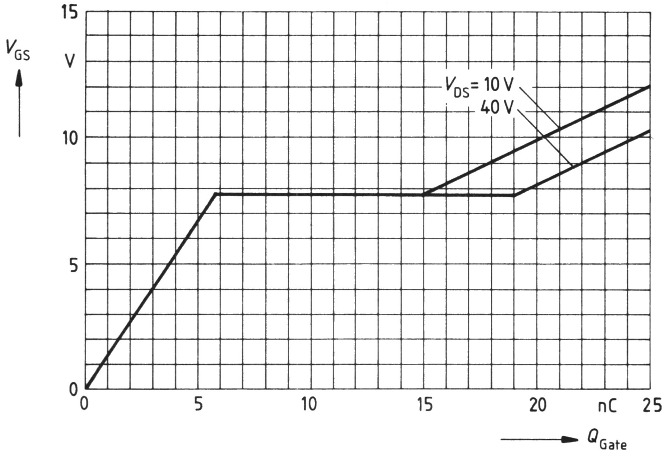


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 18$ A.

PowerMOS transistor BUZ20

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

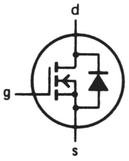
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	15	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,15	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



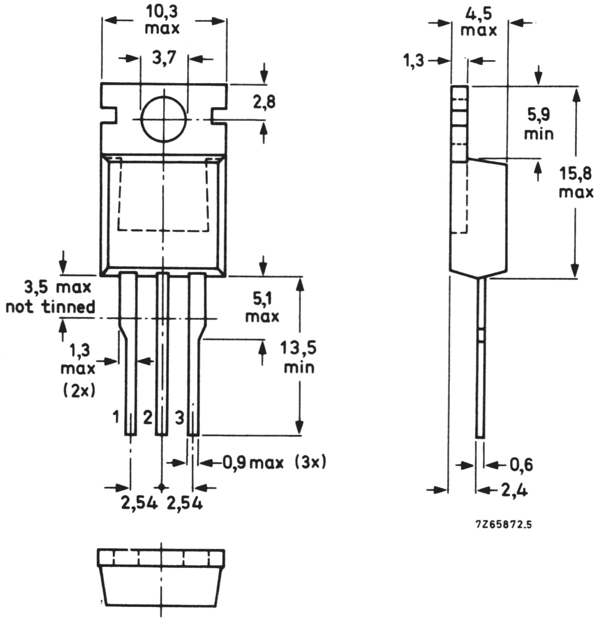

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	15	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	9,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	60	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A	–	0,13	0,15	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 10 A	6,0	10	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	940	1250	pF
C_{oss}	Output capacitance		–	500	750	pF
C_{rss}	Feedback capacitance		–	180	270	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	60	90	ns
$t_{d\ off}$	Turn-off delay time		–	100	130	ns
t_f	Turn-off fall time		–	75	95	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	15	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	60	A
V_{SD}	Diode forward on-voltage	I_F = 30 A; V_{GS} = 0 V	–	1,5	1,8	V
t_{rr}	Reverse recovery time	I_F = 15 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	150	–	ns
Q_{rr}	Reverse recovery charge		–	1,0	–	µC

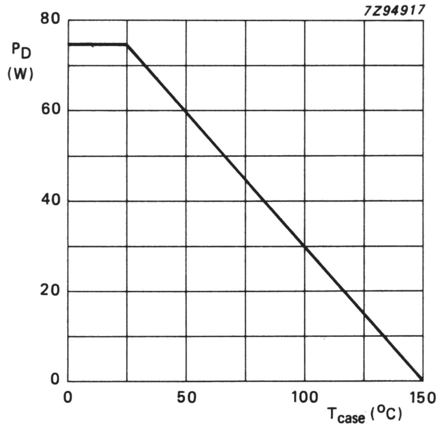


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

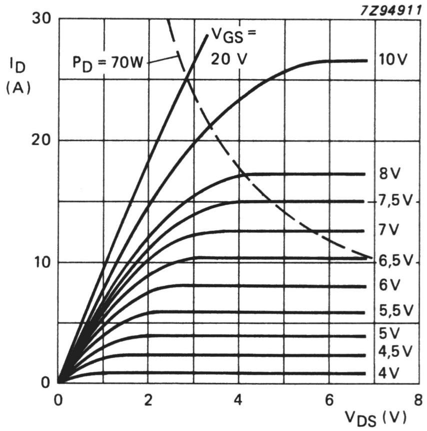


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 μs pulse test; T_{mb} = 25 °C.*

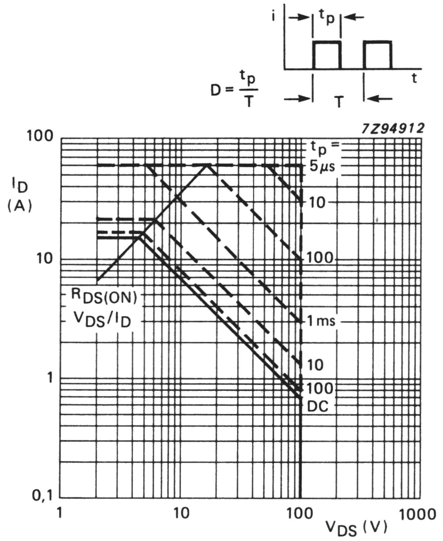


Fig. 4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

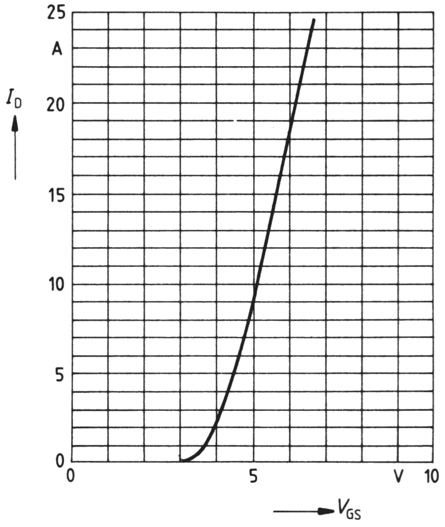


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 μs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

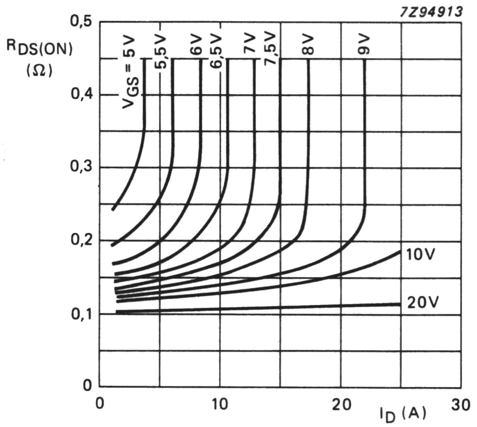


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

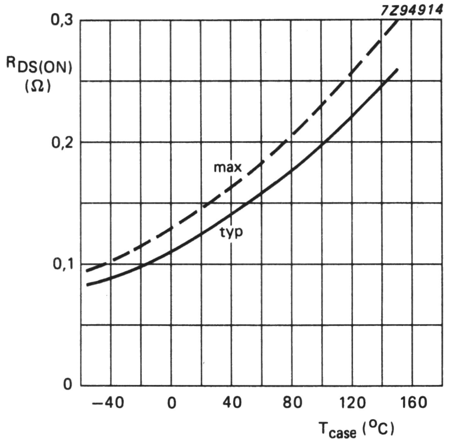


Fig.7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 10 A; V_{GS} = 10 V.

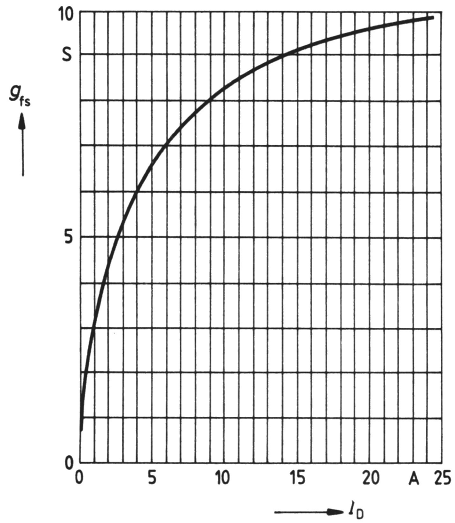


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

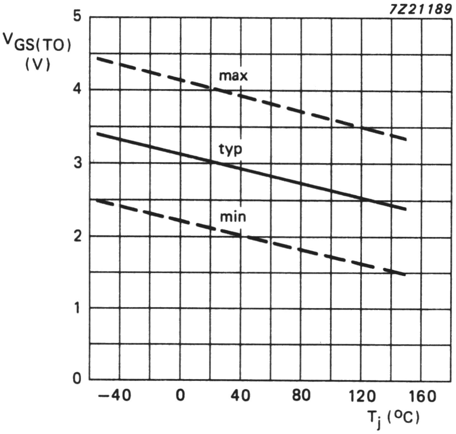


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 10 mA.

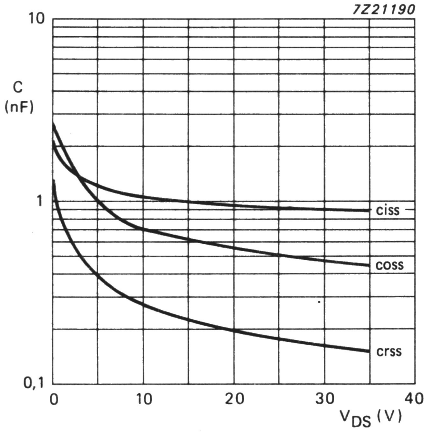


Fig.10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

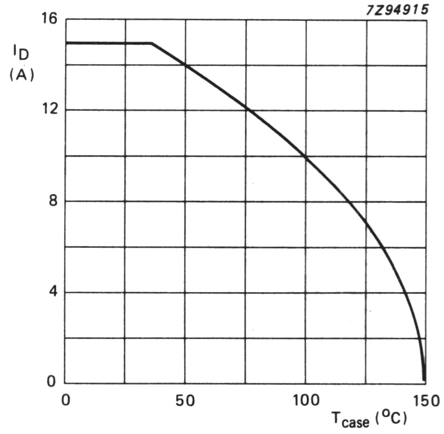


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

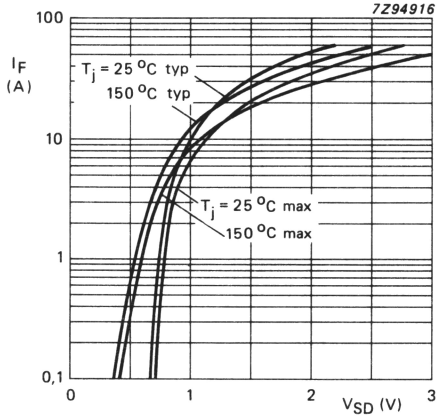


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80\ \mu s$.

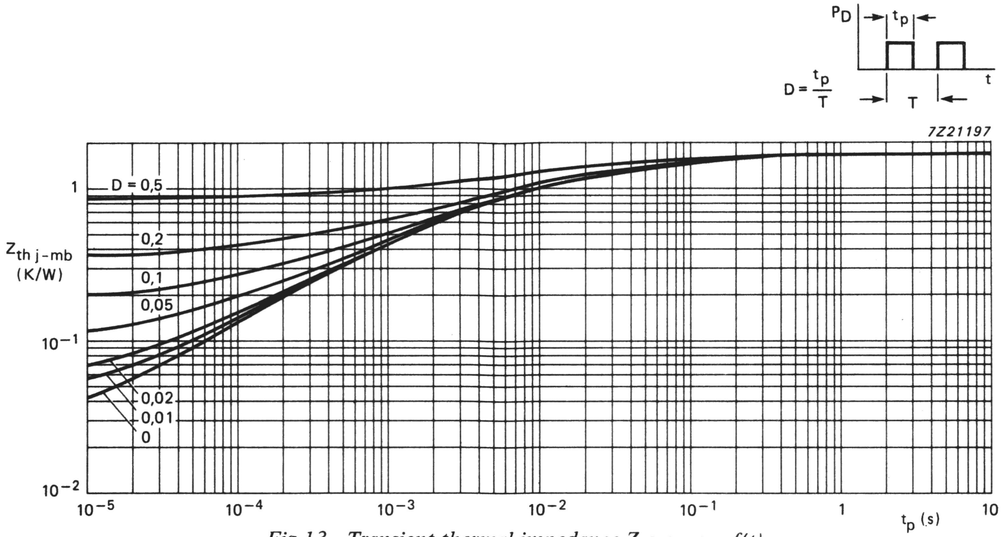


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

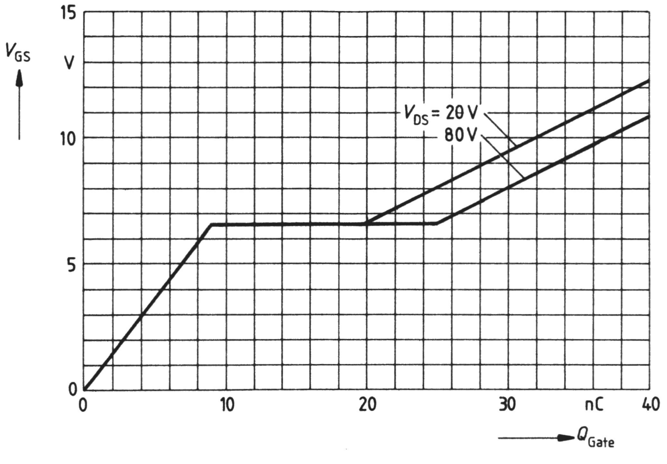


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 18$ A.

PowerMOS transistor BUZ21

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

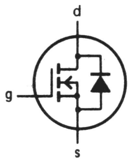
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	21	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,085	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



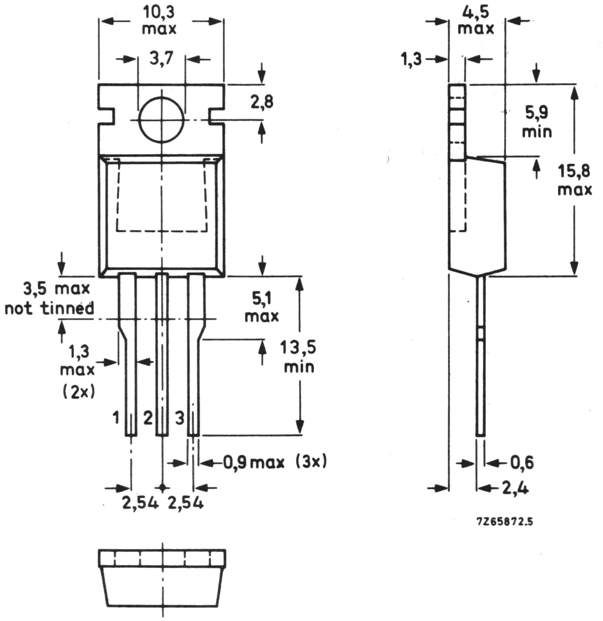

10,3
max
3,7
2,8
3,5 max
not tinned
5,1
max
1,3
max
(2x)
13,5
min
1
2
3
0,9 max (3x)
2,54 2,54
4,5
max
1,3
5,9
min
15,8
max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	21	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	13,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	84	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 13 A	–	0,07	0,085	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 13 A	4,0	8,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	450	700	pF
C_{rss}	Feedback capacitance		–	150	240	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	50	75	ns
$t_{d\ off}$	Turn-off delay time		–	170	220	ns
t_f	Turn-off fall time		–	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	21	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	84	A
V_{SD}	Diode forward on-voltage	I_F = 42 A; V_{GS} = 0 V	–	1,4	1,7	V
t_{rr}	Reverse recovery time	I_F = 21 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	200	–	ns
Q_{rr}	Reverse recovery charge		–	0,25	–	μC

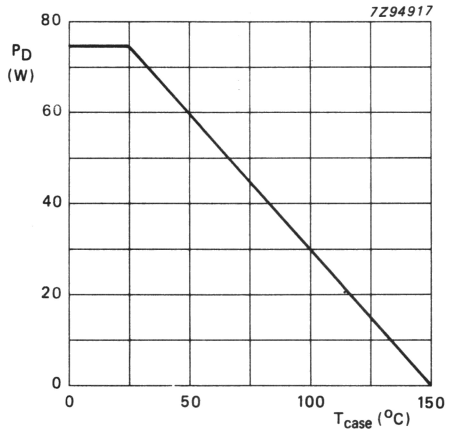


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

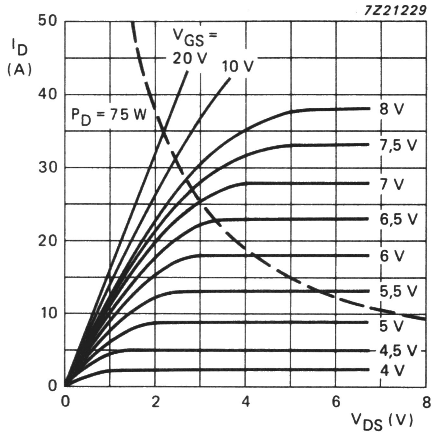


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

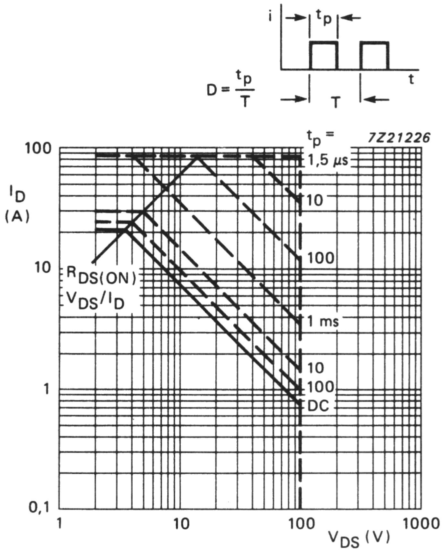


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

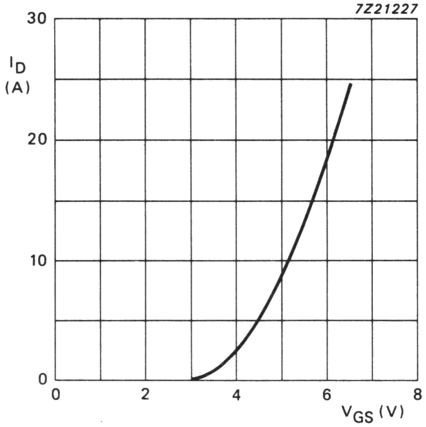


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

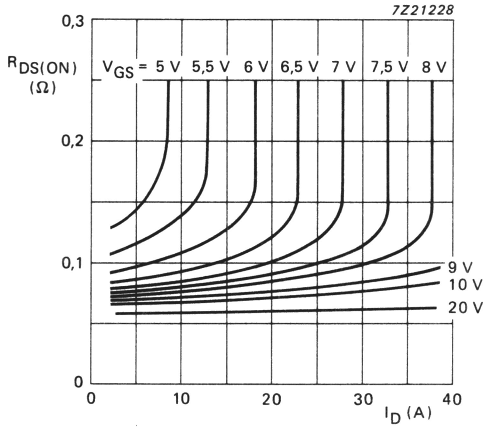


Fig. 6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

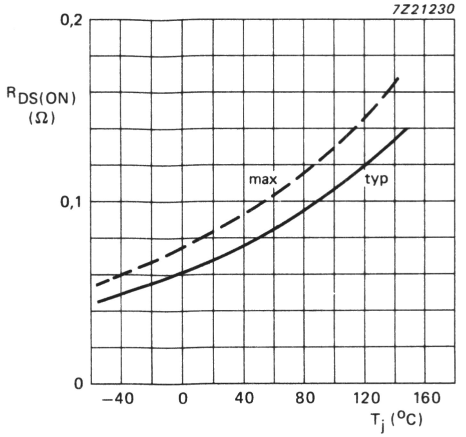


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 13 A; V_{GS} = 10 V.

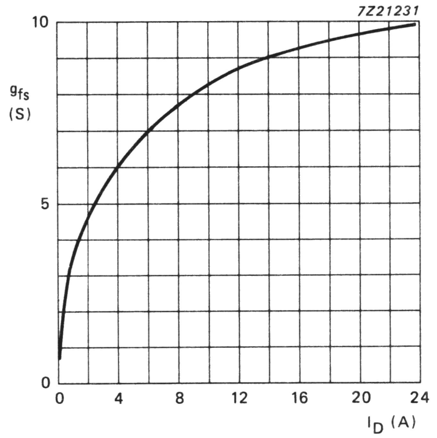


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

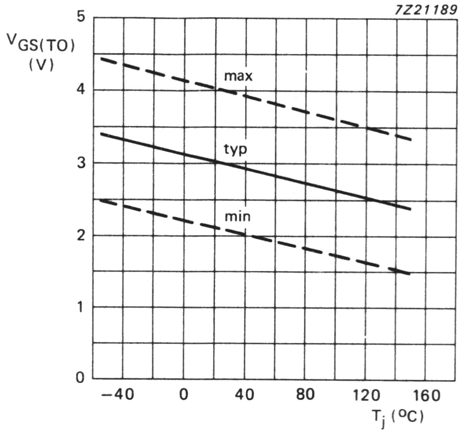


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 10 mA.

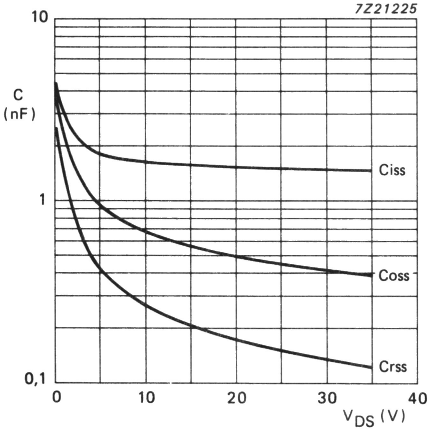


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

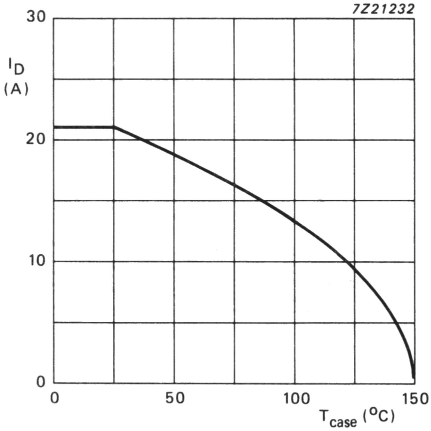


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

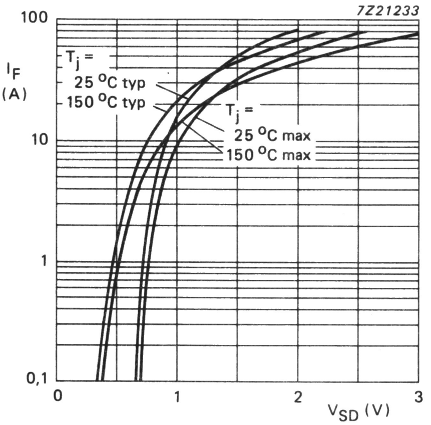


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

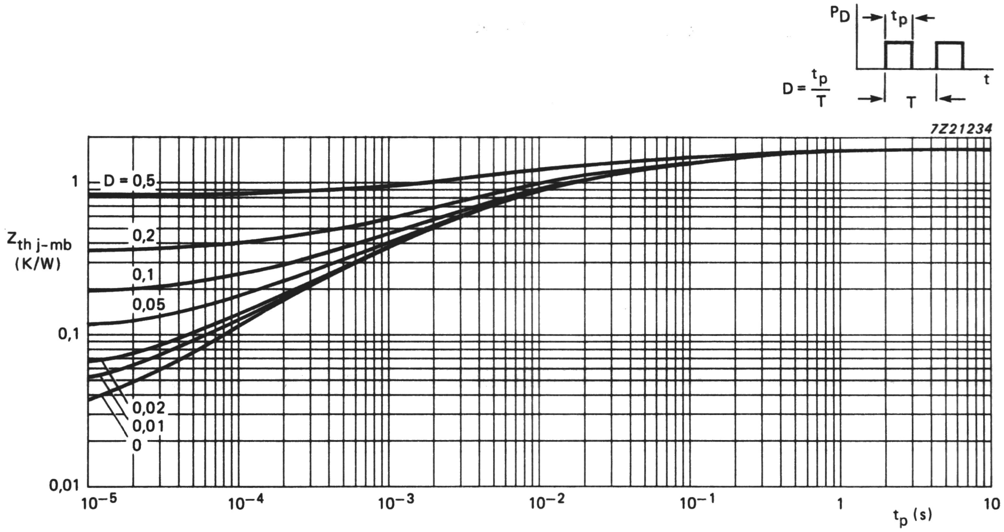


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

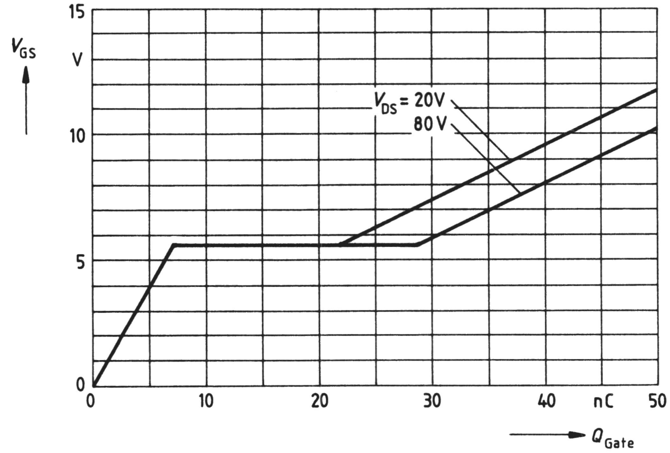


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 21$ A.

PowerMOS transistor BUZ72

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

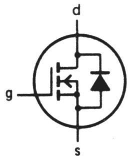
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	10	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,2	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



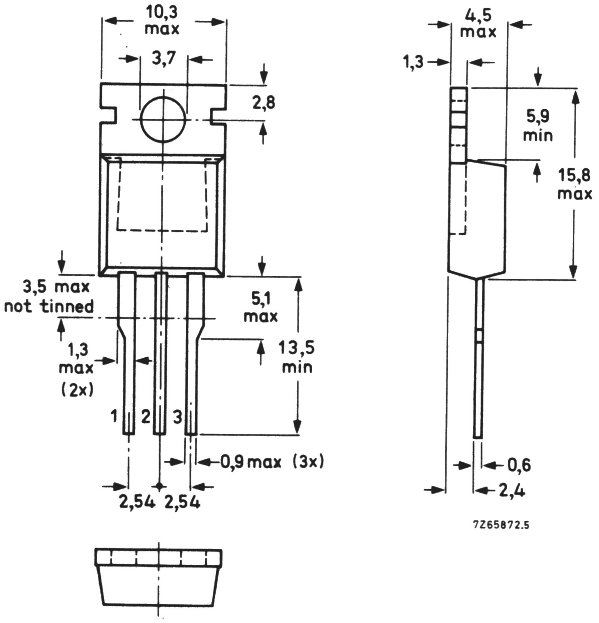

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	10	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,17	0,2	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	3,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	450	600	pF
C_{oss}	Output capacitance		–	150	240	pF
C_{rss}	Feedback capacitance		–	80	130	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	20	30	ns
t_r	Turn-on rise time		–	45	70	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	55	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	10	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	40	A
V_{SD}	Diode forward on-voltage	I_F = 20 A; V_{GS} = 0 V	–	1,55	2,1	V
t_{rr}	Reverse recovery time	I_F = 10 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 30 V	–	170	–	ns
Q_{rr}	Reverse recovery charge		–	0,3	–	μC

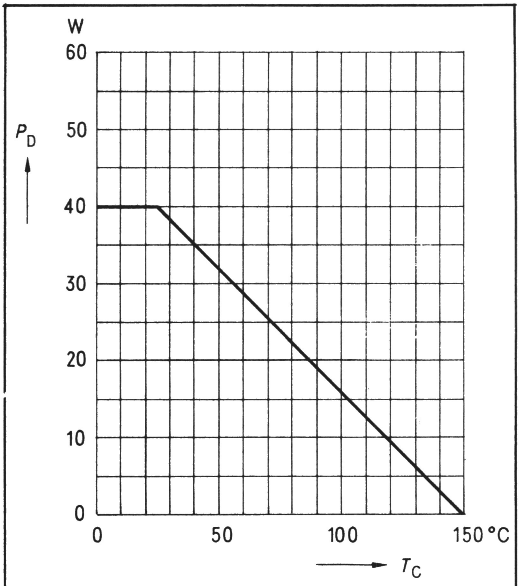


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

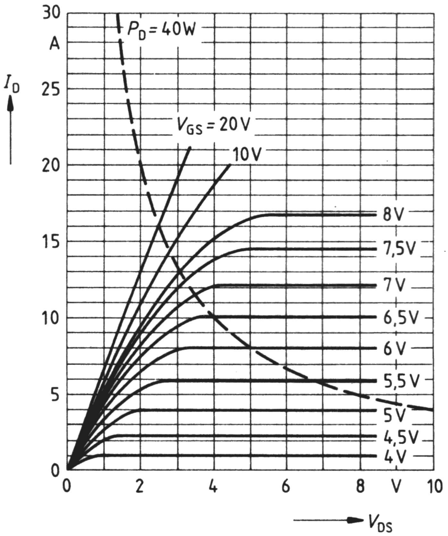


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 µs pulse test; T_{mb} = 25 °C.*

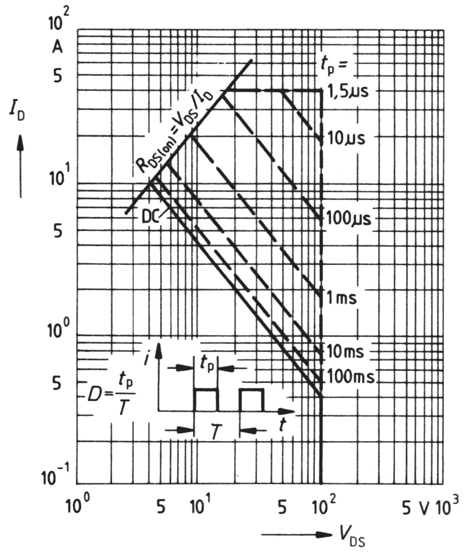


Fig. 4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

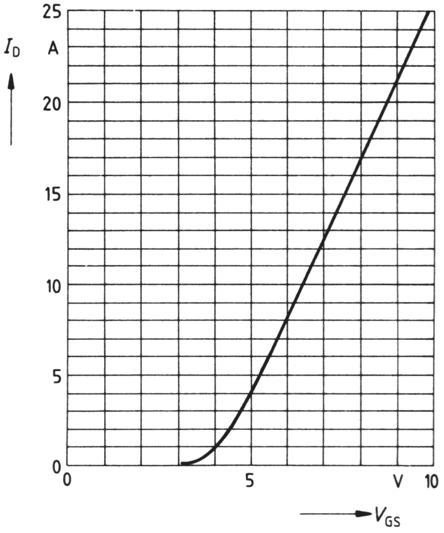


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 µs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

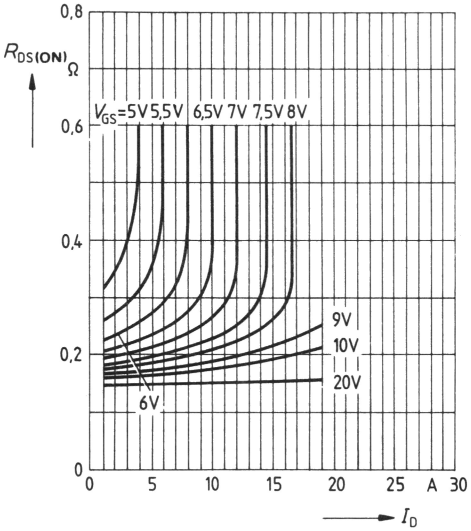


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

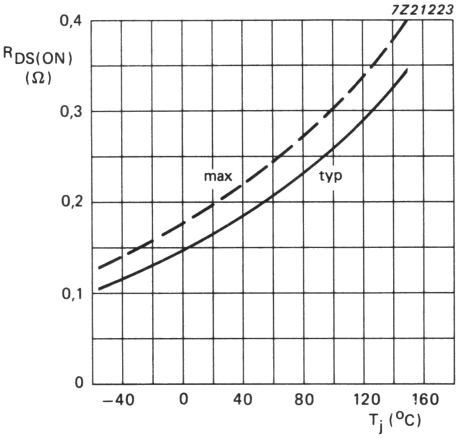


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 5 A; V_{GS} = 10 V.

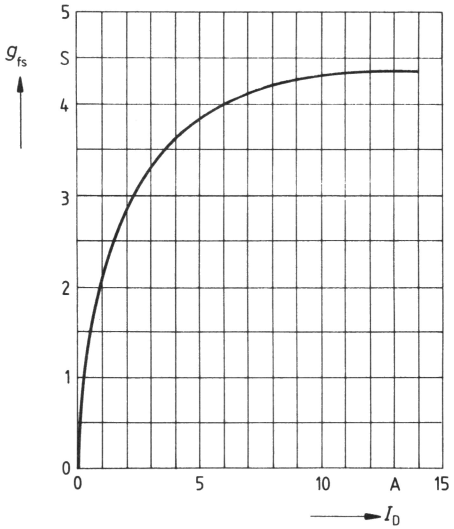


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

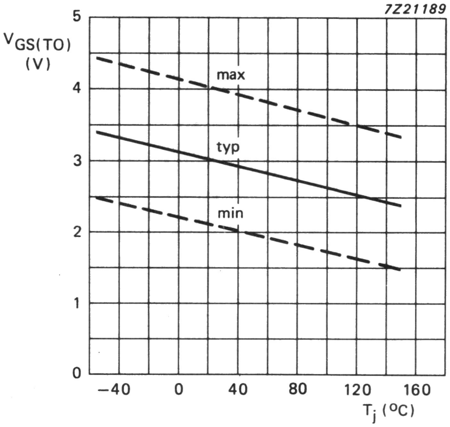


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

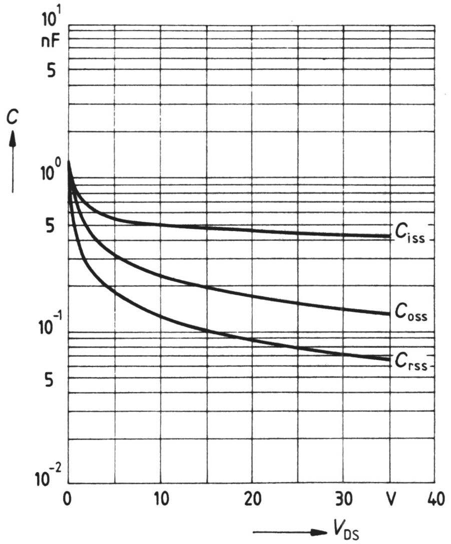


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

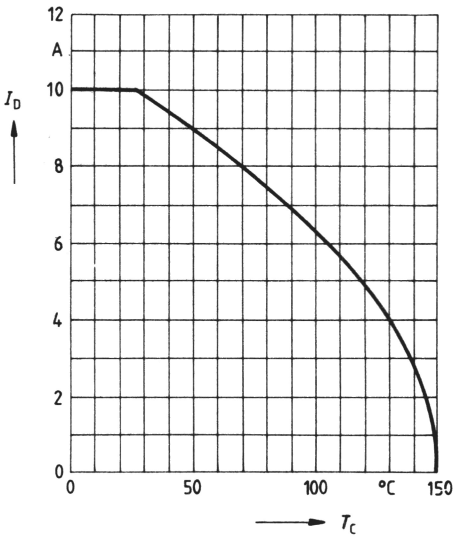


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

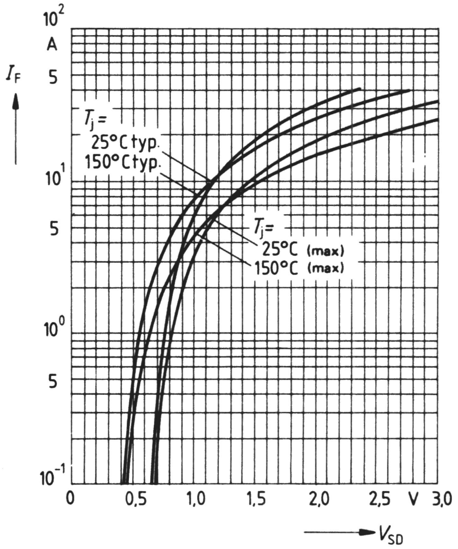


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

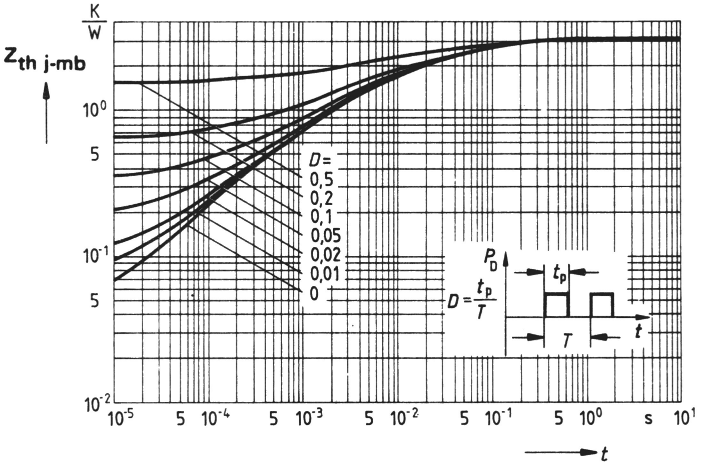


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

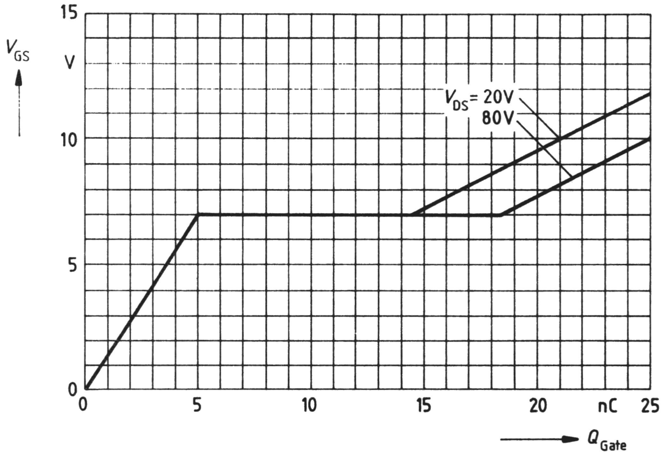


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 14$ A.

PowerMOS transistor BUZ72A

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

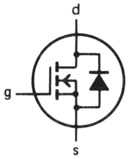
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	9,0	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,25	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



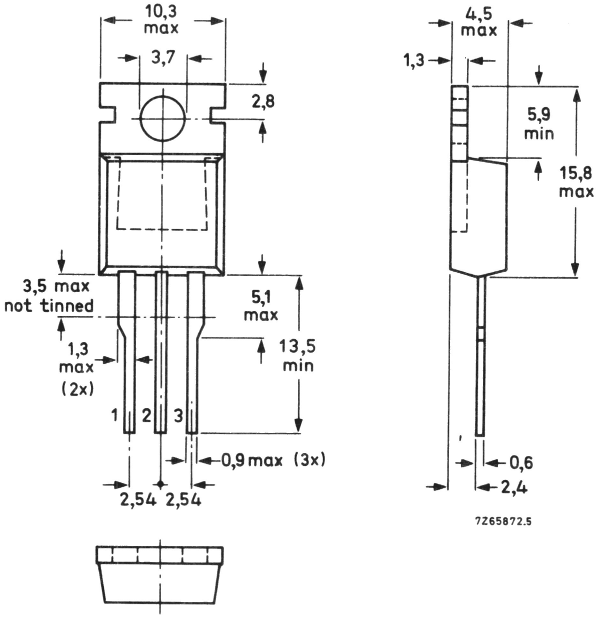

10,3
max
3,7
2,8
4,5
max
1,3
5,9
min
15,8
max
3,5 max
not tinned
5,1
max
1,3
max
(2x)
13,5
min
1
2
3
0,9 max (3x)
2,54 2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	9,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	5,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,23	0,25	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	3,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	450	600	pF
C_{oss}	Output capacitance		–	150	240	pF
C_{rss}	Feedback capacitance		–	80	130	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	20	30	ns
t_r	Turn-on rise time		–	45	70	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	55	70	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	9,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	36	A
V_{SD}	Diode forward on-voltage	I_F = 18 A; V_{GS} = 0 V	–	1,5	2,0	V
t_{rr}	Reverse recovery time	I_F = 9 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 30 V	–	170	–	ns
Q_{rr}	Reverse recovery charge		–	0,3	–	µC

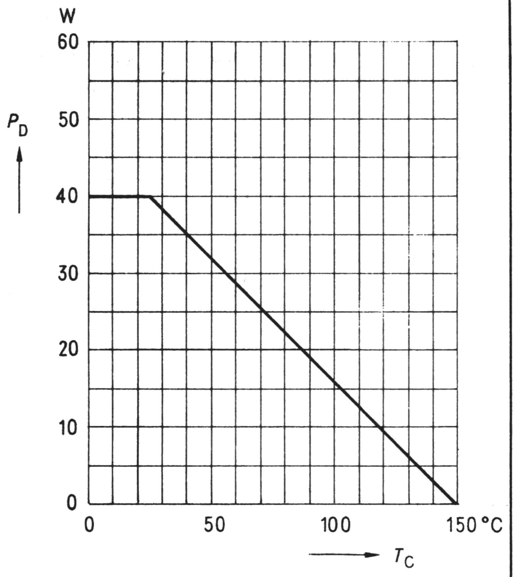


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

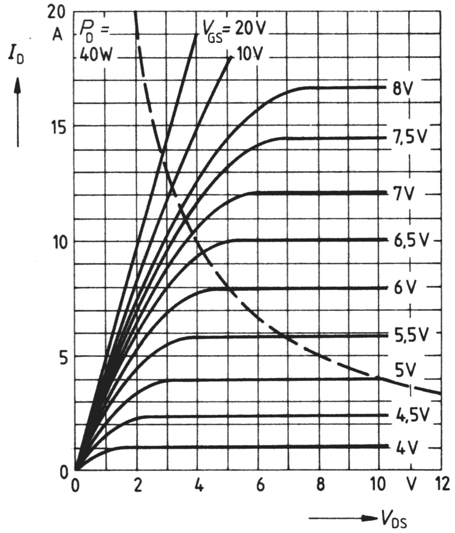


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

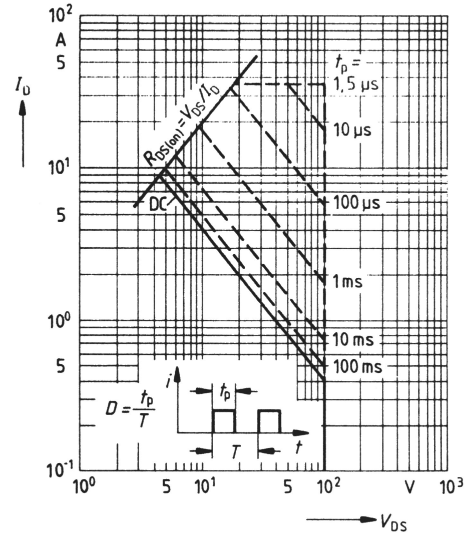


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

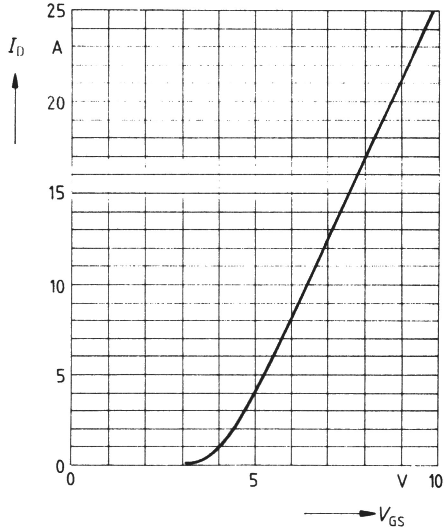


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

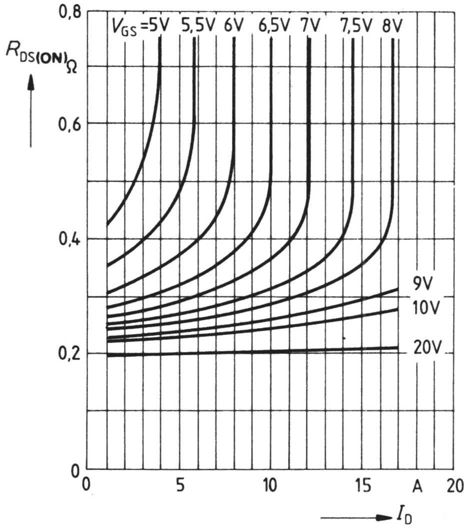


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

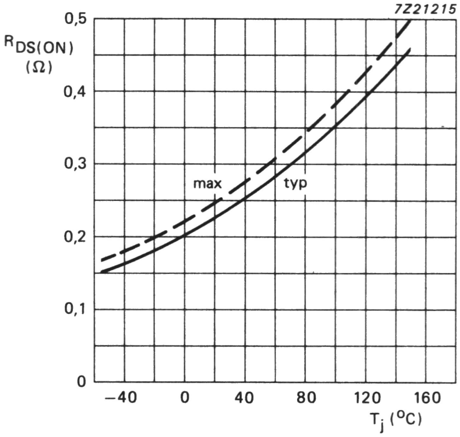


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 5$ A; $V_{GS} = 10$ V.

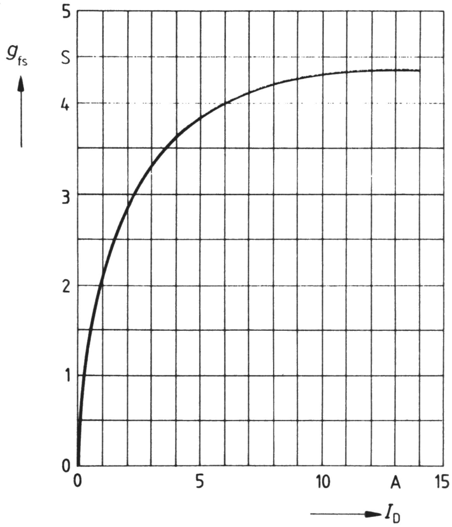


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

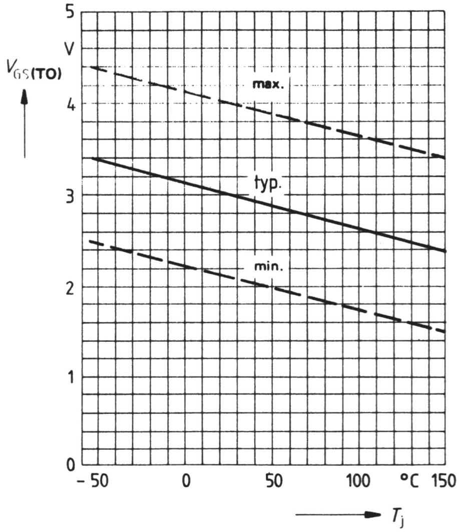


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

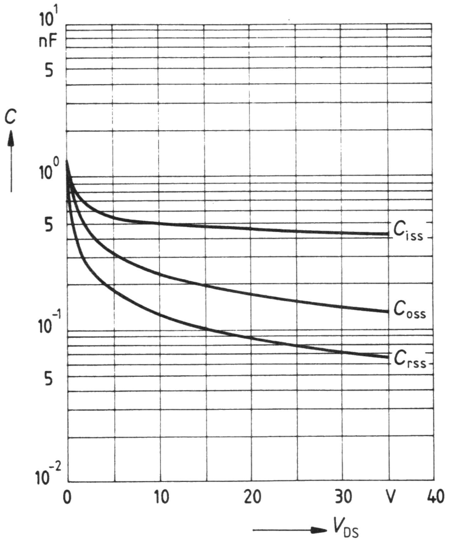


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

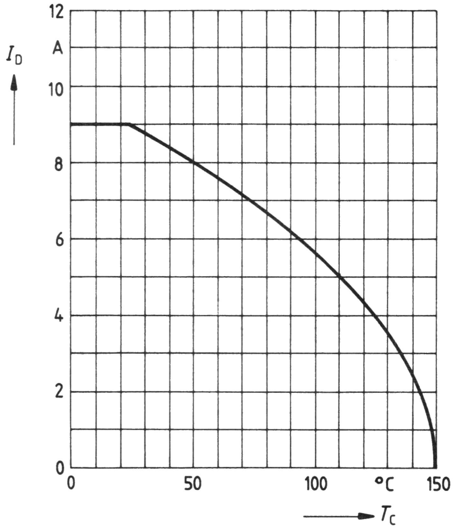


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

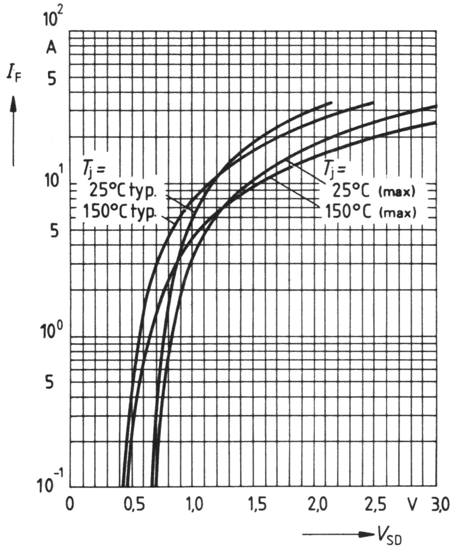


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

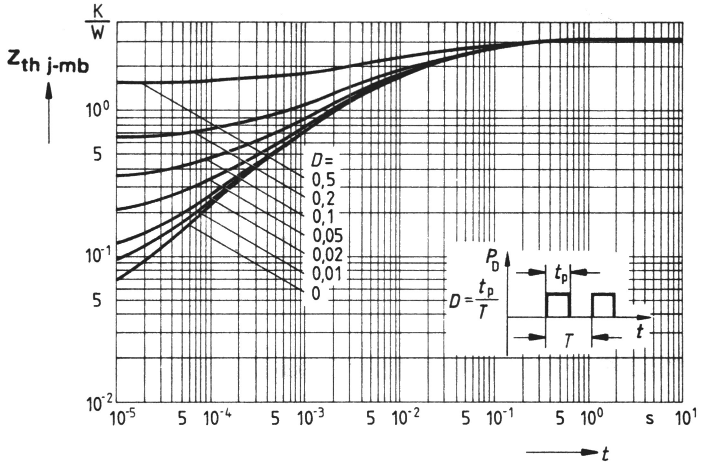


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

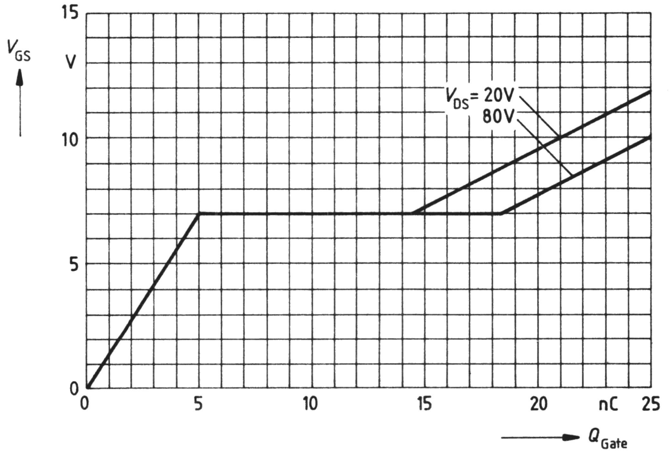


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 14$ A.

PowerMOS transistor

BUZ31

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

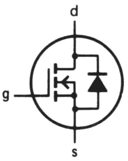
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	12,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,2	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



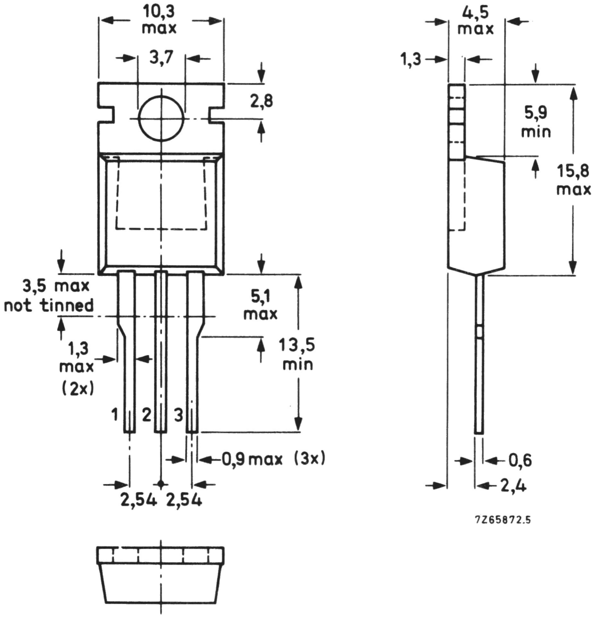

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig.1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 45 °C	–	12,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	8,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	50	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A	–	0,17	0,2	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 7 A	3,0	5,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	300	500	pF
C_{rss}	Feedback capacitance		–	140	250	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	170	220	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	12,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	50	A
V_{SD}	Diode forward on-voltage	I_F = 25 A; V_{GS} = 0 V	–	1,4	1,8	V
t_{rr}	Reverse recovery time	I_F = 12,5 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	400	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	μC

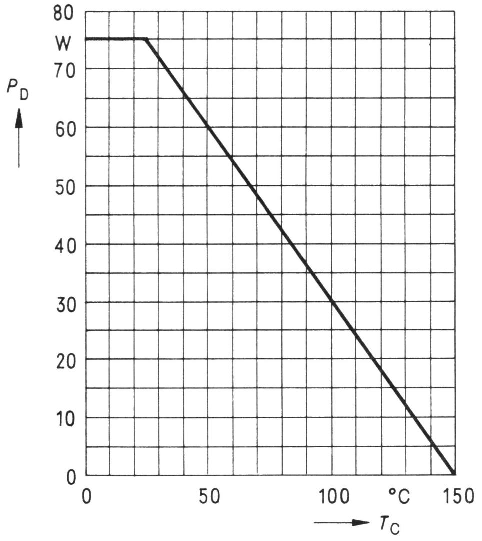


Fig.2 Power dissipation $P_D = f(T_{mb})$.

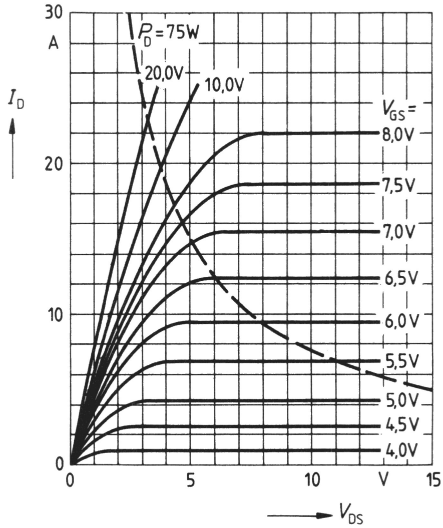


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

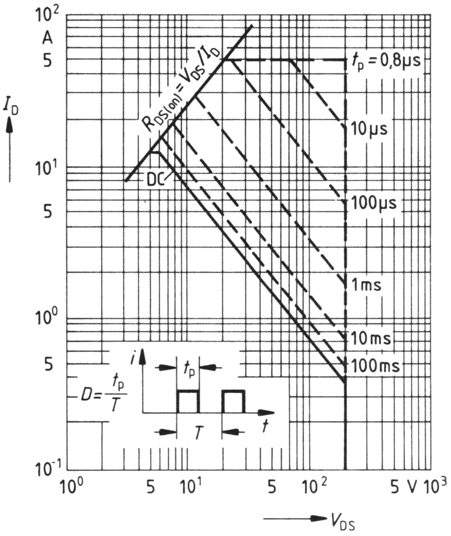


Fig.4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

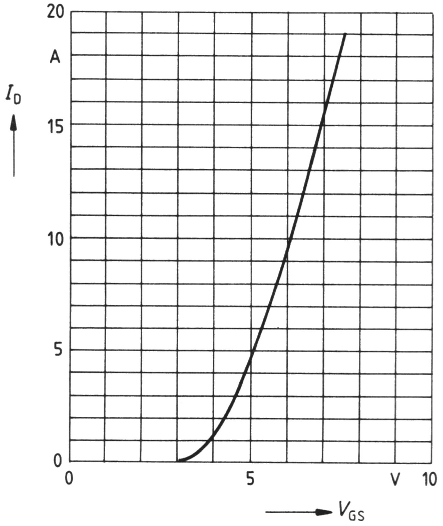


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

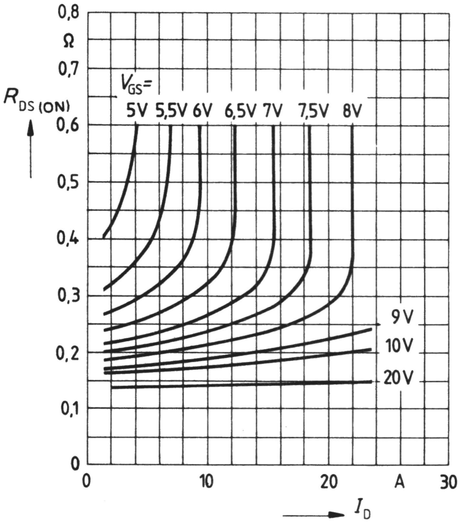


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

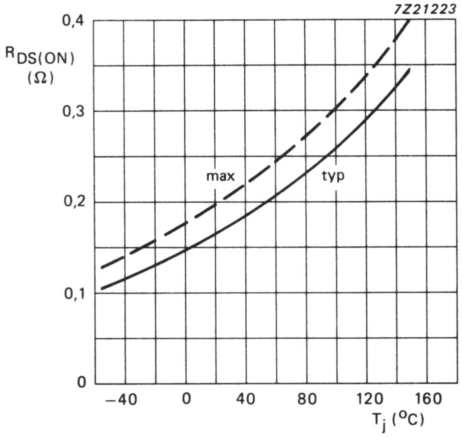


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 7 A; V_{GS} = 10 V.

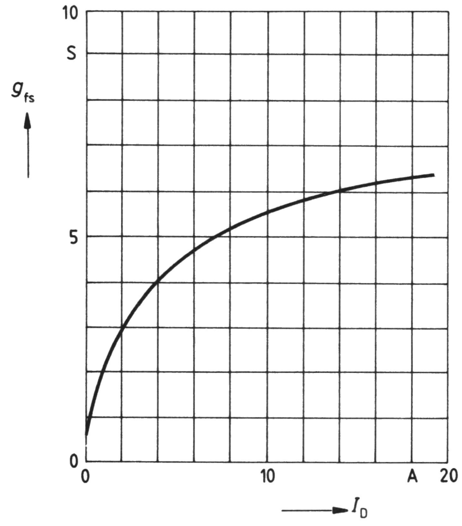


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

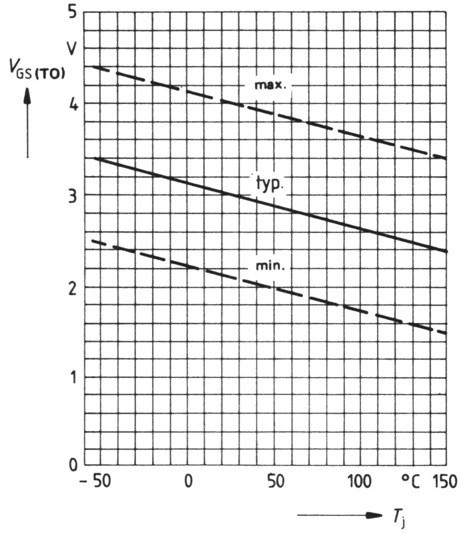


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

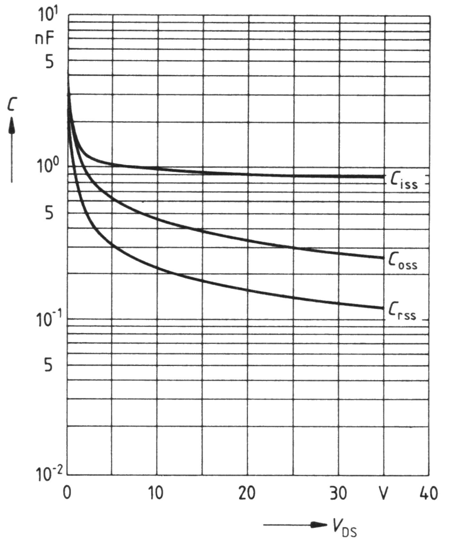


Fig.10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

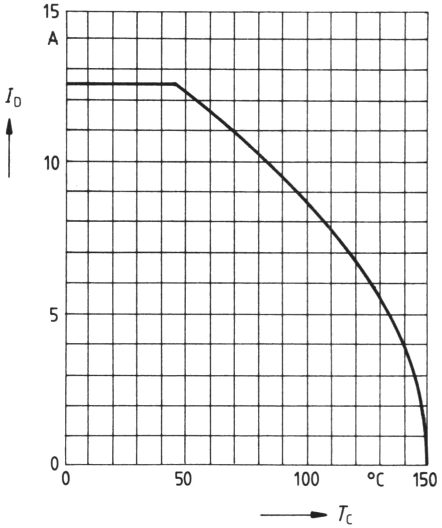


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

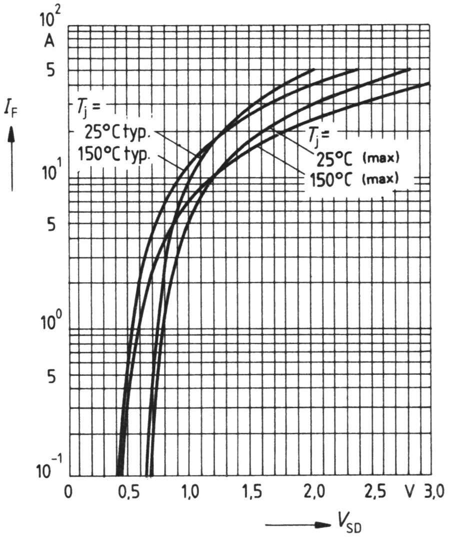


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

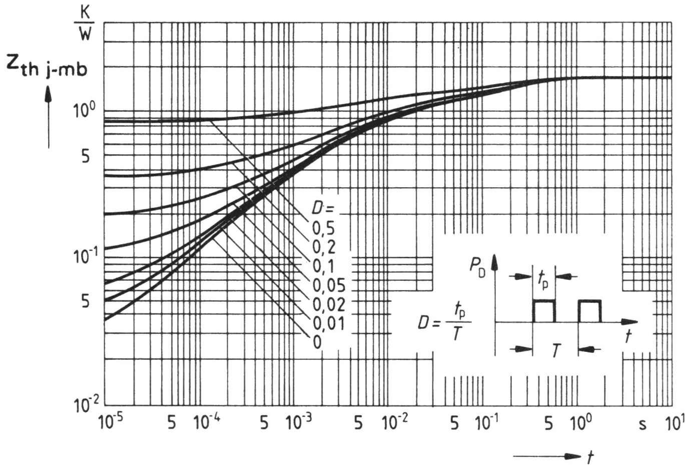


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

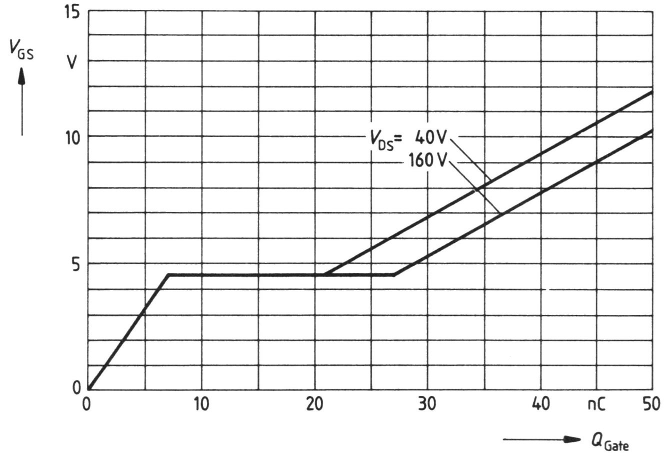


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 18,8 A.

PowerMOS transistor BUZ32

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

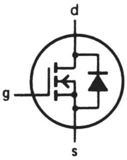
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	10,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,32	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



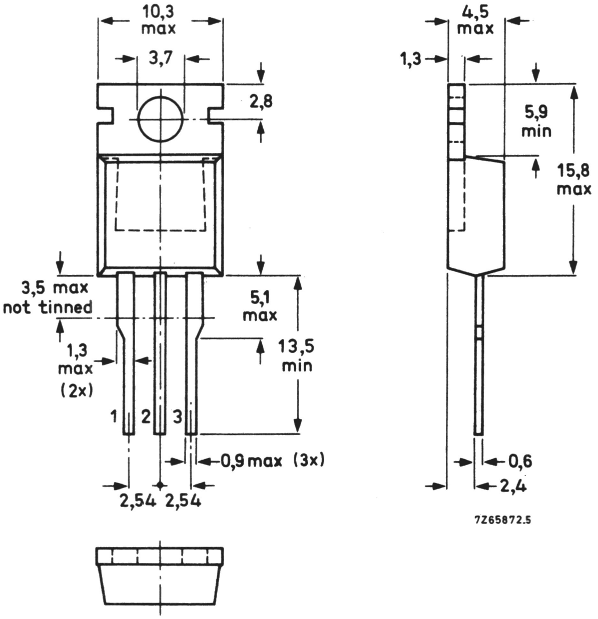

10,3
max
3,7
2,8
4,5
max
1,3
5,9
min
15,8
max
3,5 max
not tinned
5,1
max
1,3
max
(2x)
13,5
min
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	10,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	42	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6,8 A	–	0,25	0,32	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6,8 A	5,0	8,4	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	940	1250	pF
C_{oss}	Output capacitance		–	500	750	pF
C_{rss}	Feedback capacitance		–	180	270	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	60	90	ns
$t_{d\ off}$	Turn-off delay time		–	100	130	ns
t_f	Turn-off fall time		–	75	95	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	9,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	42	A
V_{SD}	Diode forward on-voltage	I_F = 21 A; V_{GS} = 0 V	–	1,3	1,5	V
t_{rr}	Reverse recovery time	I_F = 10,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	400	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	µC

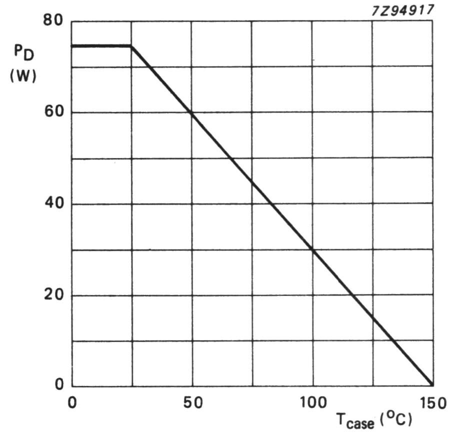


Fig.2 Power dissipation $P_D = f(T_{mb})$.

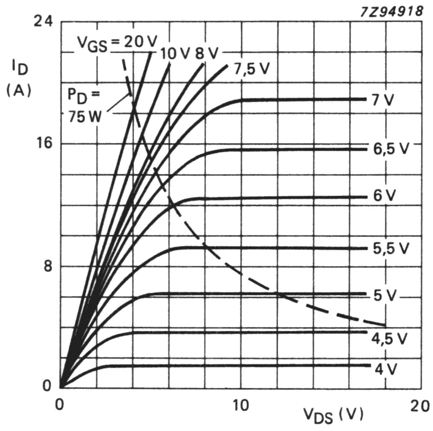


Fig.3 Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 μs pulse test; T_{mb} = 25 °C.

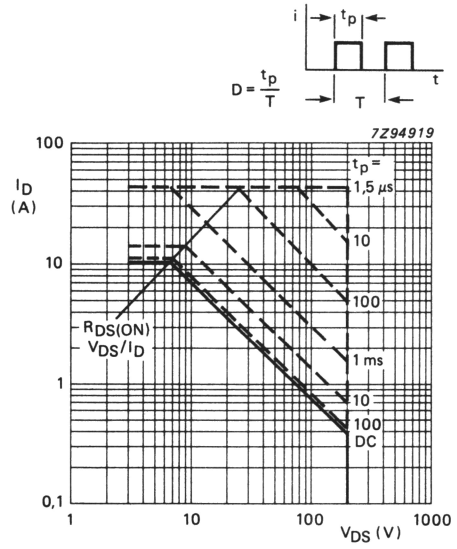


Fig.4 Safe operating area $I_D(DC)$ and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

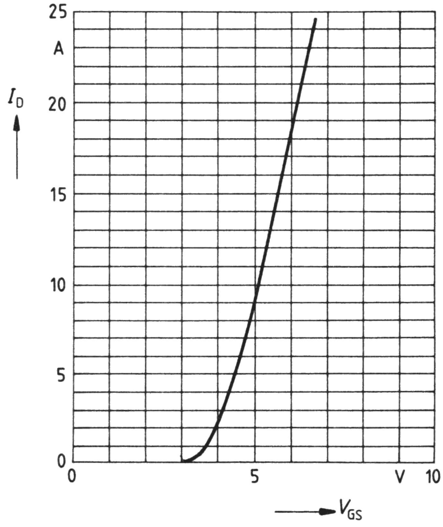


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 μs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.

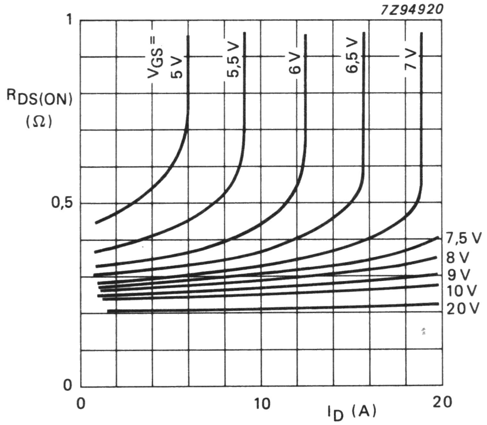


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

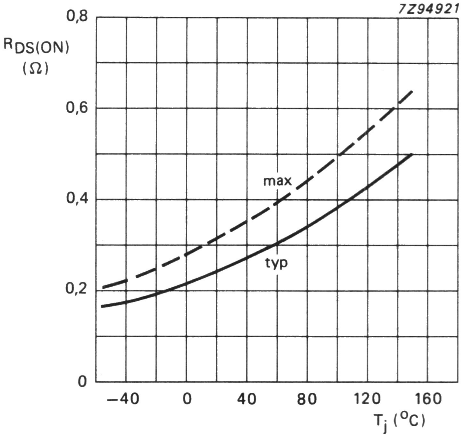


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 6{,}8$ A; $V_{GS} = 10$ V.

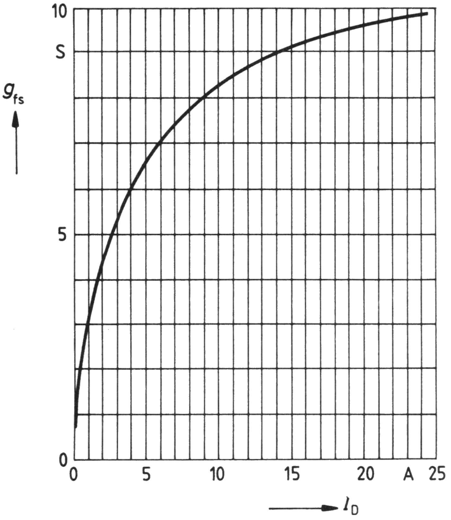


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

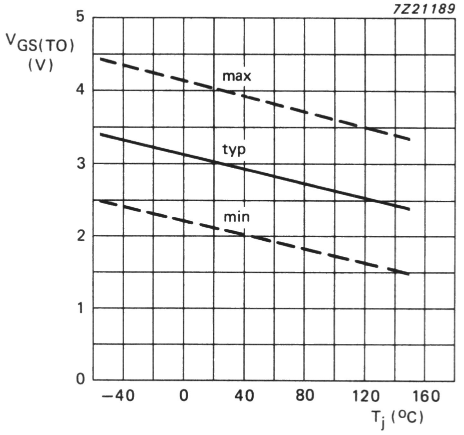


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 10$ mA.

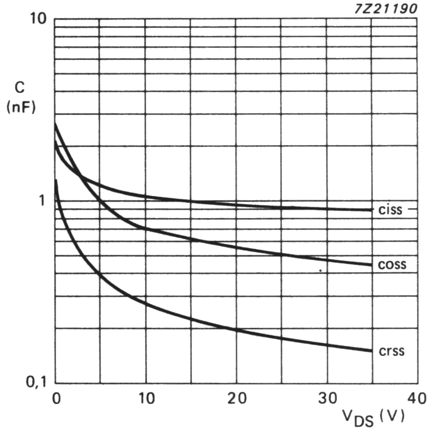


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

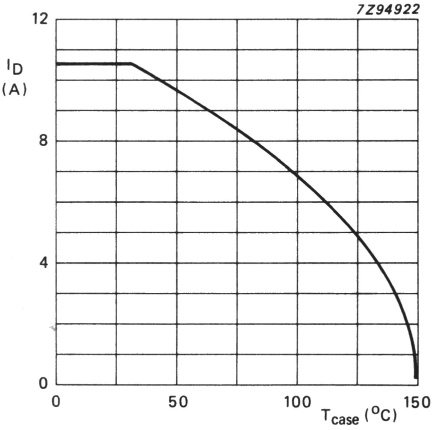


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

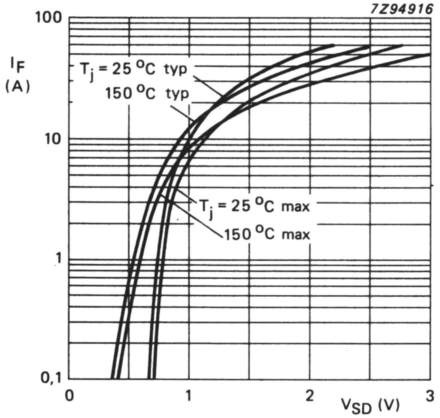


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

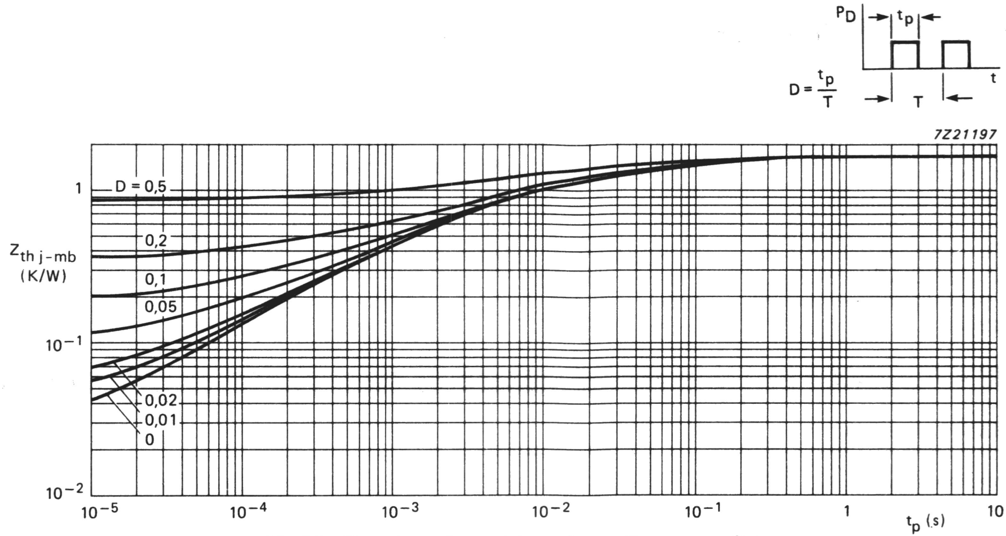


Fig.13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

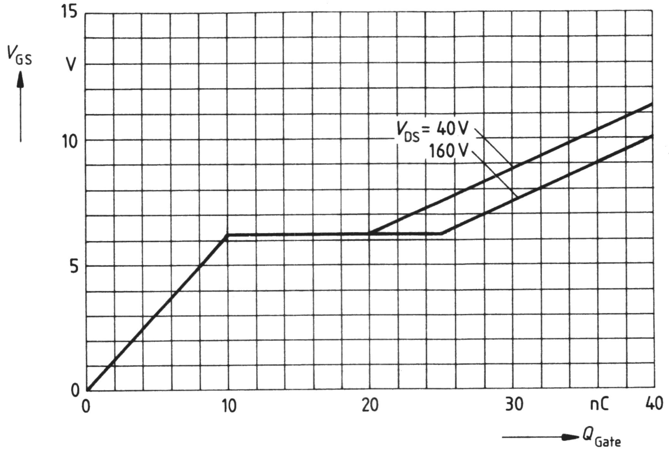


Fig.14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 14{,}3$ A.

PowerMOS transistor BUZ73

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

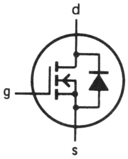
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	7,0	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,4	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



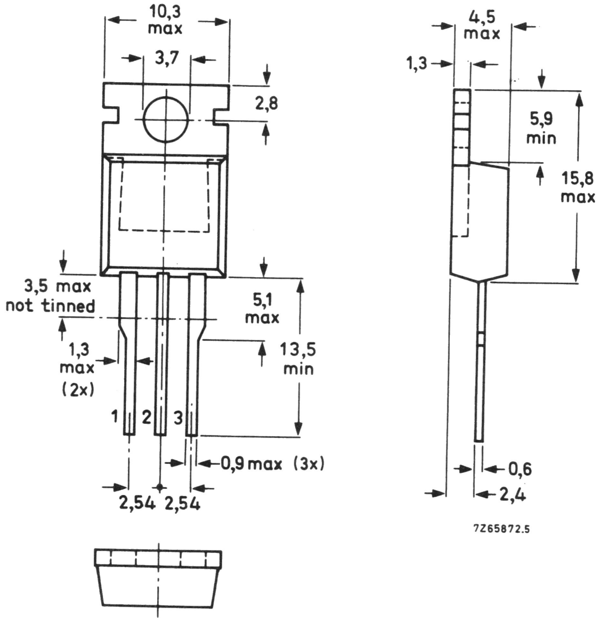

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	7,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	4,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	28	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,5 A	–	0,35	0,4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,5 A	2,2	3,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	450	600	pF
C_{oss}	Output capacitance		–	100	160	pF
C_{rss}	Feedback capacitance		–	50	80	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	7,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	28	A
V_{SD}	Diode forward on-voltage	I_F = 14 A; V_{GS} = 0 V	–	1,4	1,7	V
t_{rr}	Reverse recovery time	I_F = 7 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	200	–	ns
Q_{rr}	Reverse recovery charge		–	0,6	–	µC

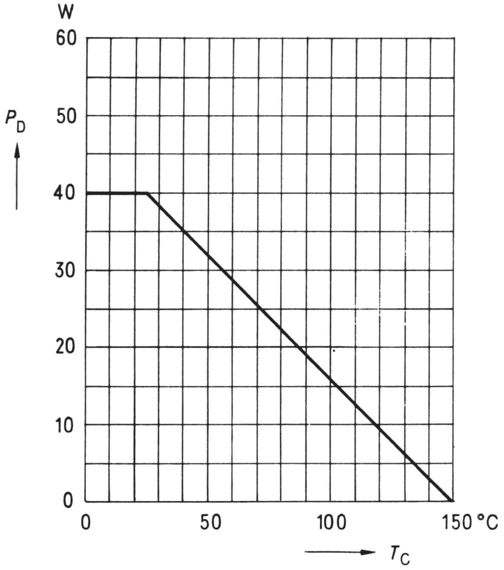


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

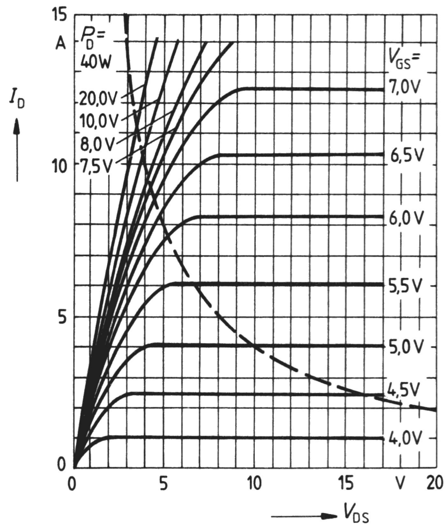


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

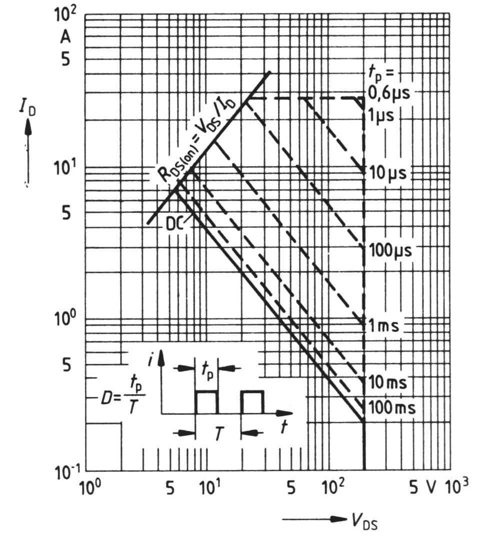


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

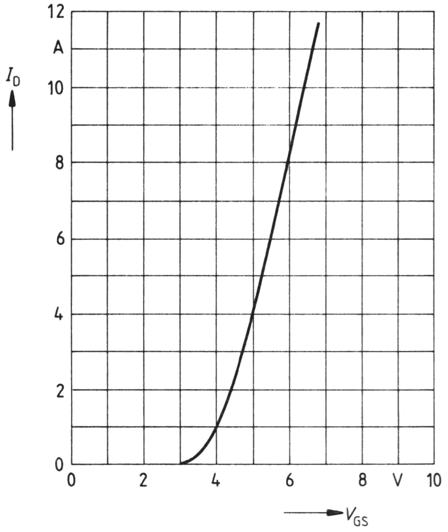


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

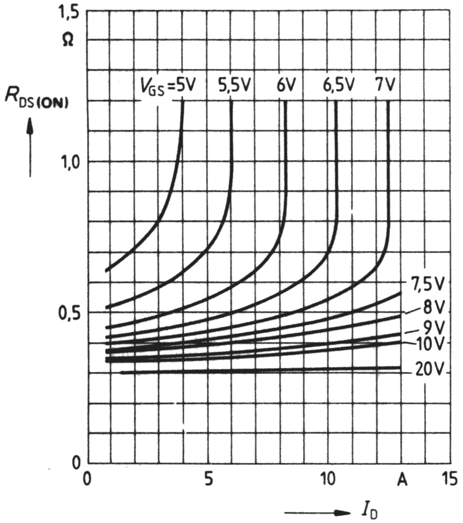


Fig.6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

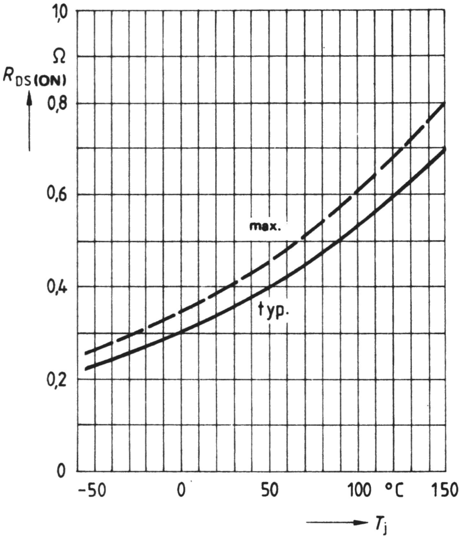


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 3,5 A; V_{GS} = 10 V.

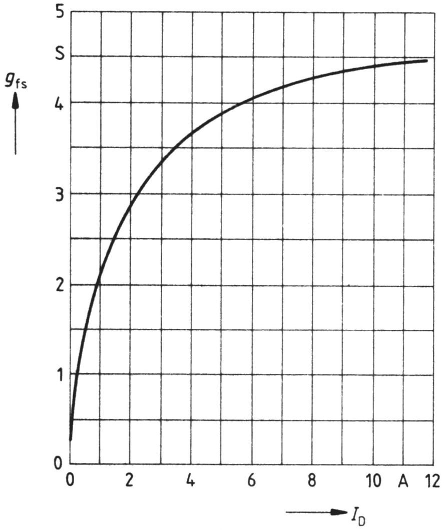


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

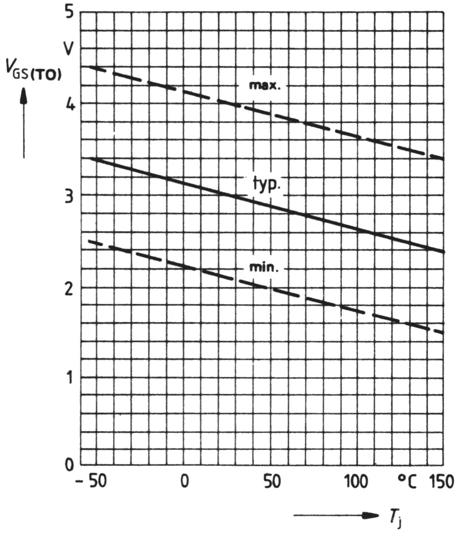


Fig.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

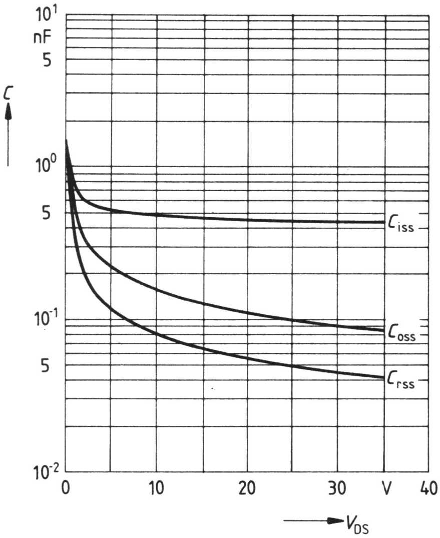


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

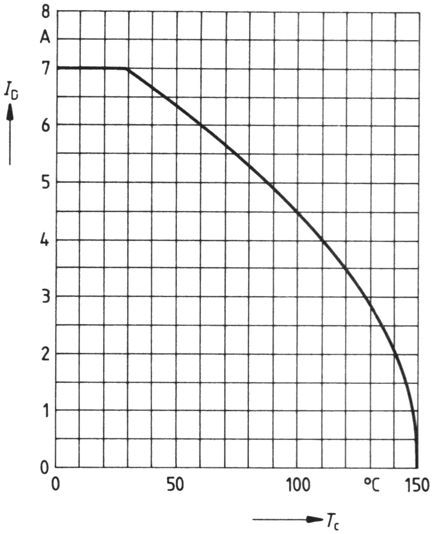


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

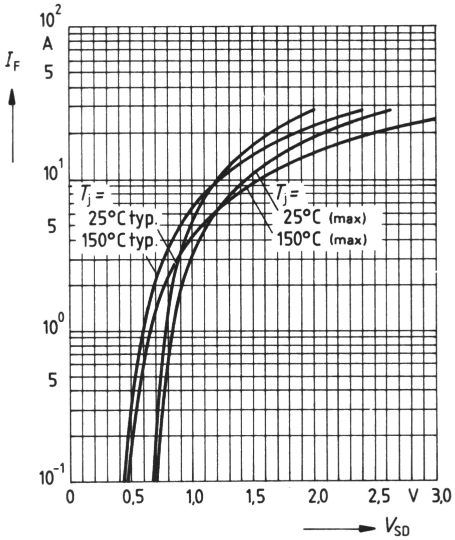


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

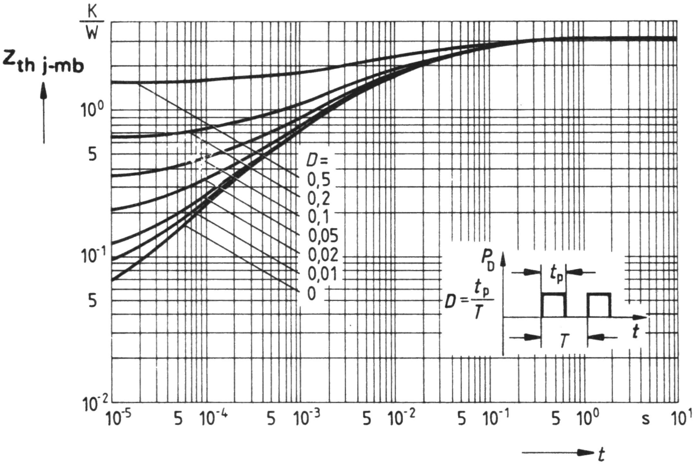


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

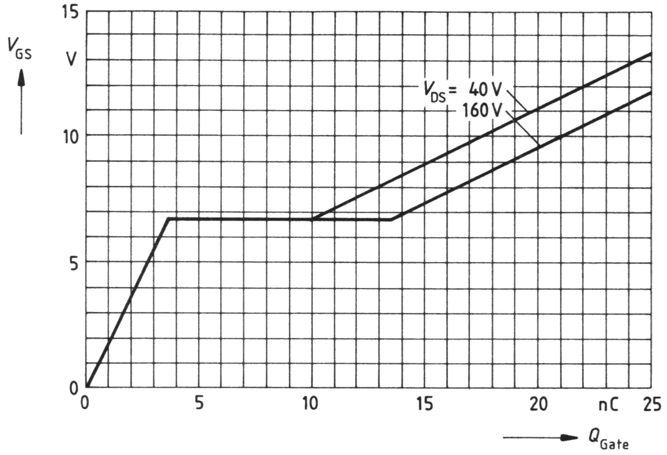


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 10{,}5$ A.

PowerMOS transistor BUZ73A

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

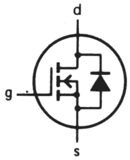
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	5,8	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,6	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



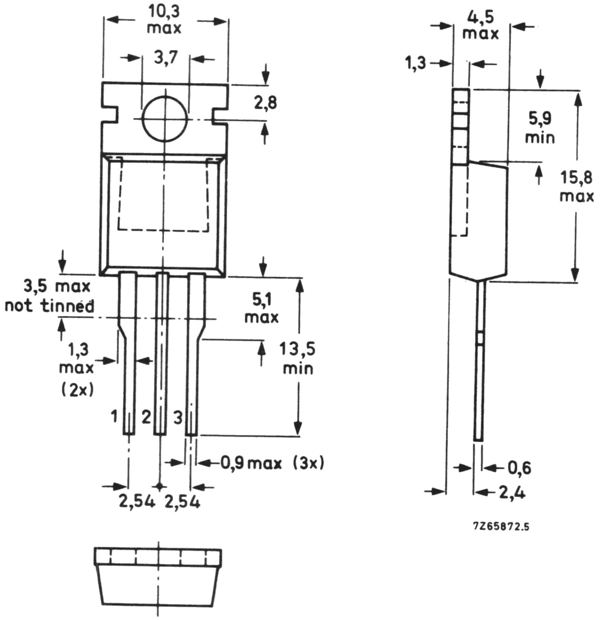

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	5,8	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	23	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,5 A	–	0,5	0,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,5 A	2,2	3,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	450	600	pF
C_{oss}	Output capacitance		–	100	160	pF
C_{rss}	Feedback capacitance		–	50	80	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	70	90	ns
t_f	Turn-off fall time		–	40	55	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	5,8	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	23	A
V_{SD}	Diode forward on-voltage	I_F = 11,6 A; V_{GS} = 0 V	–	1,4	1,7	V
t_{rr}	Reverse recovery time	I_F = 5,8 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	200	–	ns
Q_{rr}	Reverse recovery charge		–	0,6	–	μC

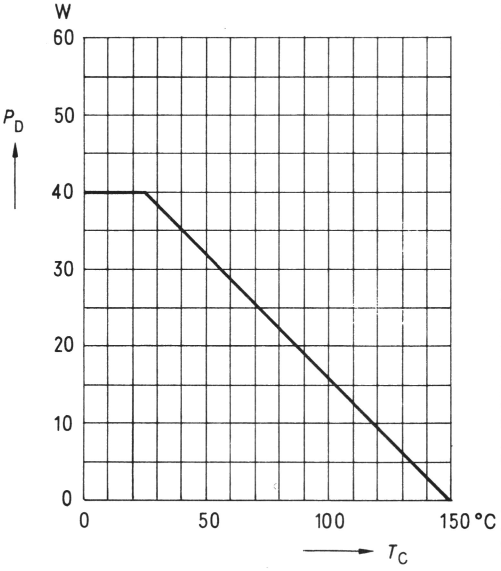


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

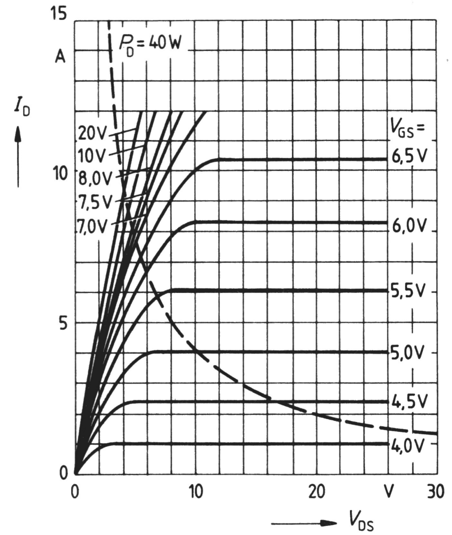


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

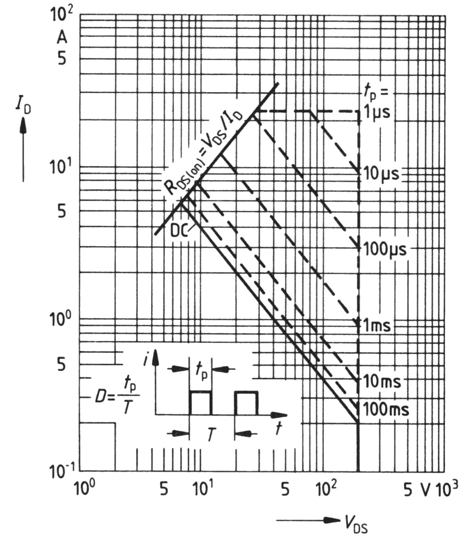


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

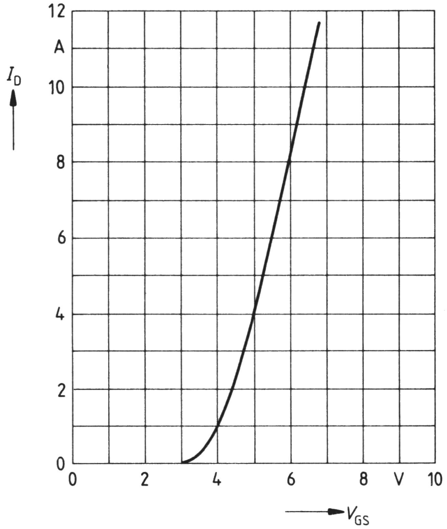


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

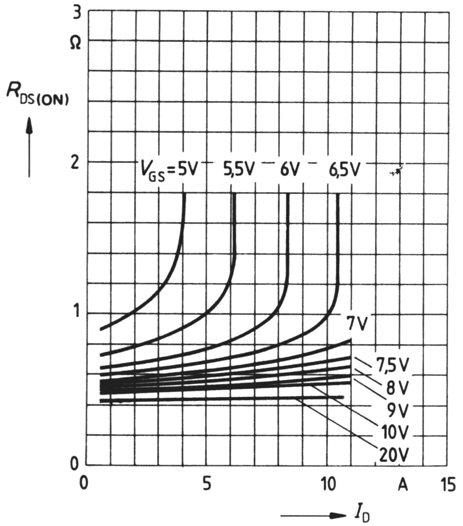


Fig. 6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

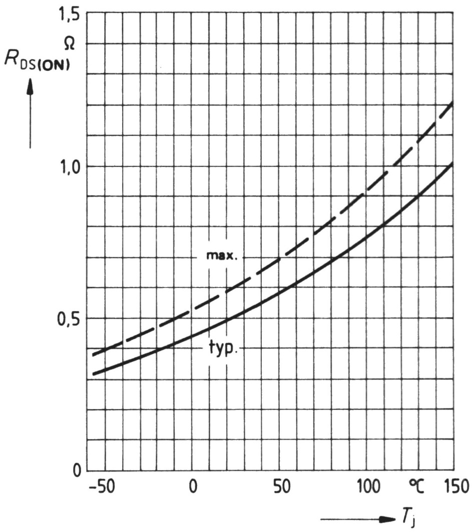


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 3{,}5$ A; $V_{GS} = 10$ V.

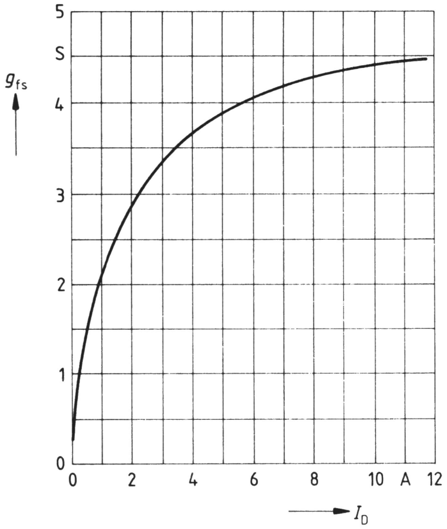


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

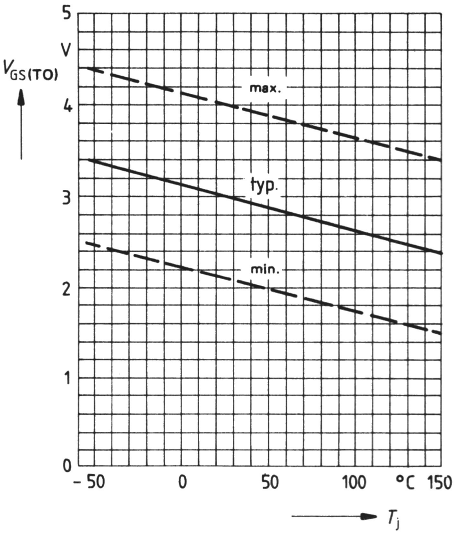


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

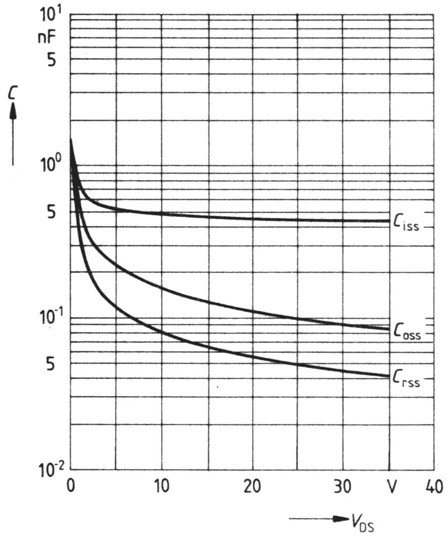


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

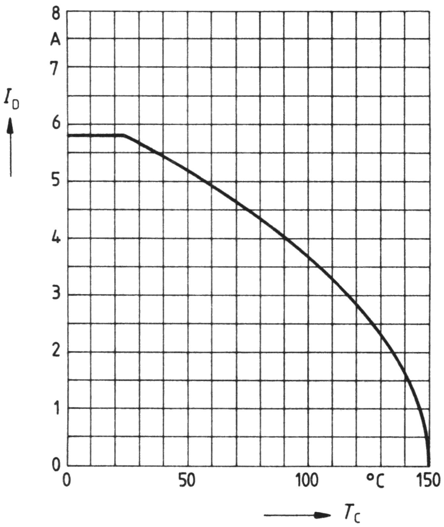


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

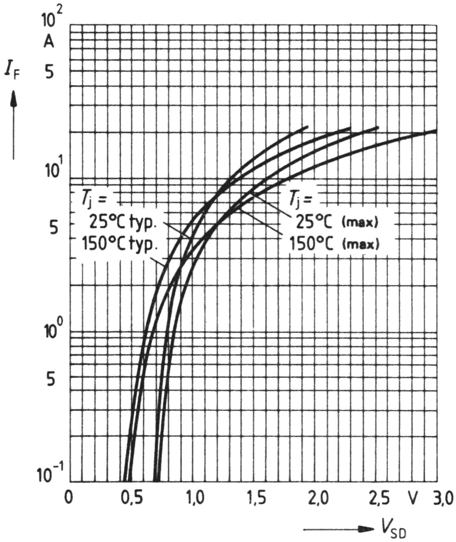


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

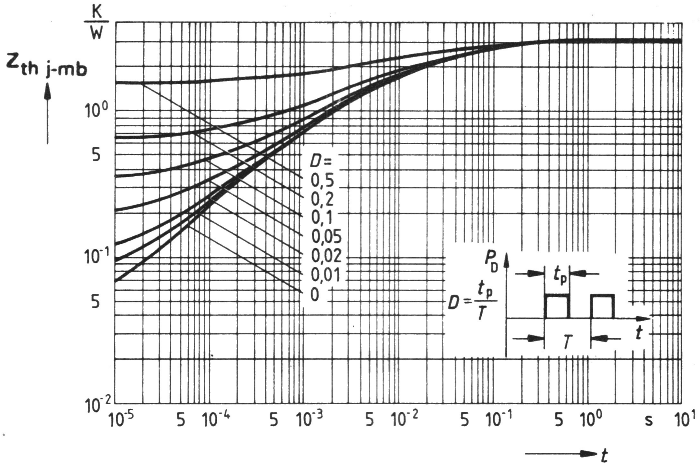


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

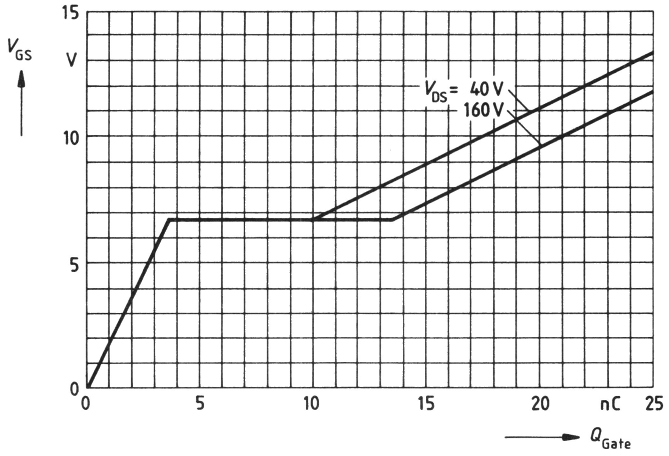


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 10{,}5$ A.

PowerMOS transistor BUZ60

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

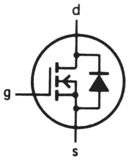
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	5,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



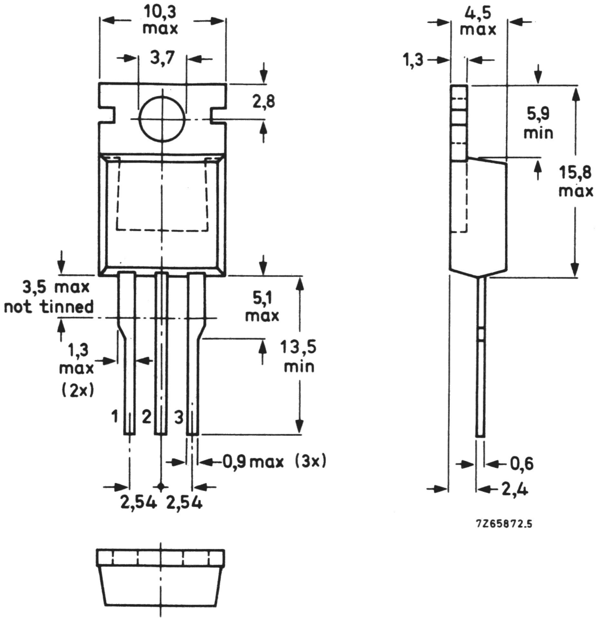

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	5,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	22	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,5 A	–	0,9	1,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,5 A	1,7	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	120	180	pF
C_{rss}	Feedback capacitance		–	35	60	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	65	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	22	A
V_{SD}	Diode forward on-voltage	I_F = 11 A; V_{GS} = 0 V	–	1,15	1,6	V
t_{rr}	Reverse recovery time	I_F = 5,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1000	–	ns
Q_{rr}	Reverse recovery charge		–	5,0	–	µC

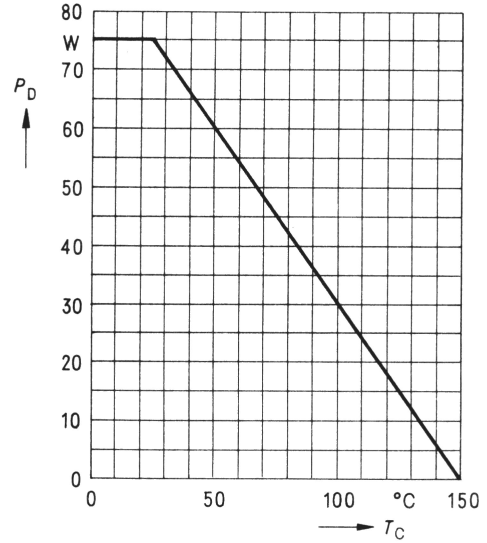


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

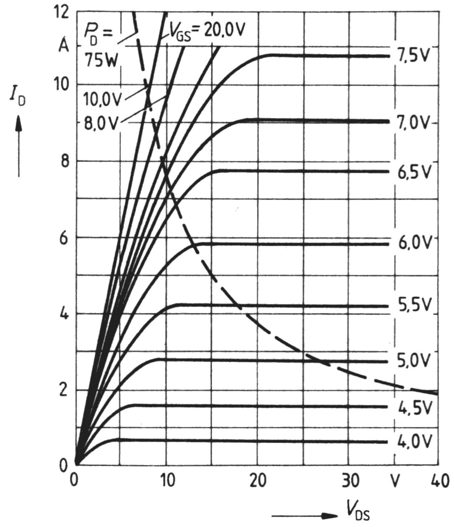


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

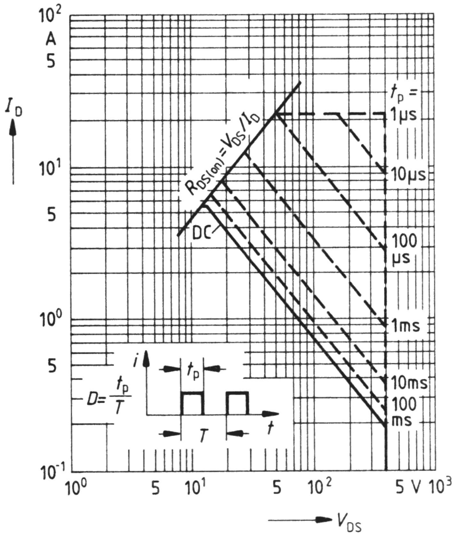


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

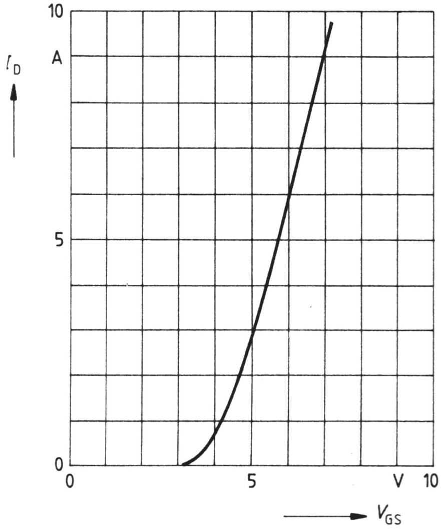


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

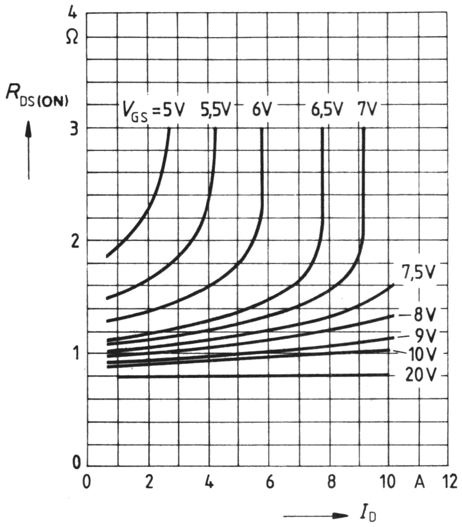


Fig. 6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$*
Parameter: V_{GS}; T_j = 25 °C.

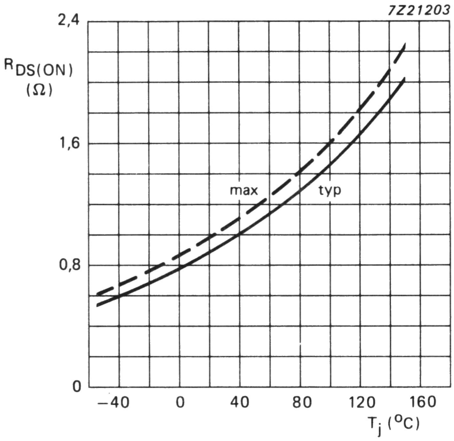


Fig. 7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$*
Conditions: I_D = 2,5 A; V_{GS} = 10 V.

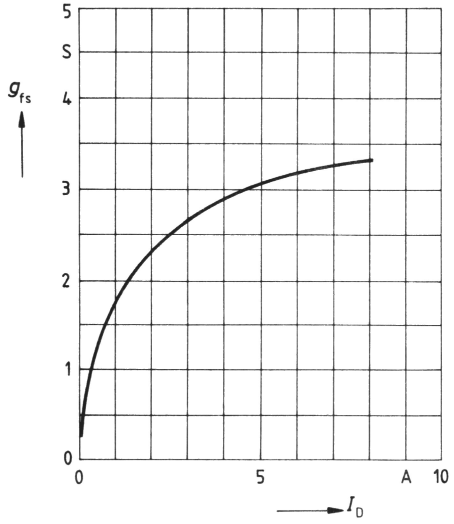


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

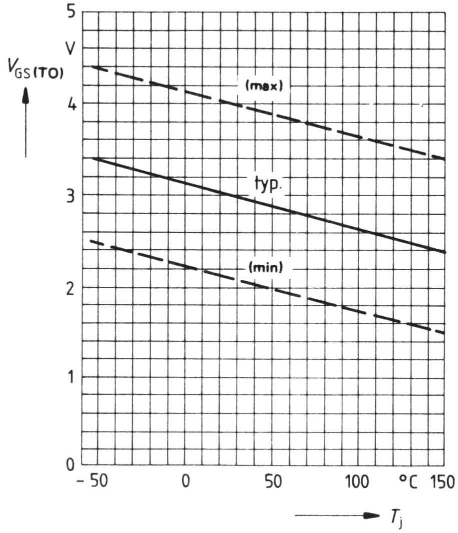


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

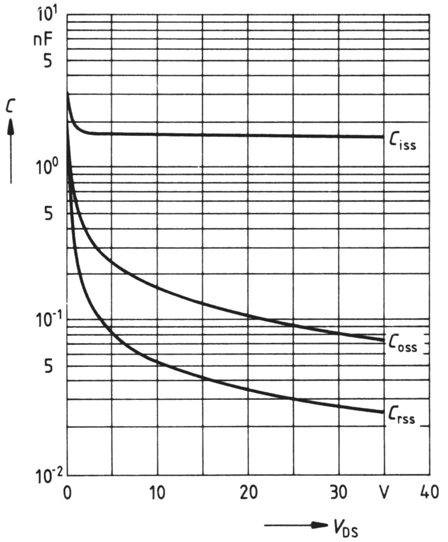


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

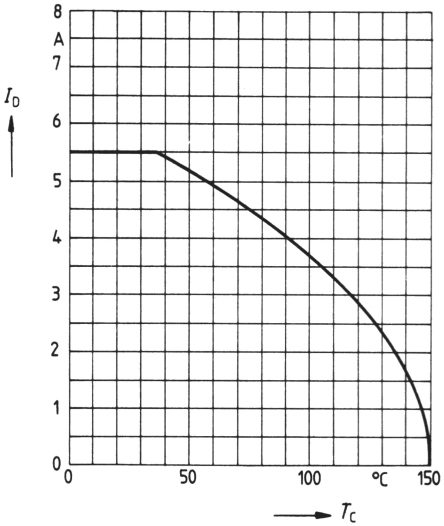


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

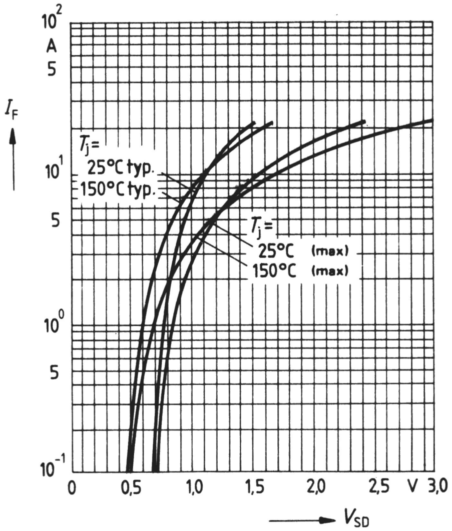


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

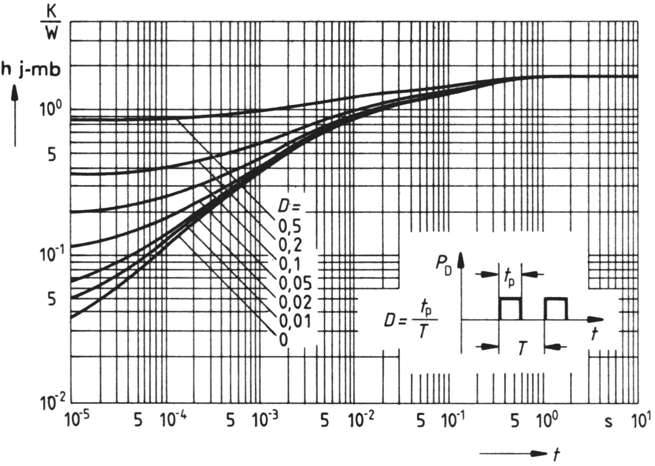


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

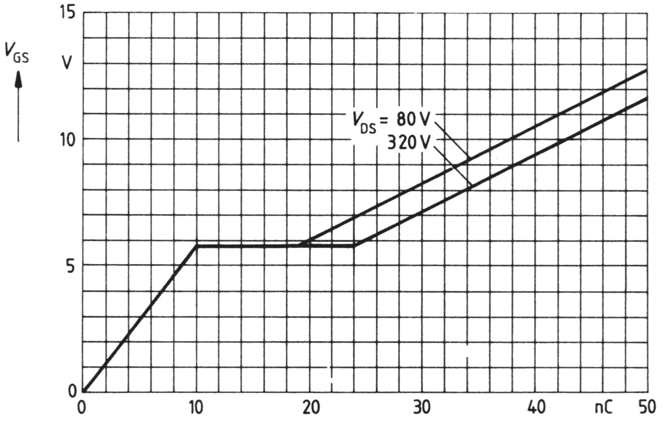


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 8{,}3$ A.

PowerMOS transistor BUZ76

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

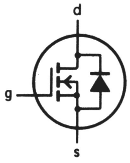
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	3,0	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,8	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



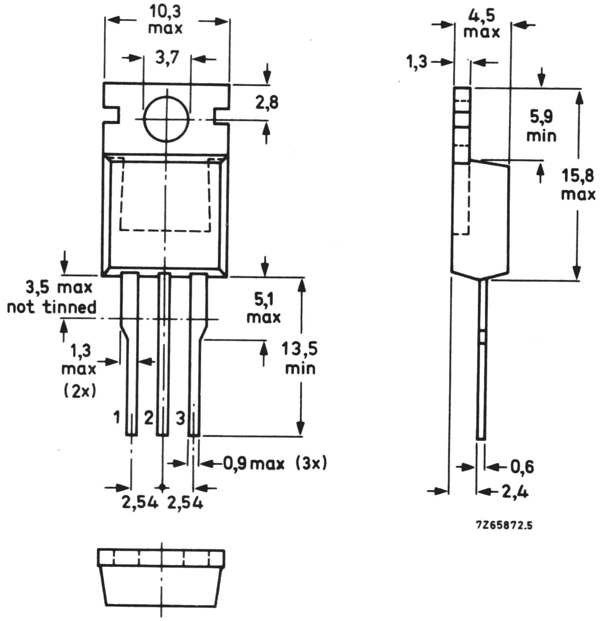

10,3
max
3,7
2,8
4,5
max
1,3
5,9
min
15,8
max
3,5 max
not tinned
5,1
max
13,5
min
1,3
max
(2x)
1
2
3
0,9 max (3x)
2,54 2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	3,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	1,65	1,8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	2,1	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	300	500	pF
C_{oss}	Output capacitance		–	50	80	pF
C_{rss}	Feedback capacitance		–	35	60	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	50	65	ns
t_f	Turn-off fall time		–	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	3,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	12	A
V_{SD}	Diode forward on-voltage	I_F = 6 A; V_{GS} = 0 V	–	1,1	1,4	V
t_{rr}	Reverse recovery time	I_F = 3 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	300	–	ns
Q_{rr}	Reverse recovery charge		–	2,5	–	µC

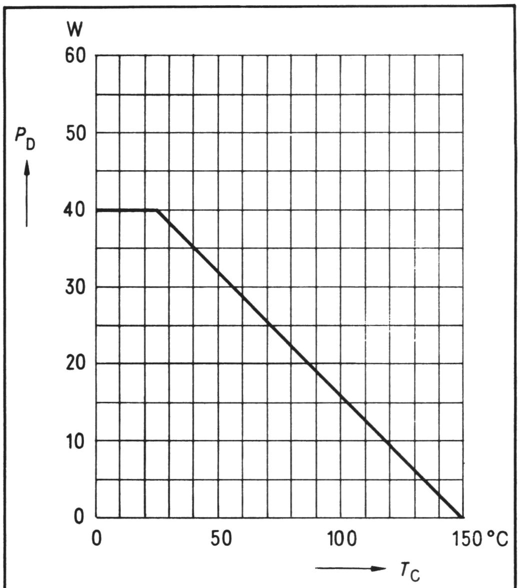


Fig.2 Power dissipation $P_D = f(T_{mb})$.

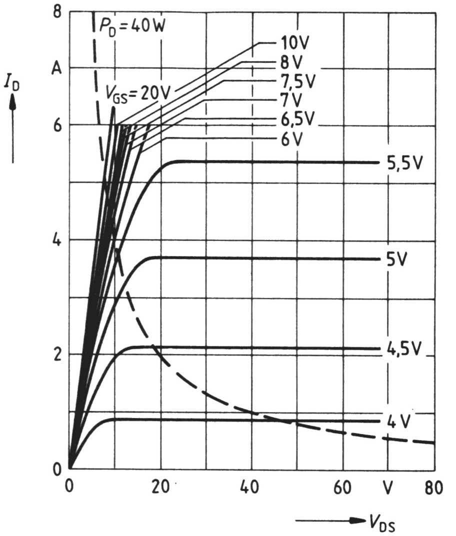


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25\ °C$.

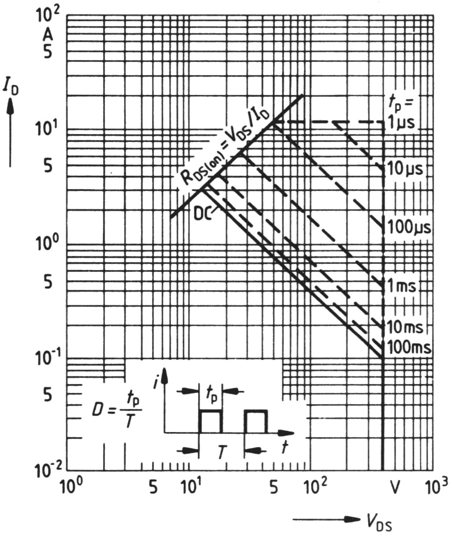


Fig.4 Safe operating area $I_D(DC)$ and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\ °C$.

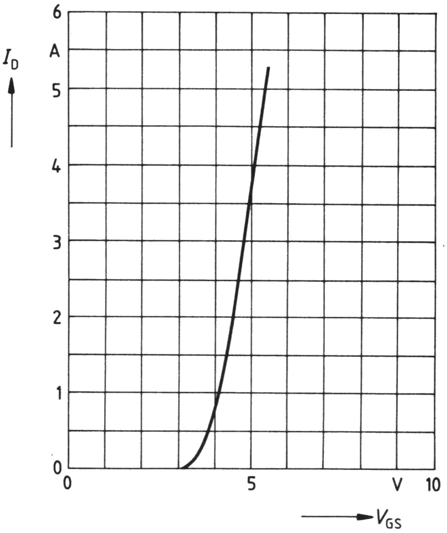


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25\ °C$.

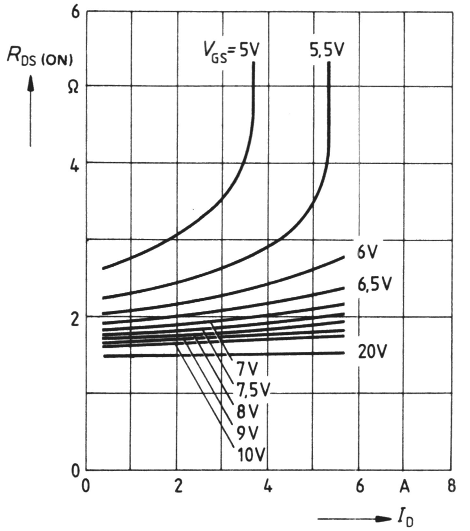


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

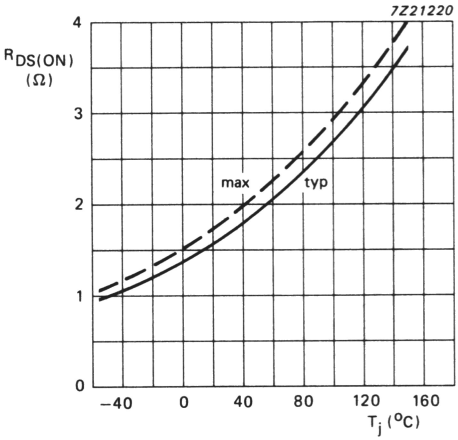


Fig.7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 1,5 A; V_{GS} = 10 V.

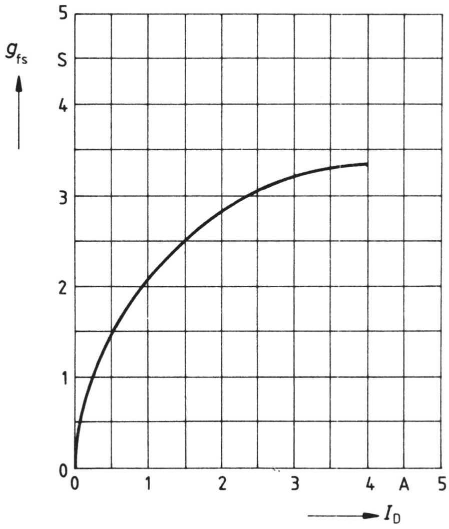


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

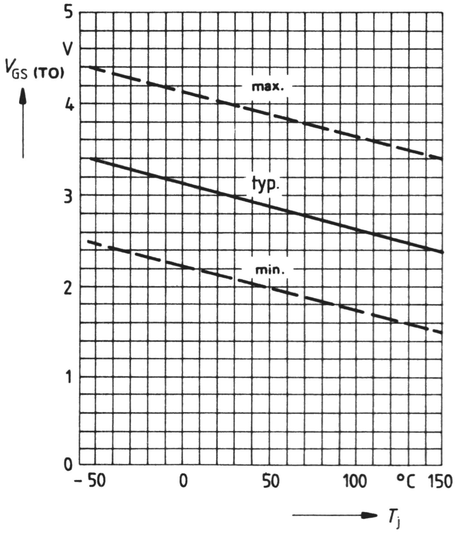


Fig.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

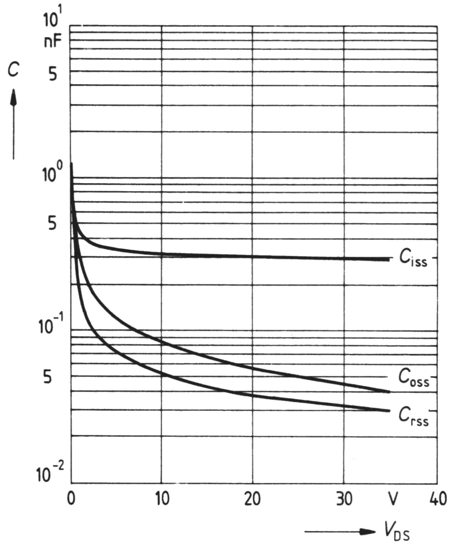


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

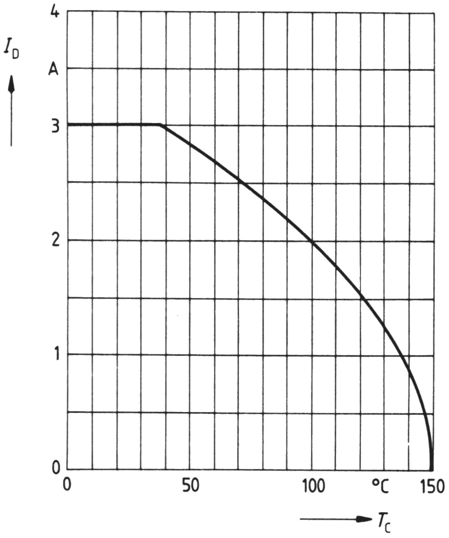


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

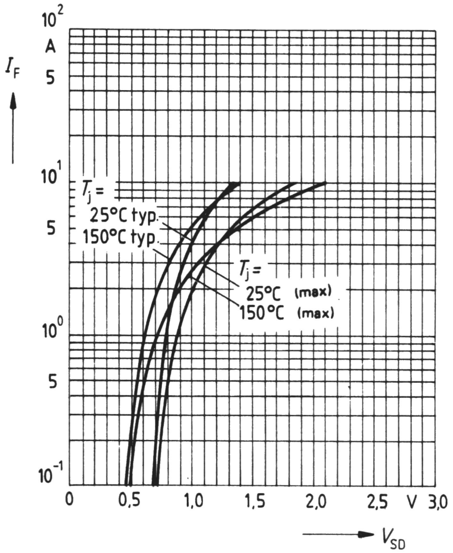


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

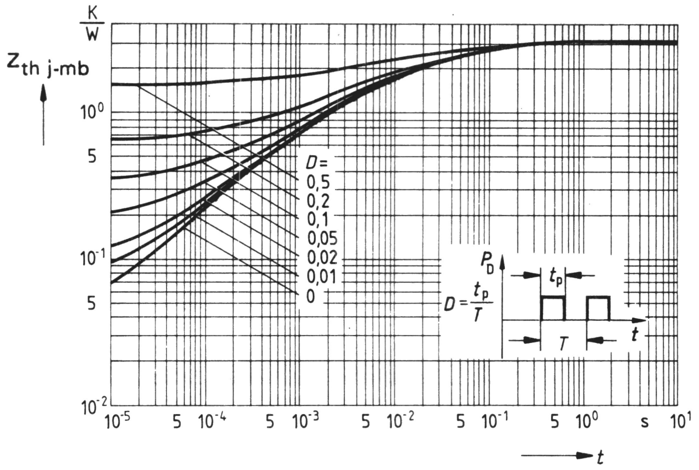


*Fig. 13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.*

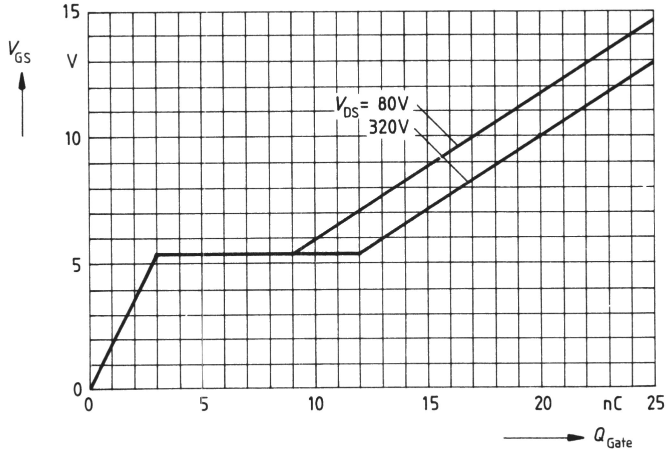


*Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 4{,}5$ A.*

PowerMOS transistor BUZ76A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

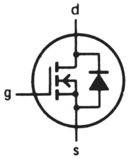
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	2,6	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



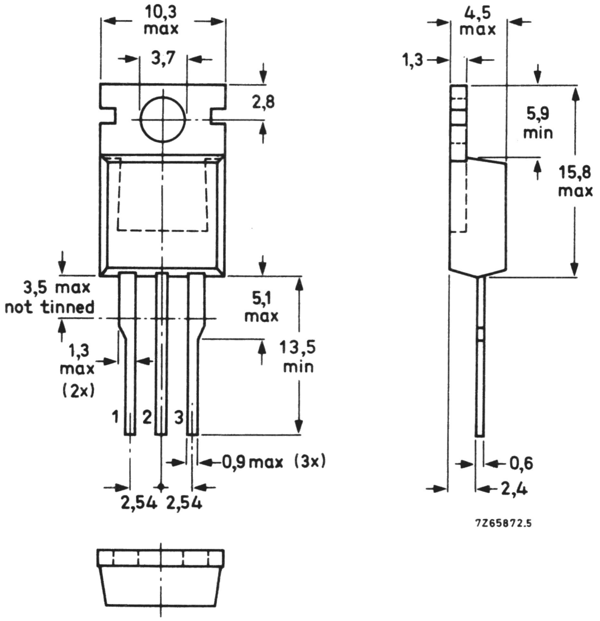

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,6	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	2,2	2,5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	2,1	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	300	500	pF
C_{oss}	Output capacitance		–	50	80	pF
C_{rss}	Feedback capacitance		–	35	60	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,4 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	50	65	ns
t_f	Turn-off fall time		–	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,6	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5,2 A; V_{GS} = 0 V	–	1,1	1,4	V
t_{rr}	Reverse recovery time	I_F = 2,6 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	300	–	ns
Q_{rr}	Reverse recovery charge		–	2,5	–	μC

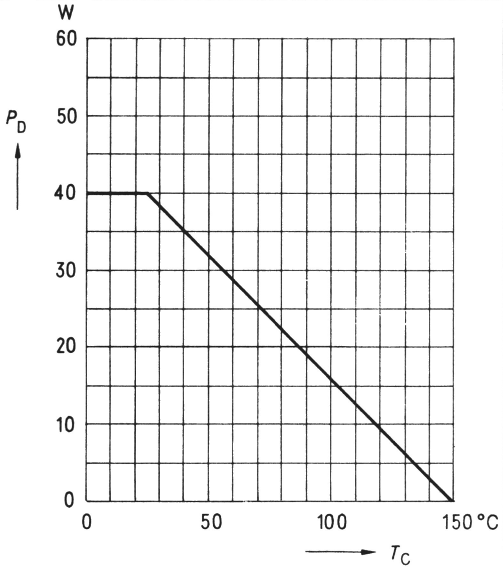


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

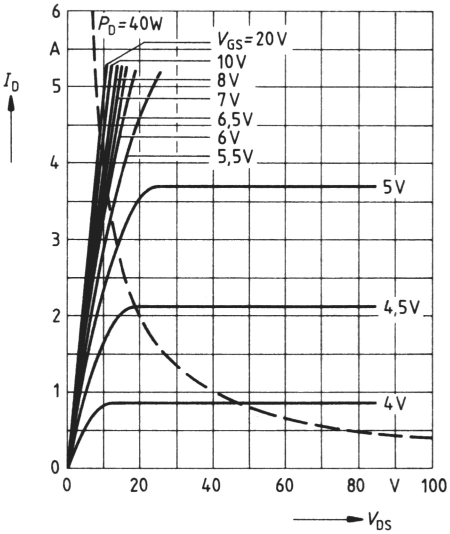


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

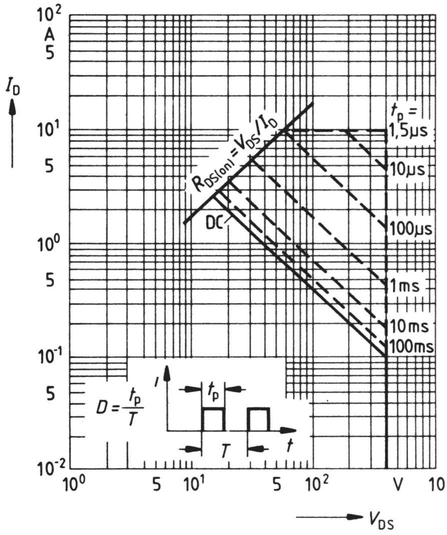


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

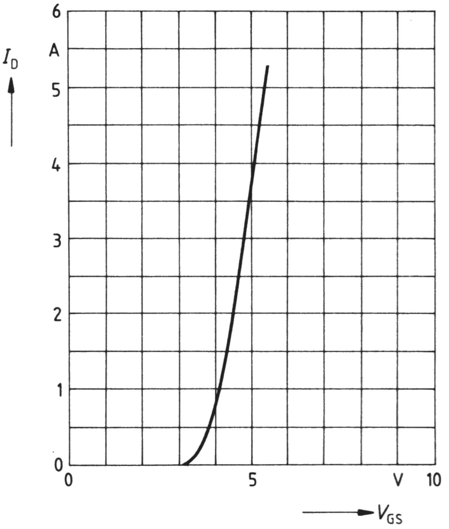


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

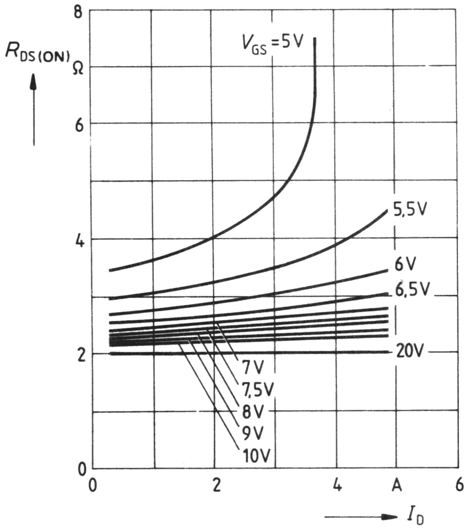


Fig. 6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

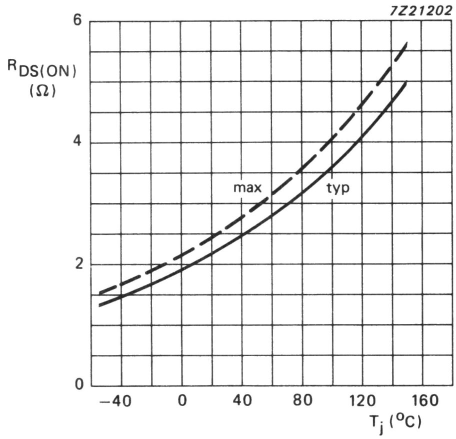


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

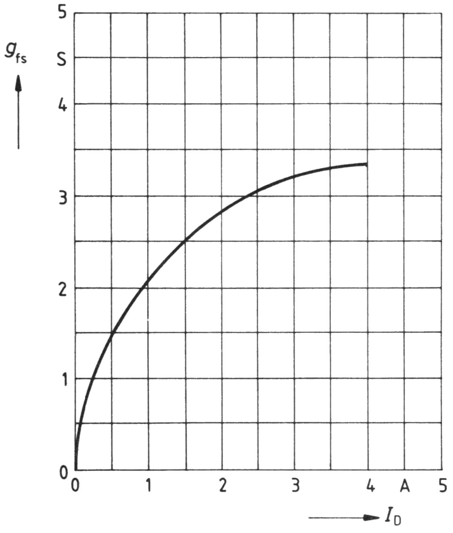


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

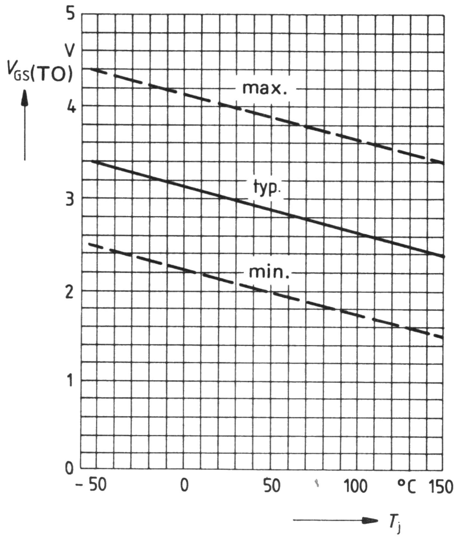


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

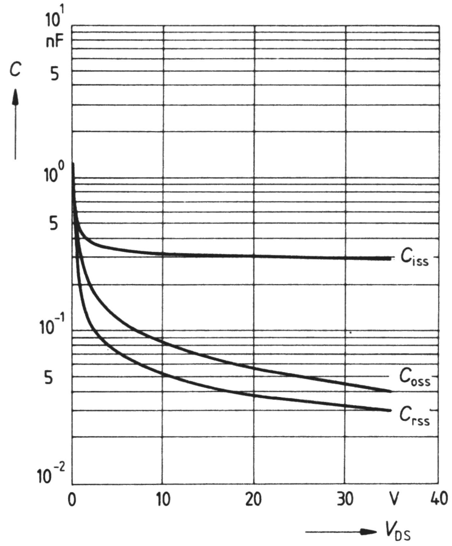


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

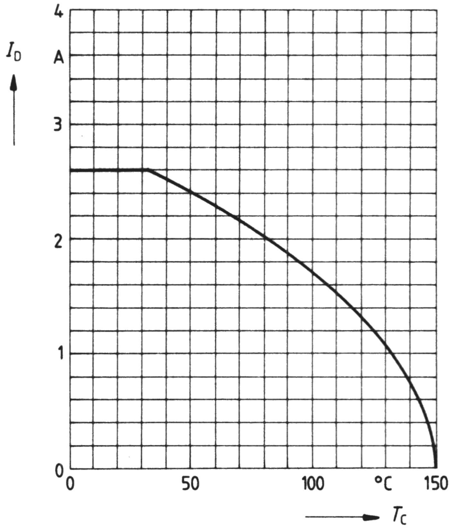


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

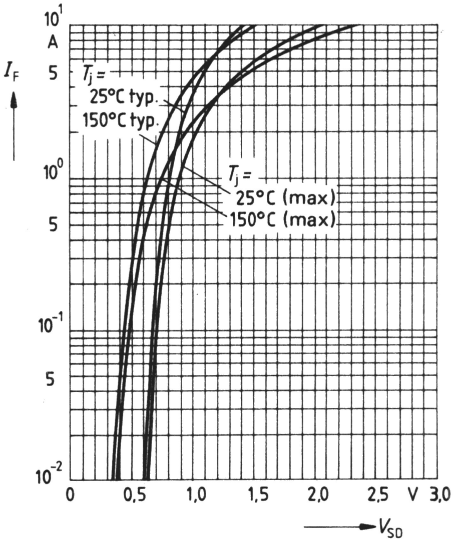


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

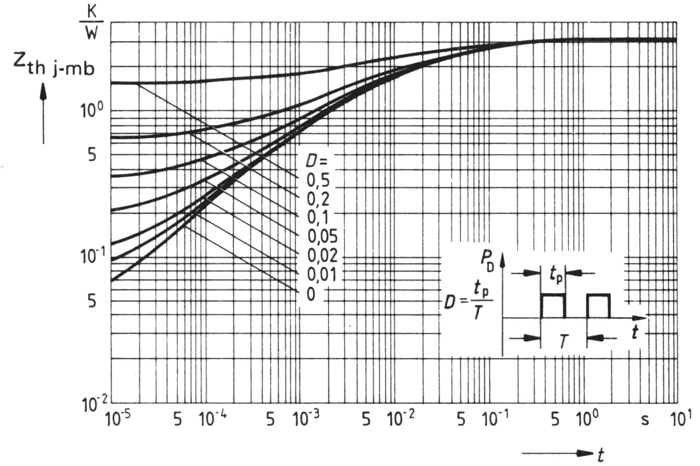


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

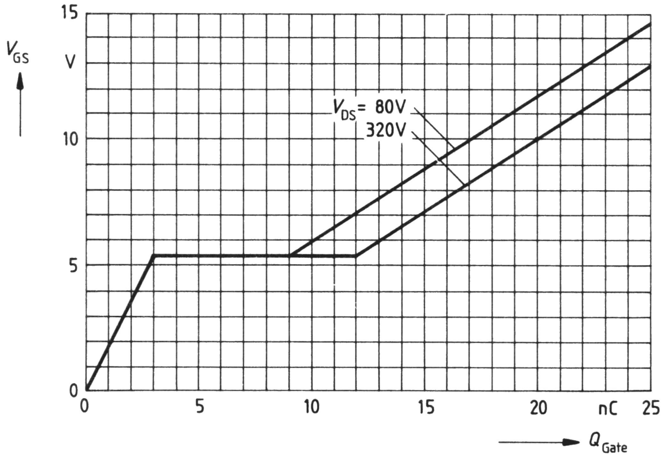


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 4,5 A.

PowerMOS transistor BUZ41A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

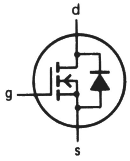
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	4,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



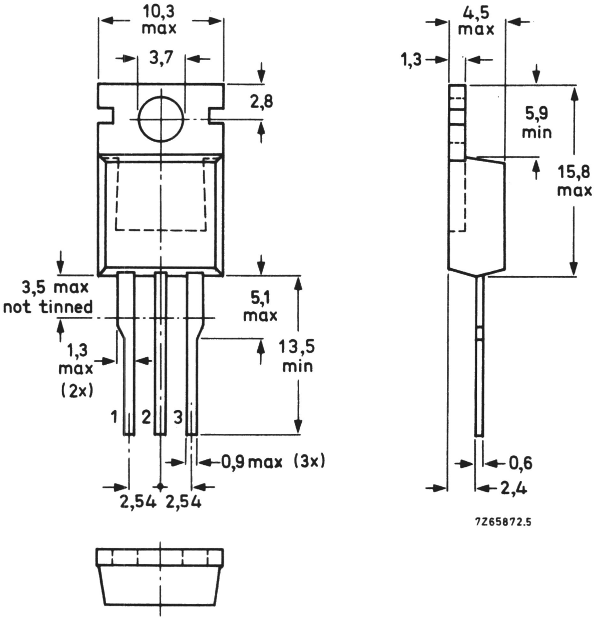

10,3 max
3,7
2,8
3,5 max not tinned
1,3 max (2x)
5,1 max
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	4,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,0	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	18	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,5 A	–	1,4	1,5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,5 A	1,5	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	110	170	pF
C_{rss}	Feedback capacitance		–	40	70	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,6 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	65	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	4,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	18	A
V_{SD}	Diode forward on-voltage	I_F = 9 A; V_{GS} = 0 V	–	1,1	1,5	V
t_{rr}	Reverse recovery time	I_F = 4,5 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	1200	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	μC

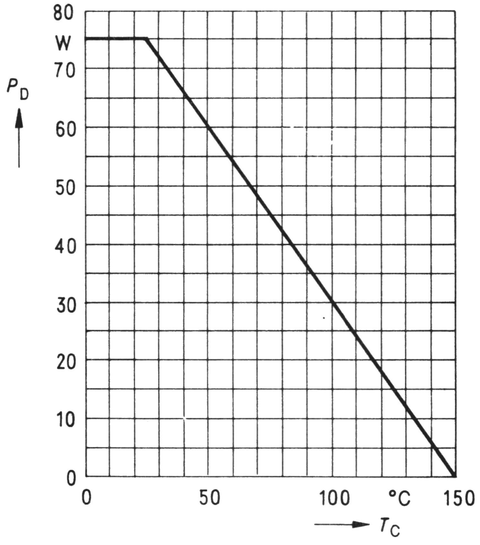


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

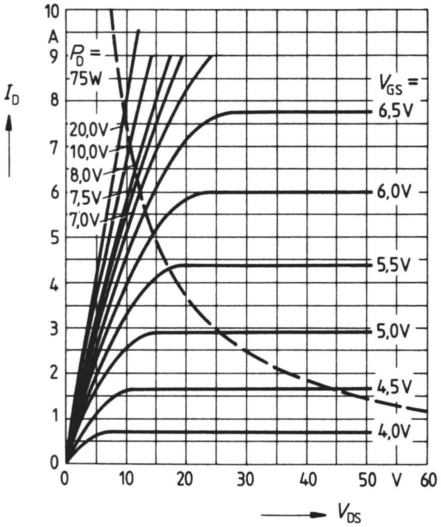


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

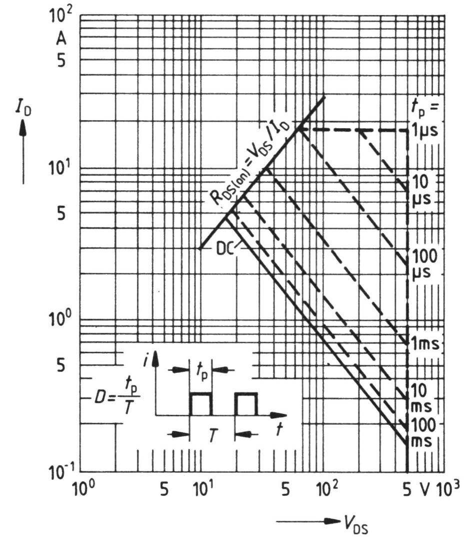


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

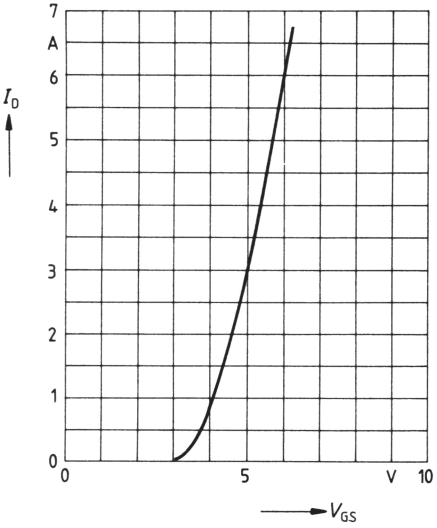


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

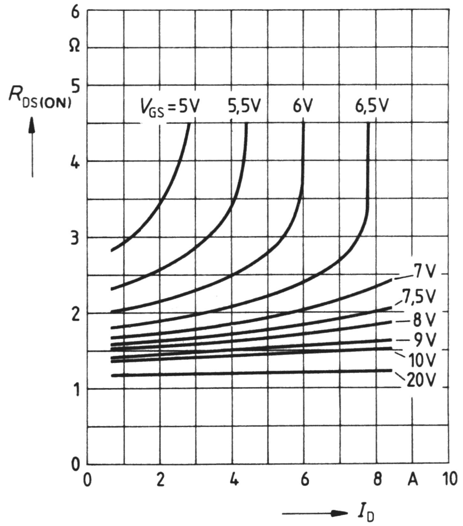


Fig. 6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; T_j = 25 °C.

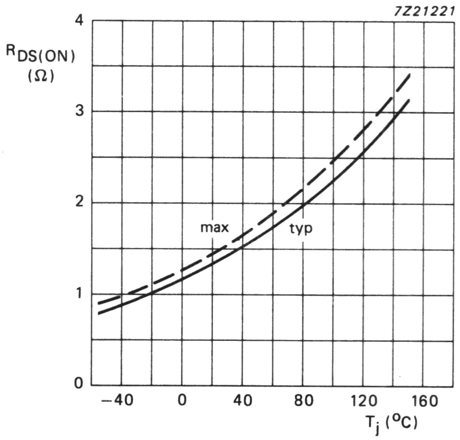


Fig. 7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* I_D = 2,5 A; V_{GS} = 10 V.

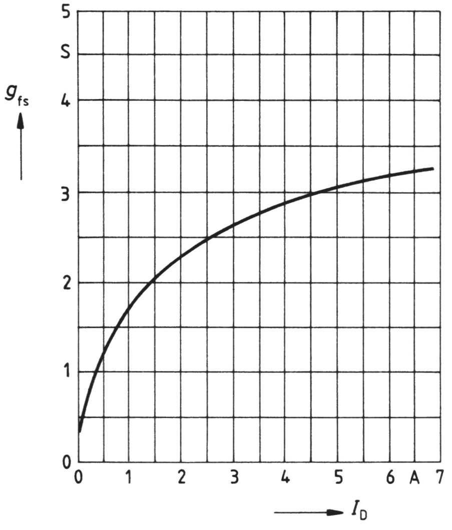


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions:* 80 μs pulse test; V_{DS} = 25 V; T_j = 25 °C.

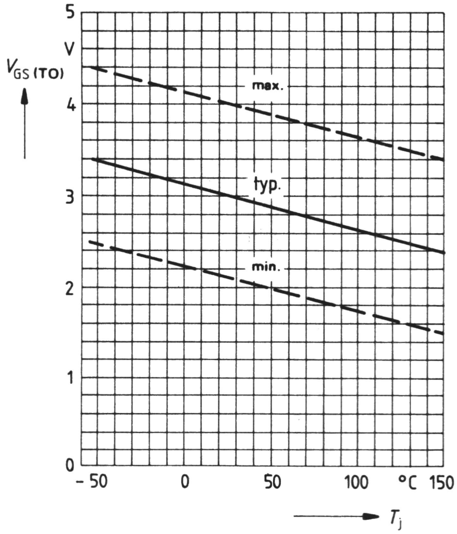


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; I_D = 1 mA.

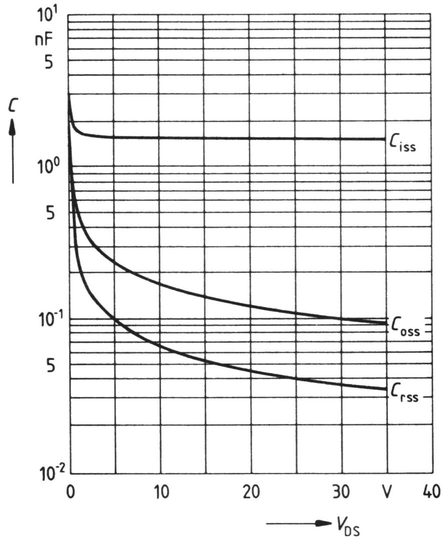


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

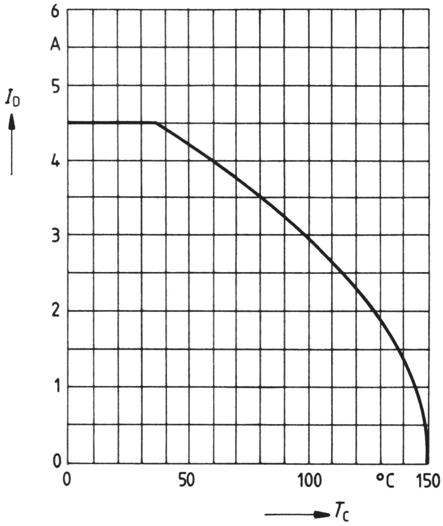


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

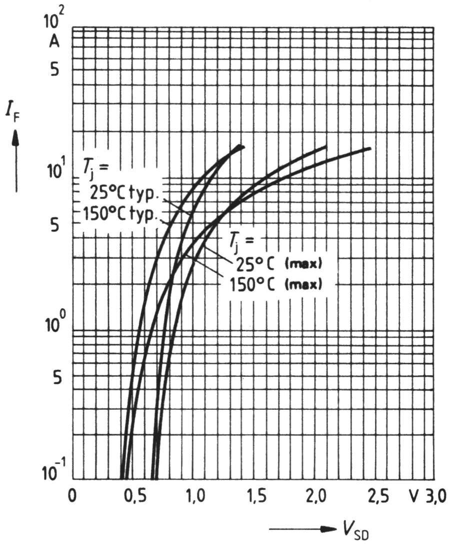


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

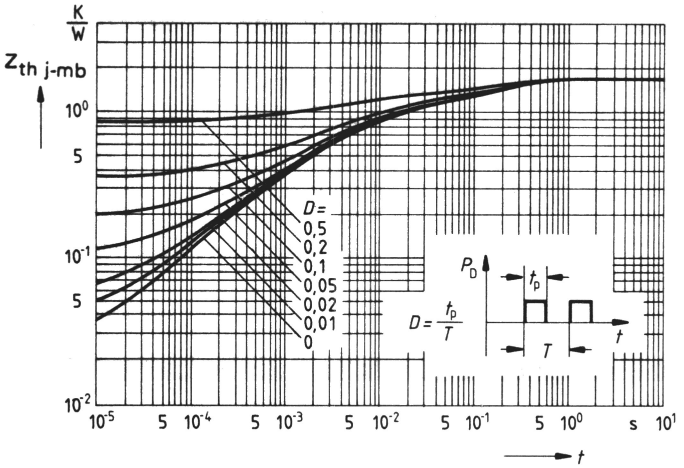


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

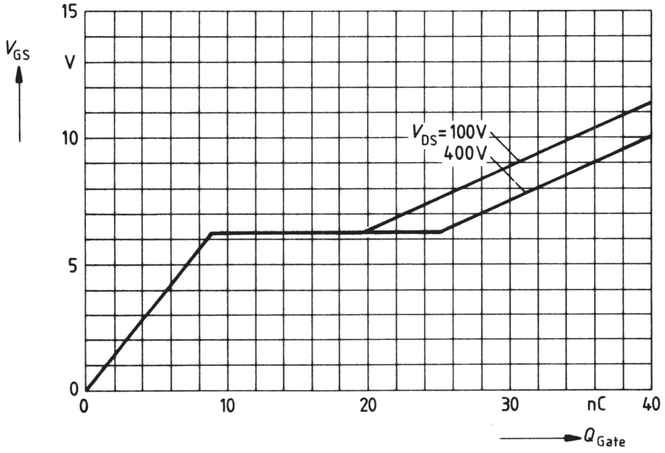


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 6,8 A.

PowerMOS transistor BUZ42

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

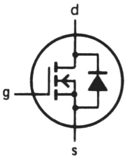
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	4,0	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



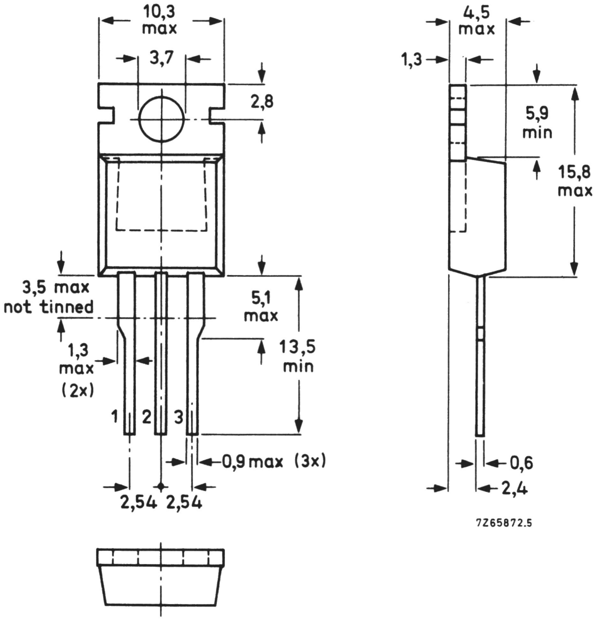

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	4,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	16	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,5 A	–	1,6	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,5 A	1,5	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	110	170	pF
C_{rss}	Feedback capacitance		–	40	70	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	65	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	4,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	16	A
V_{SD}	Diode forward on-voltage	I_F = 8 A; V_{GS} = 0 V	–	1,1	1,5	V
t_{rr}	Reverse recovery time	I_F = 4 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	1200	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	μC

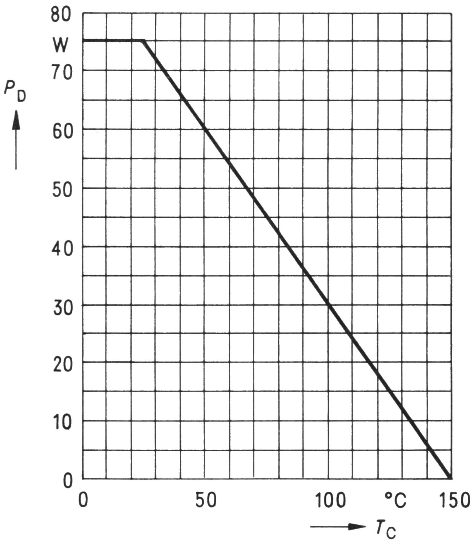


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

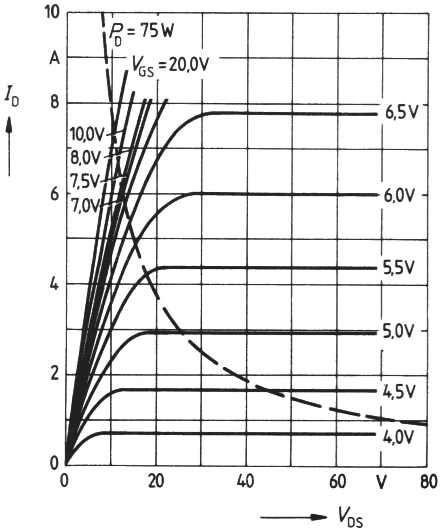


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

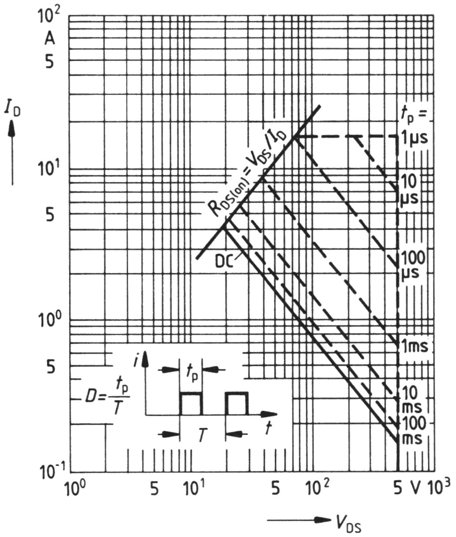


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

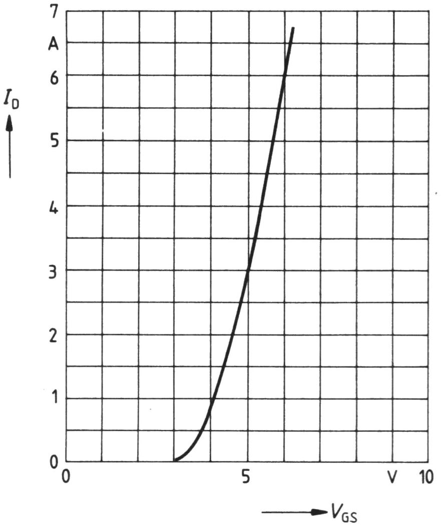


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

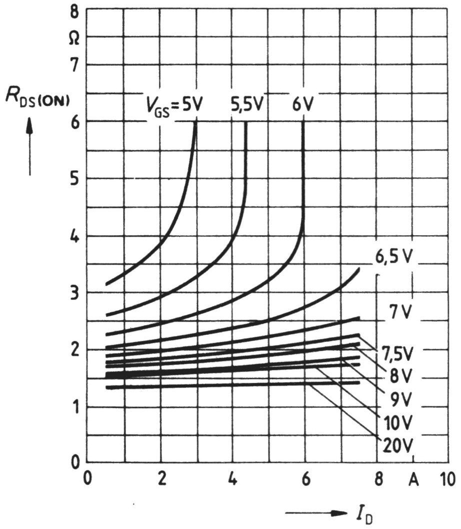


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

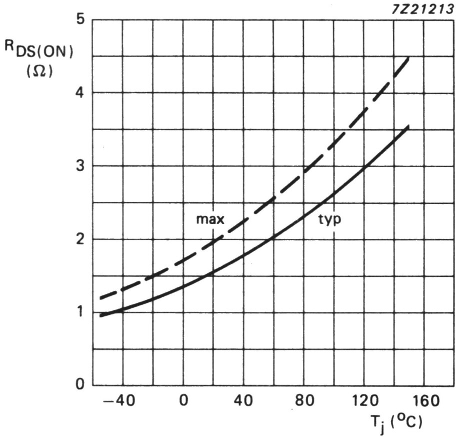


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 2,5 A; V_{GS} = 10 V.

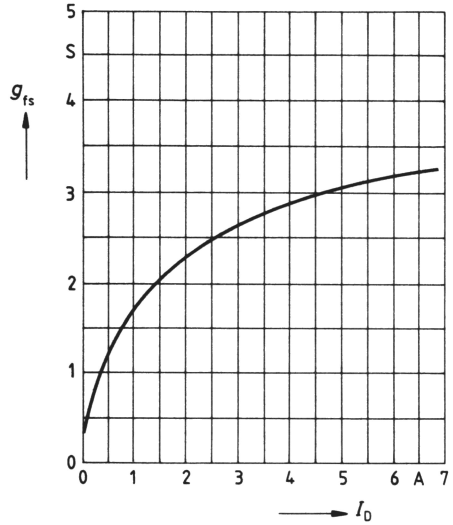


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

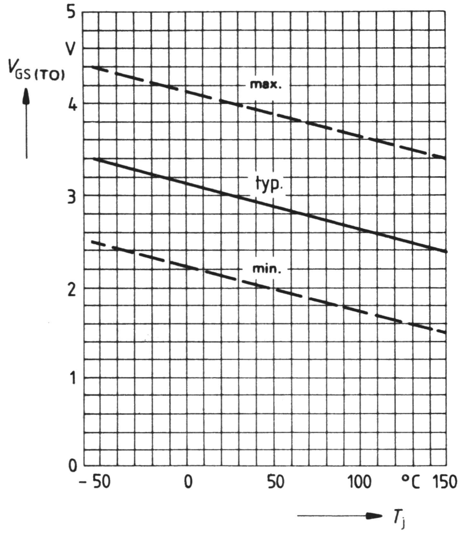


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

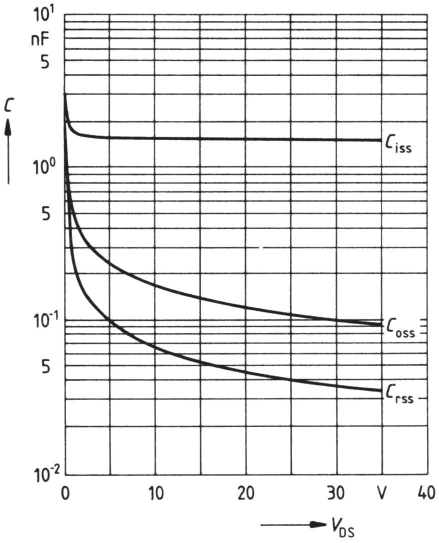


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

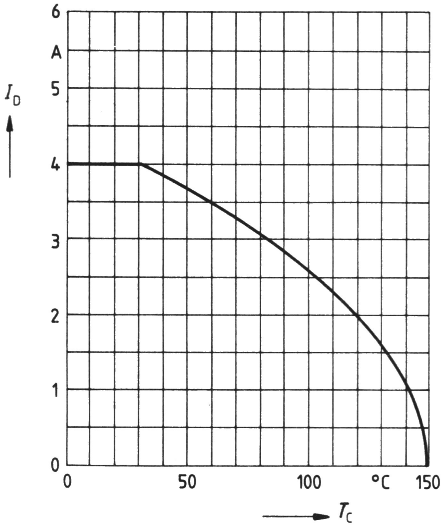


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

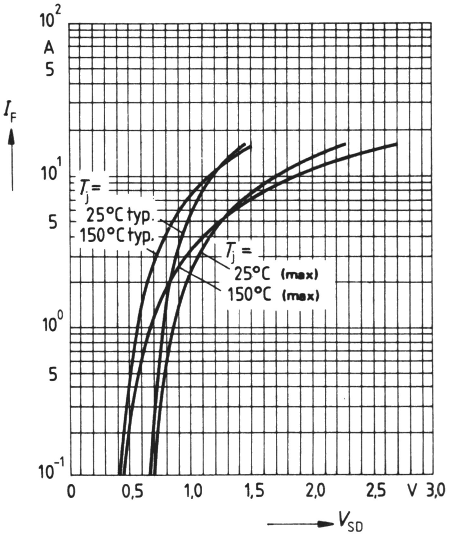


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

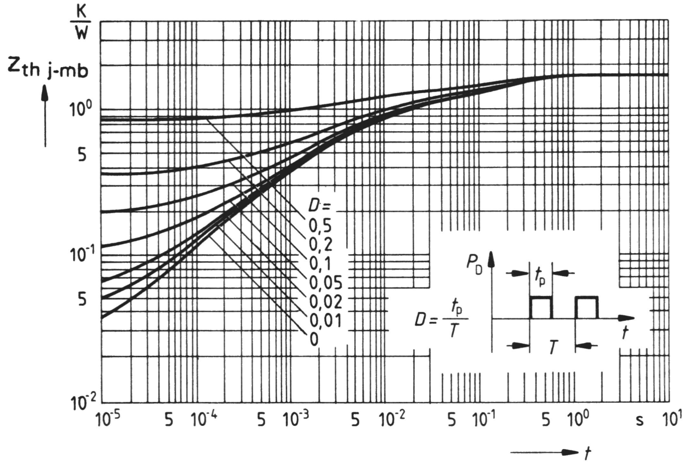


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

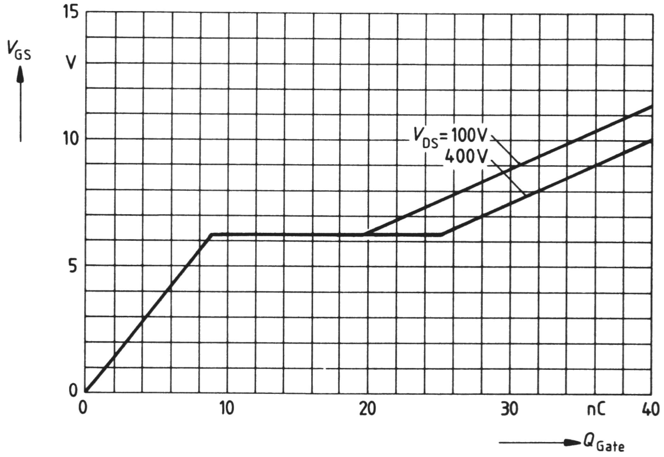


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 6{,}8$ A.

PowerMOS transistor BUZ74

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

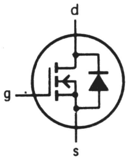
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	2,4	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	3,0	Ω

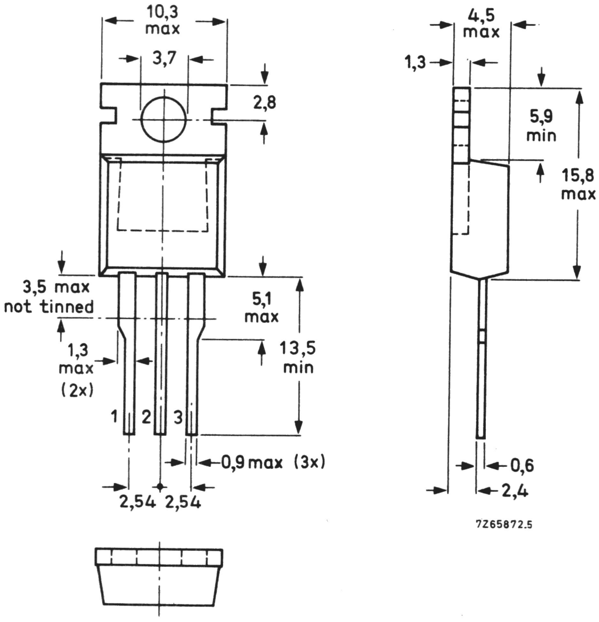
MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source





10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,4	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	9,5	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,2 A	–	2,6	3,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,2 A	1,9	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	300	500	pF
C_{oss}	Output capacitance		–	50	80	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	50	65	ns
t_f	Turn-off fall time		–	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,4	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	9,5	A
V_{SD}	Diode forward on-voltage	I_F = 4,8 A; V_{GS} = 0 V	–	1,0	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,4 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	350	–	ns
Q_{rr}	Reverse recovery charge		–	3,5	–	µC

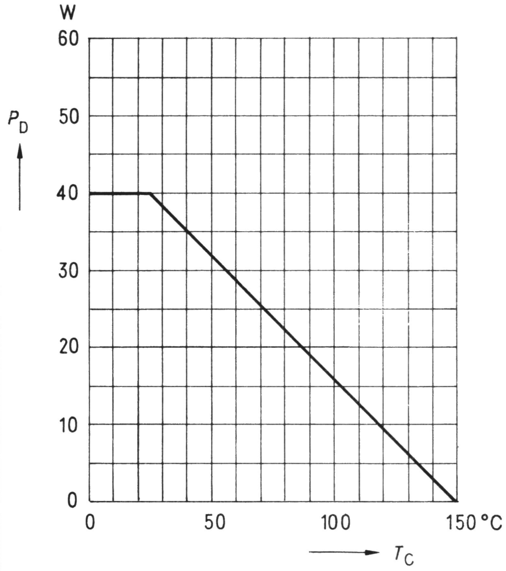


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

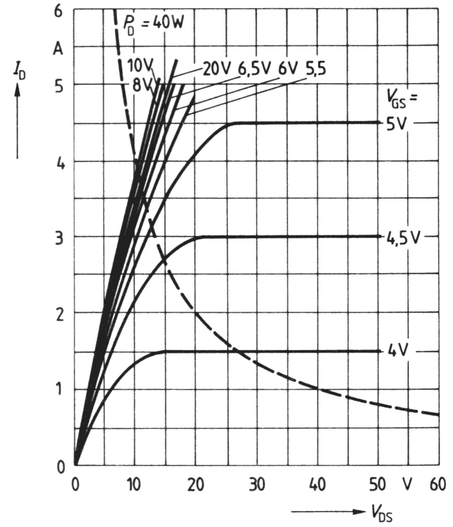


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

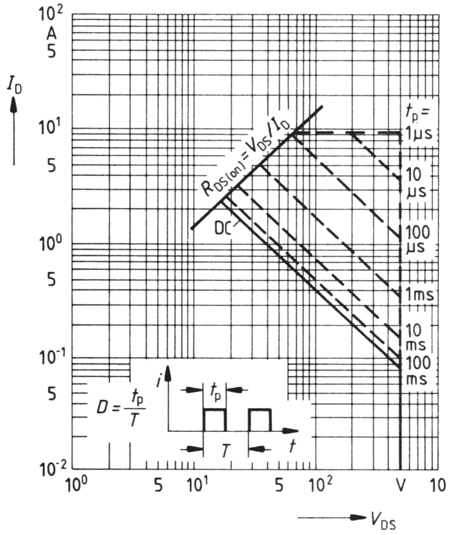


Fig. 4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; $T_{mb} = 25$ °C.

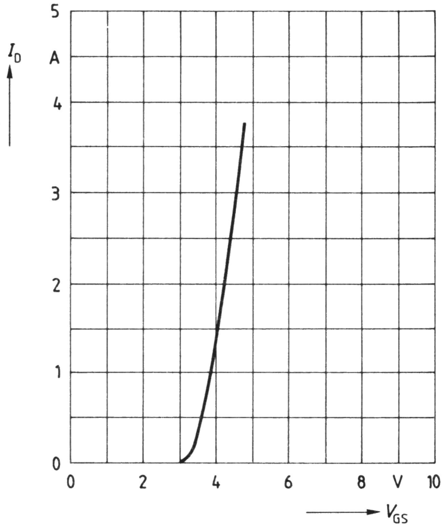


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

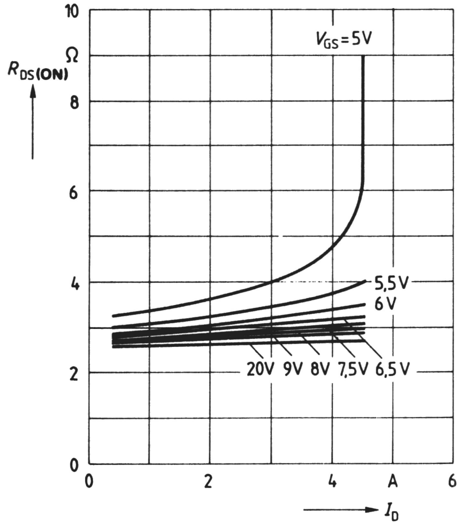


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

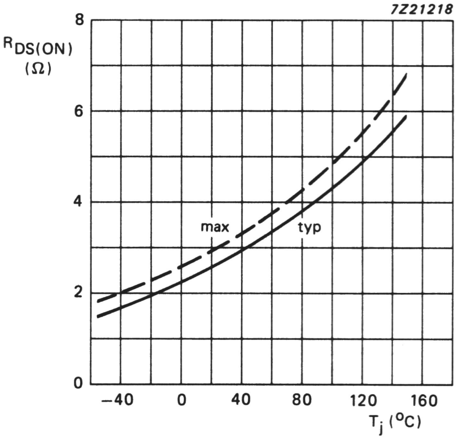


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}2$ A; $V_{GS} = 10$ V.

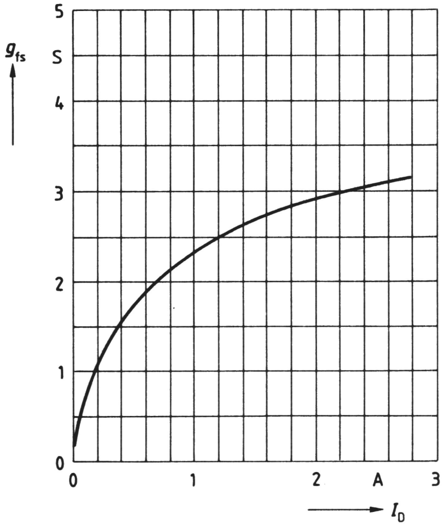


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

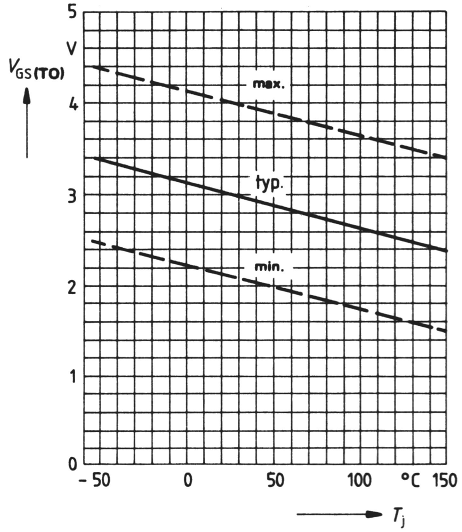


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

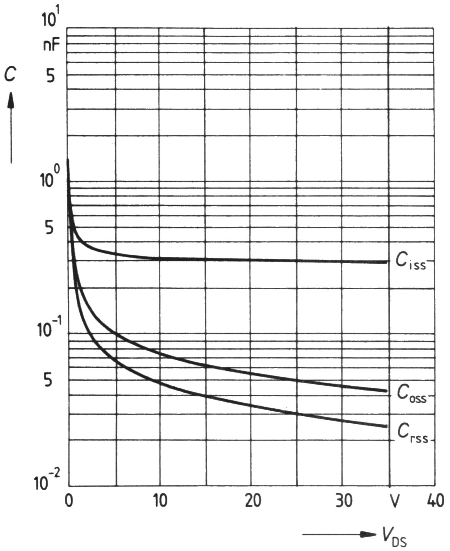


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

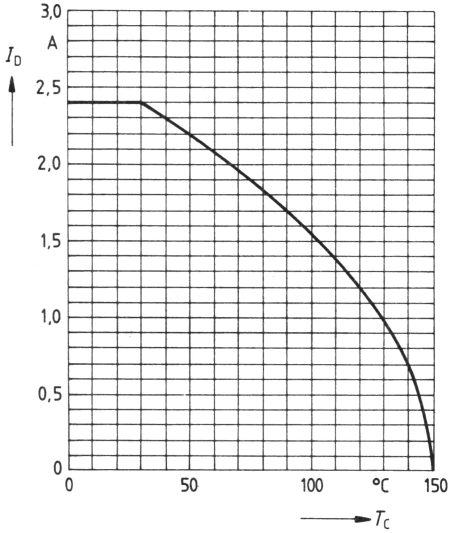


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geq 10$ V.

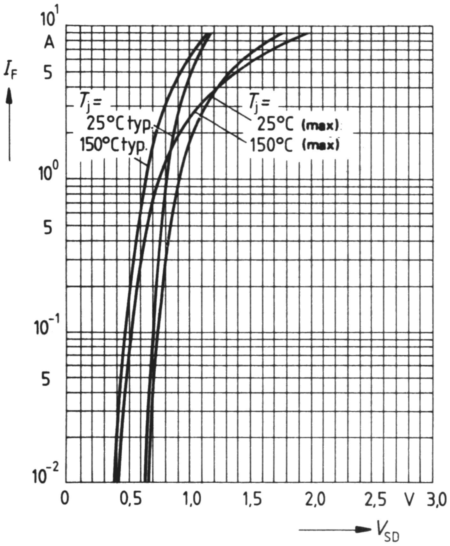


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

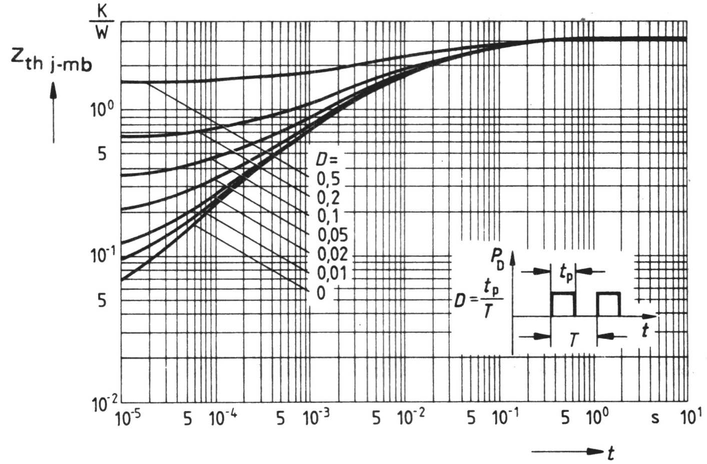


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

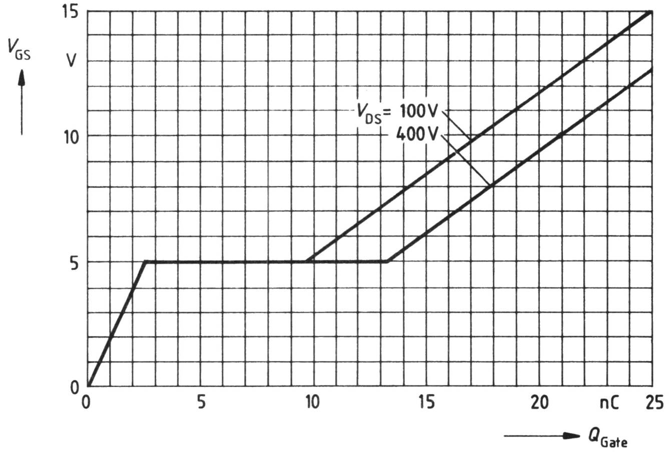


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 3{,}6$ *A.*

PowerMOS transistor BUZ74A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

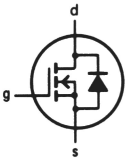
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	2,0	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	4,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



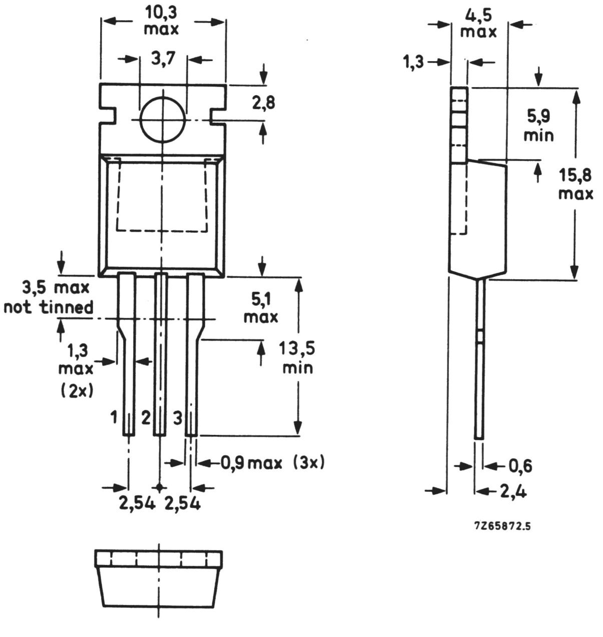

10,3
max
3,7
2,8
3,5 max
not tinned
5,1
max
1,3
max
(2x)
13,5
min
1
2
3
0,9 max (3x)
2,54 2,54
4,5
max
1,3
5,9
min
15,8
max
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 40 °C	–	2,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	8,0	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,2 A	–	3,6	4,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,2 A	1,9	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	300	500	pF
C_{oss}	Output capacitance		–	50	80	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,1 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	50	65	ns
t_f	Turn-off fall time		–	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	8,0	A
V_{SD}	Diode forward on-voltage	I_F = 4,0 A; V_{GS} = 0 V	–	1,0	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,0 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	350	–	ns
Q_{rr}	Reverse recovery charge		–	3,5	–	µC

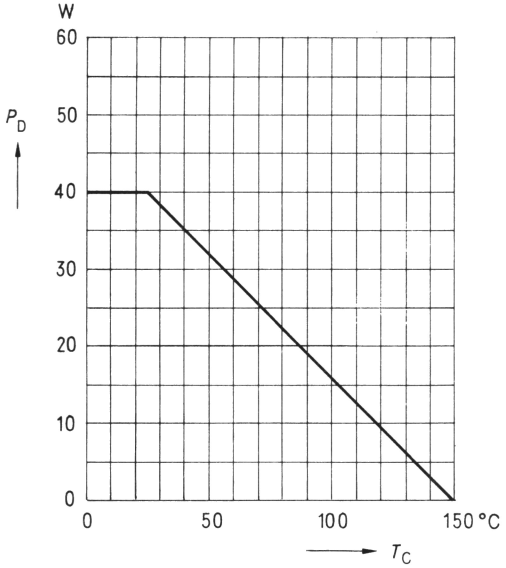


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

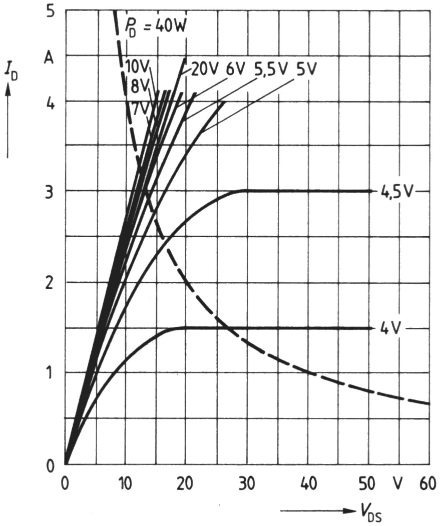


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 µs pulse test; T_{mb} = 25 °C.*

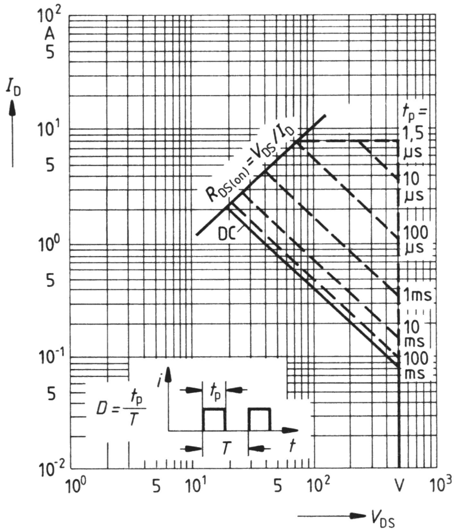


Fig.4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

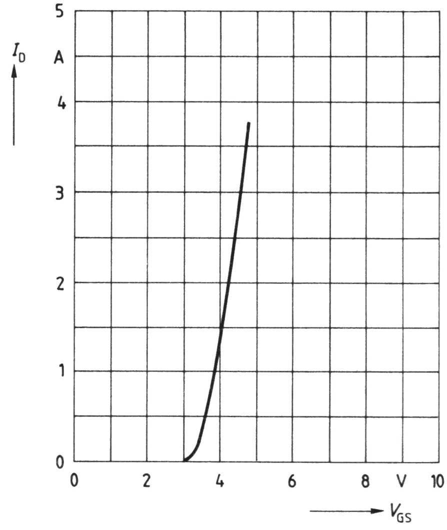


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 µs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

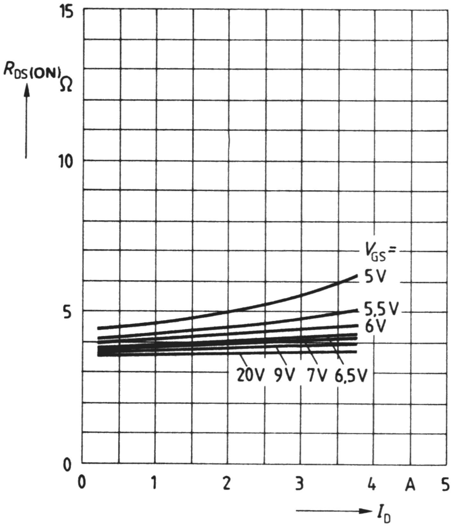


Fig. 6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

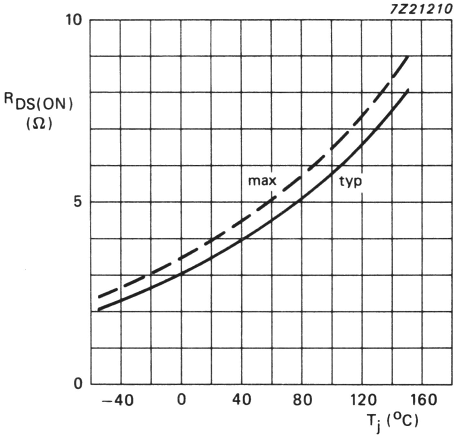


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 1,2 A; V_{GS} = 10 V.

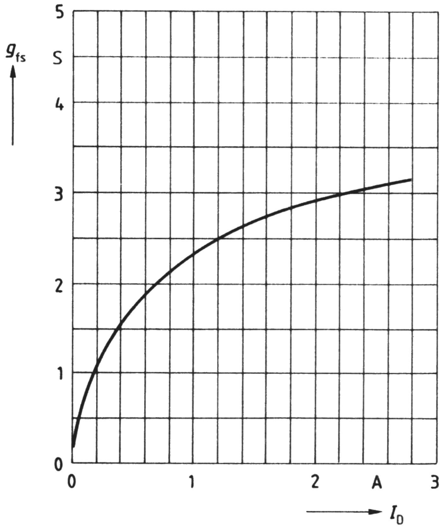


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

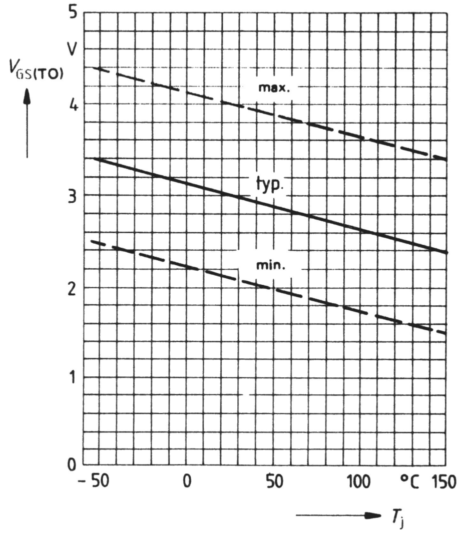


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

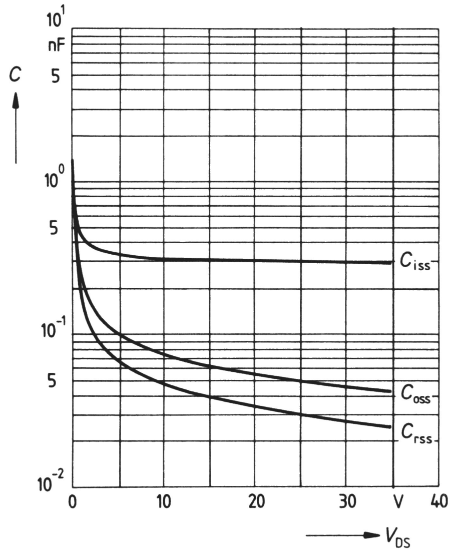


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

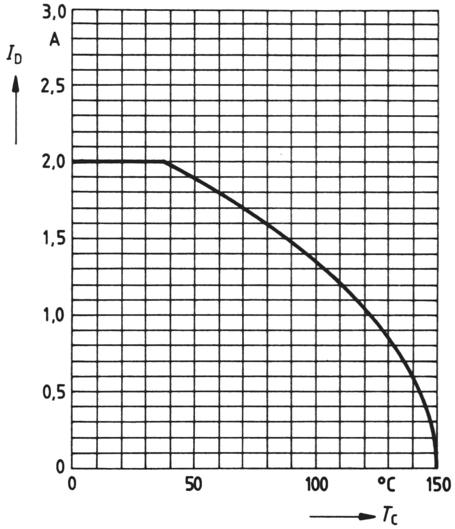


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

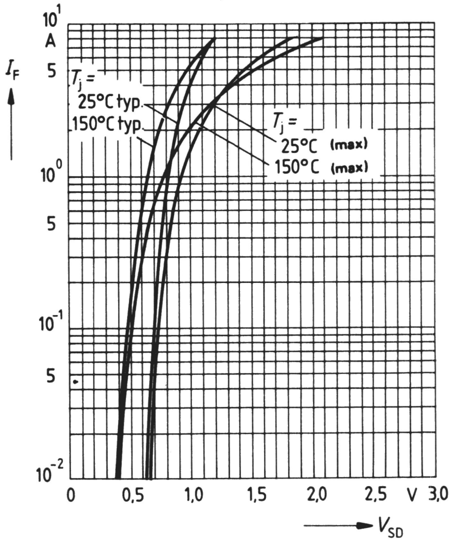


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

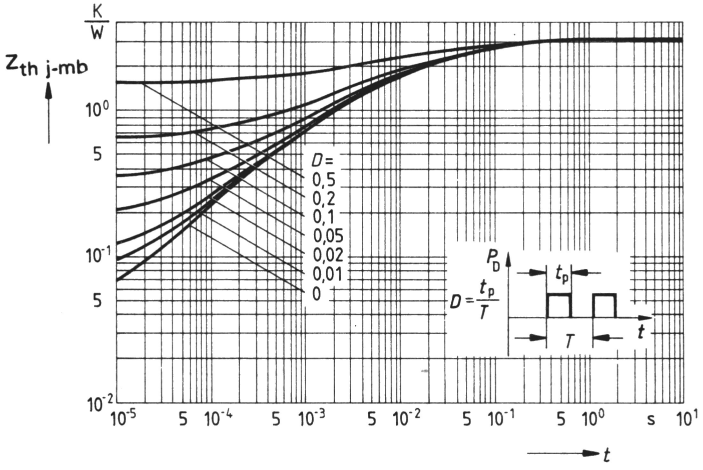


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

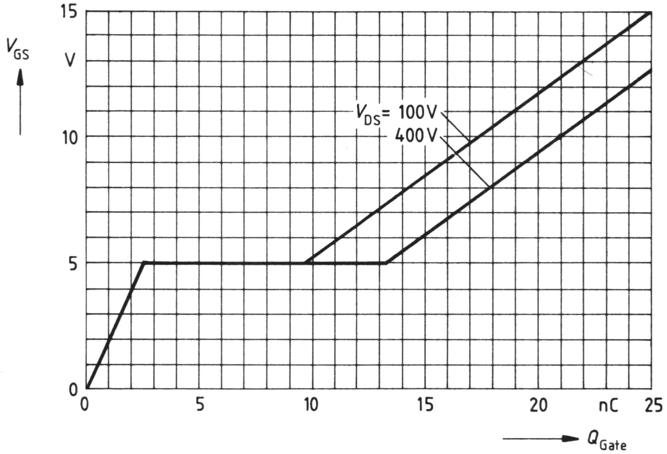


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 3,6$ A.

PowerMOS transistor BUZ90

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

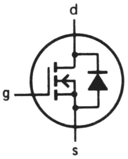
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (d.c.)	4,0	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



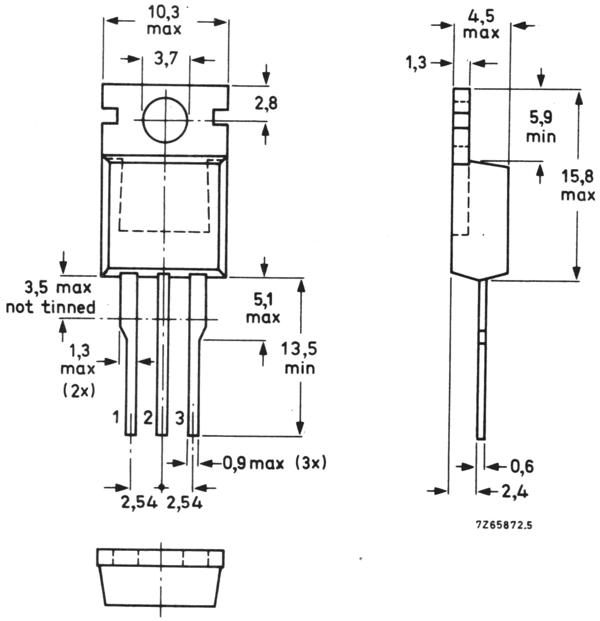

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54 2,54
0,6
2,4
7Z65872.5

Fig. 1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	600	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	4,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	16	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	600	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,5 A	–	1,8	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,5 A	1,5	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	110	170	pF
C_{rss}	Feedback capacitance		–	40	70	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	60	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	4,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	16	A
V_{SD}	Diode forward on-voltage	I_F = 8,0 A; V_{GS} = 0 V	–	0,95	1,2	V
t_{rr}	Reverse recovery time	I_F = 4,0 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1,2	–	µs
Q_{rr}	Reverse recovery charge		–	6,0	–	µC

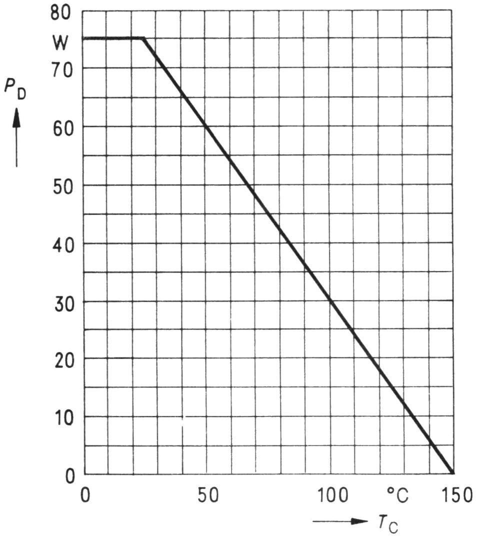


Fig.2 Power dissipation $P_D = f(T_{mb})$.

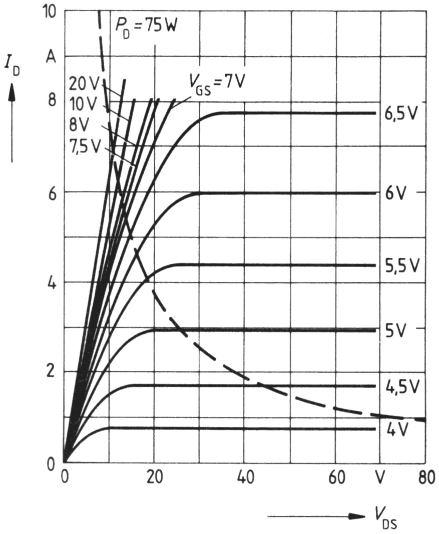


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 μs pulse test;
$T_{mb} = 25\ °C$.

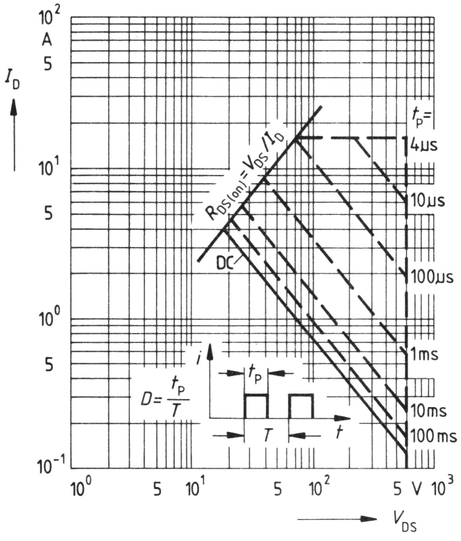


Fig.4 Safe operating area $I_D(DC)$ and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\ °C$.

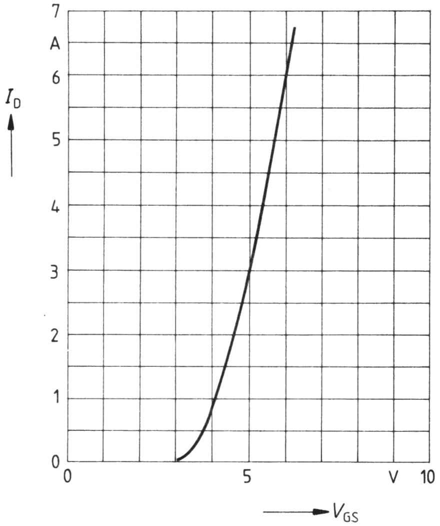


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 μs pulse test; $V_{DS} = 25\ V$,
$T_{mb} = 25\ °C$.

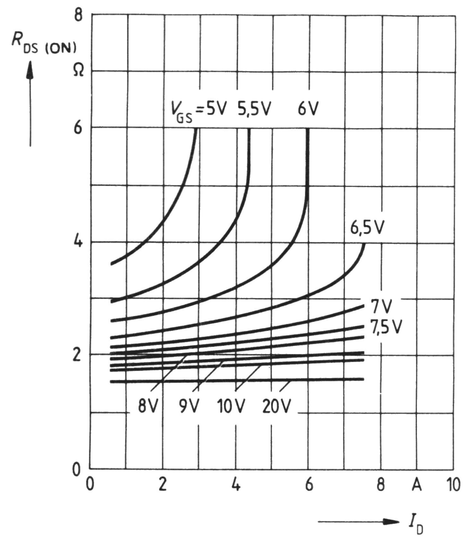


Fig. 6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

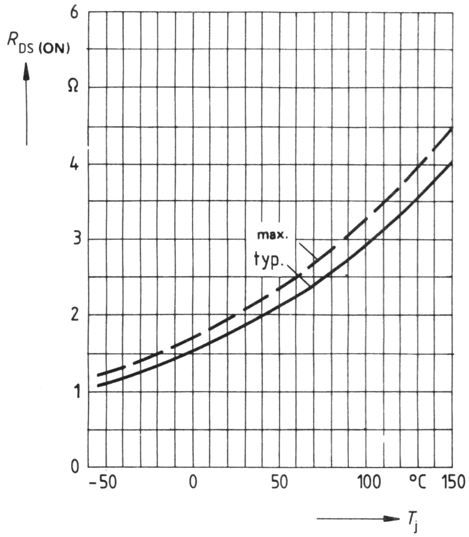


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 2,5 A; V_{GS} = 10 V.

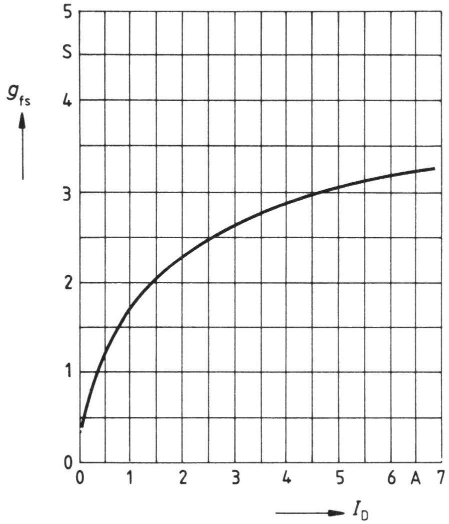


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

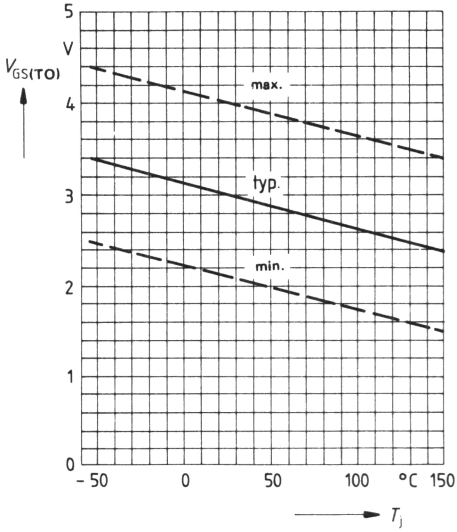


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

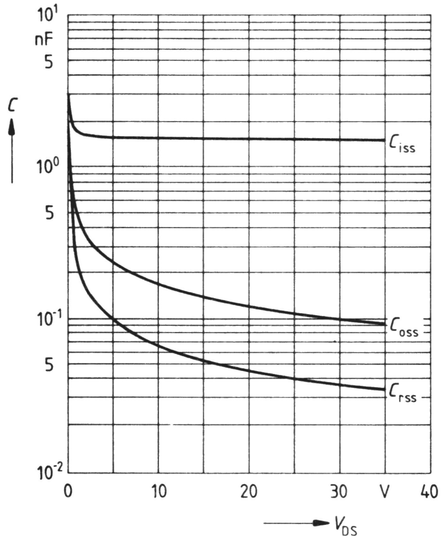


Fig. 10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

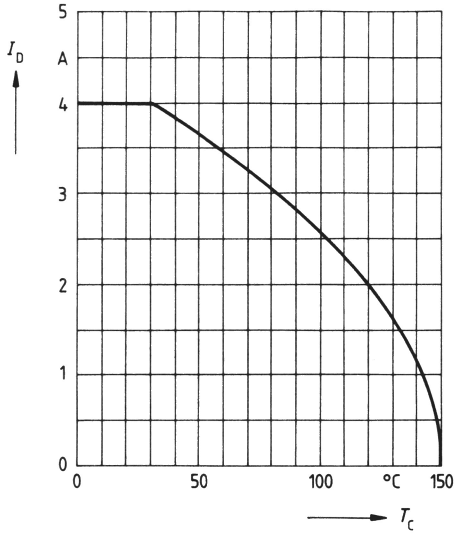


Fig. 11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

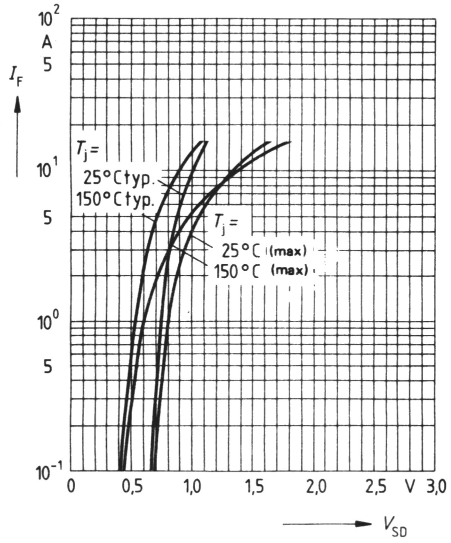


Fig. 12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

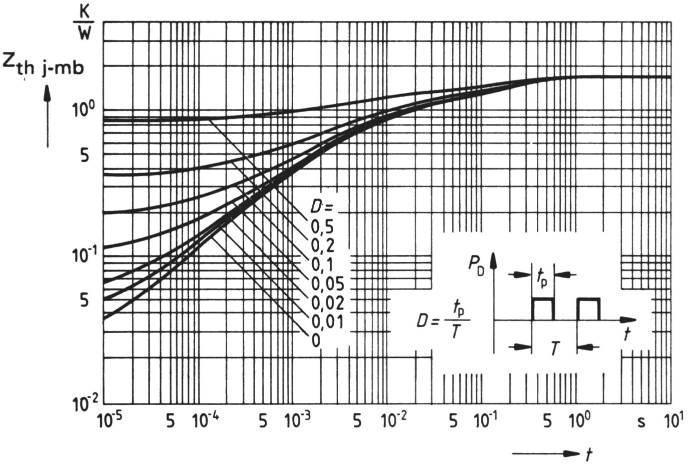


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

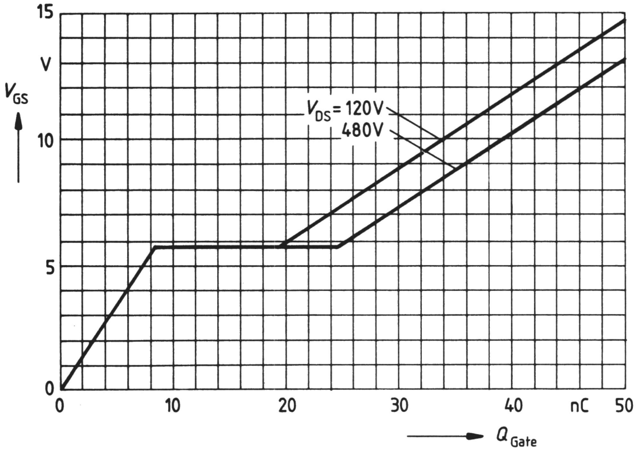


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 39,9 A.

PowerMOS transistor

BUZ90A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

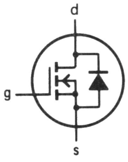
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (d.c.)	3,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



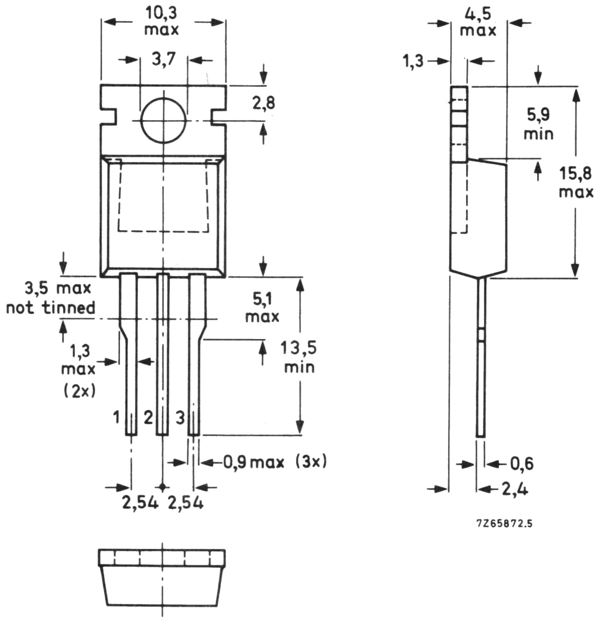

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54 2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	600	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20$ kΩ	–	600	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 35$ °C	–	3,5	A
I_D	Drain current (d.c.)	$T_{mb} = 100$ °C	–	2,3	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25$ °C	–	14	A
P_{tot}	Total power dissipation	$T_{mb} = 25$ °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1{,}67$ K/W
From junction to ambient	$R_{th\ j\text{-}a} = 75$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0{,}25$ mA	600	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600$ V; $V_{GS} = 0$ V; $T_j = 25$ °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 600$ V; $V_{GS} = 0$ V; $T_j = 125$ °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 2{,}5$ A	–	2,2	2,5	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 2{,}5$ A	1,5	2,5	–	S
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	110	170	pF
C_{rss}	Feedback capacitance		–	40	70	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30$ V; $I_D = 2{,}4$ A; $V_{GS} = 10$ V; $R_{GS} = 50$ Ω; $R_{gen} = 50$ Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	65	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	3,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	14	A
V_{SD}	Diode forward on-voltage	I_F = 7,0 A; V_{GS} = 0 V	–	1,1	1,5	V
t_{rr}	Reverse recovery time	I_F = 3,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1,2	–	µs
Q_{rr}	Reverse recovery charge		–	6,0	–	µC

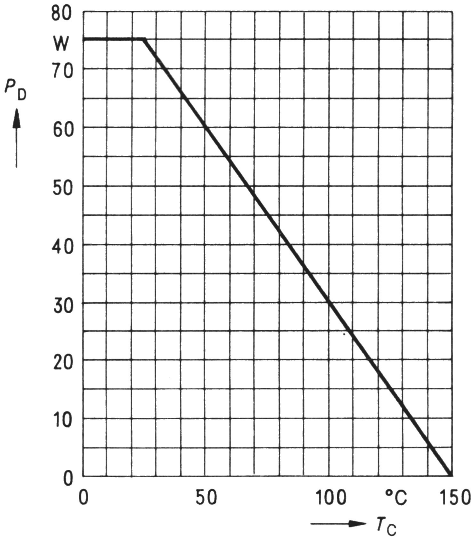


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

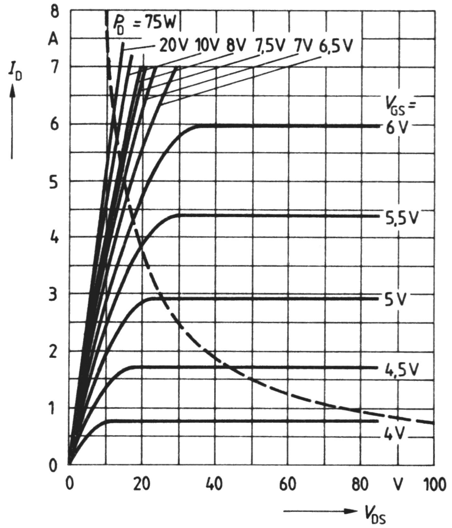


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

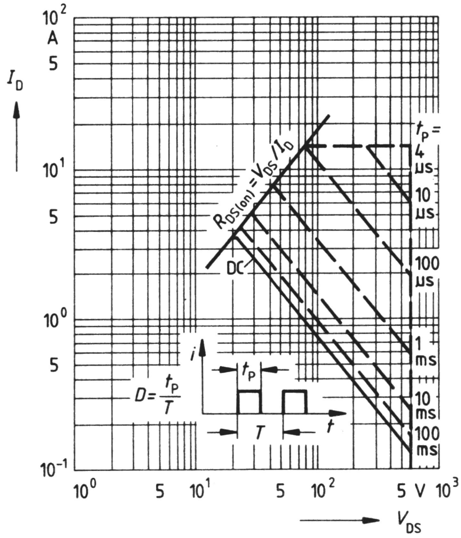


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

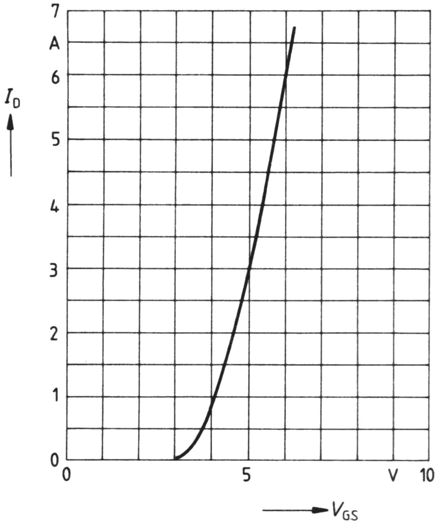


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

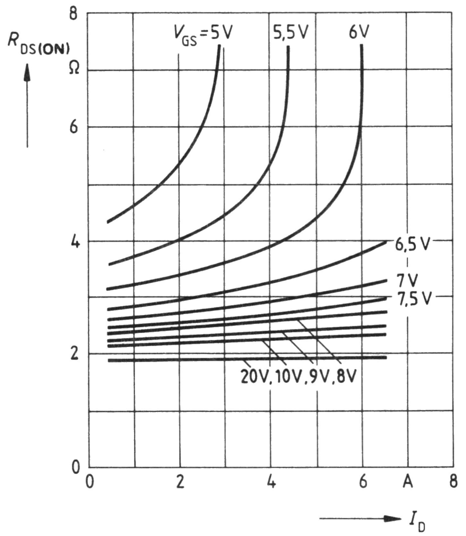


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

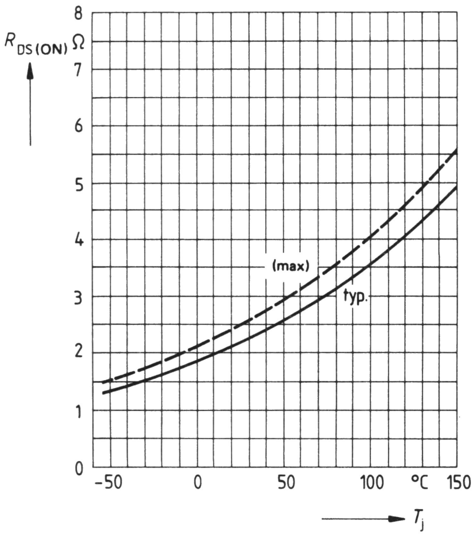


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 2,5 A; V_{GS} = 10 V.

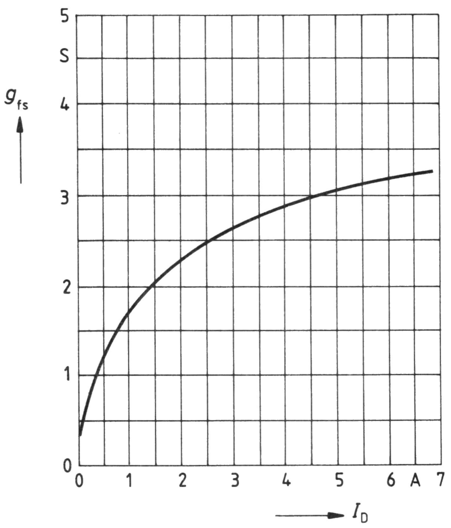


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

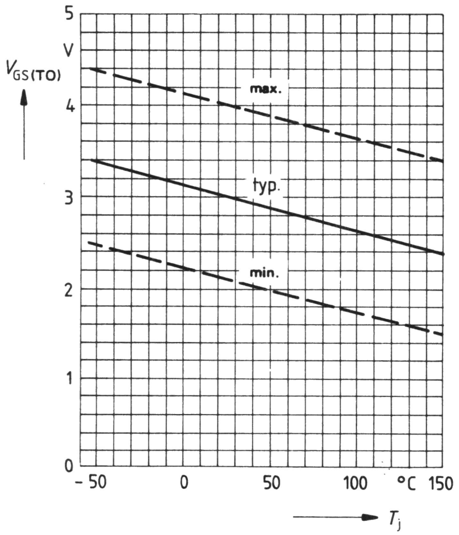


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

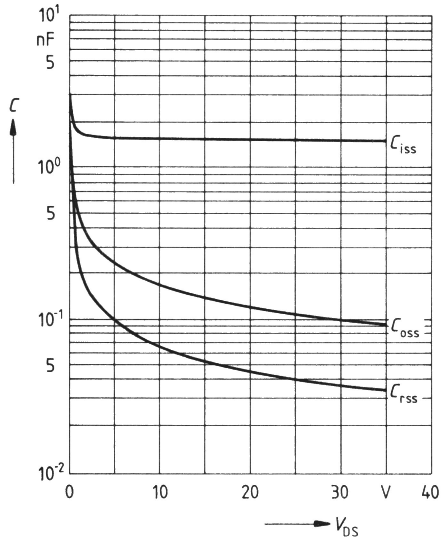


*Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.*

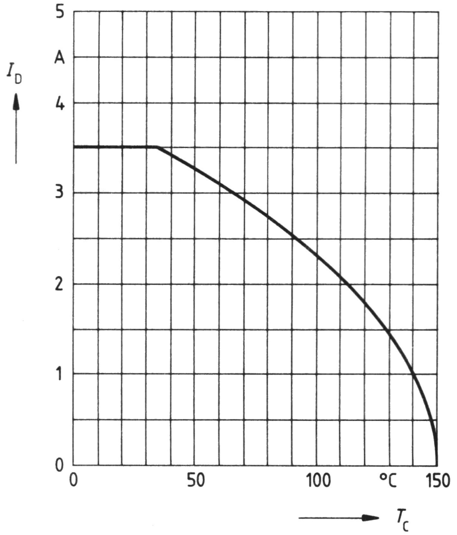


*Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.*

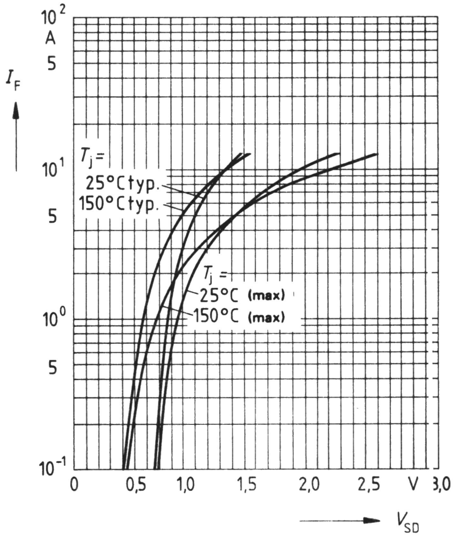


*Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.*

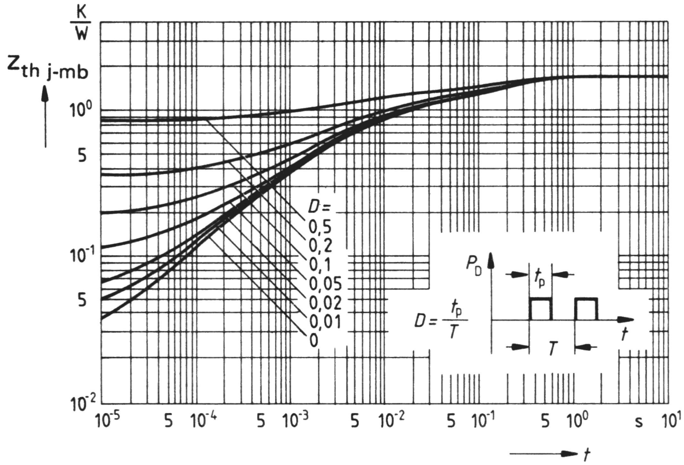


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

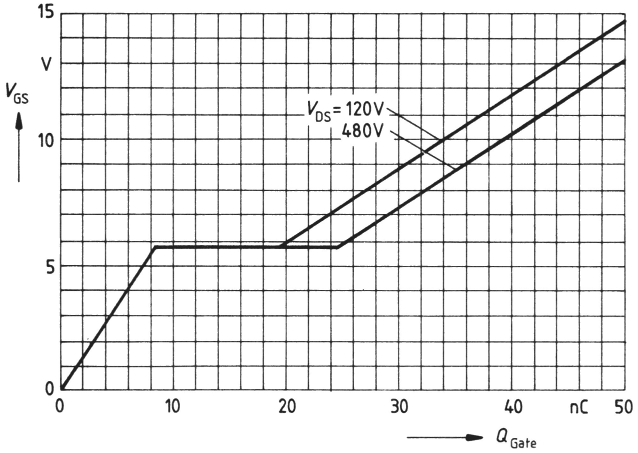


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 39,9$ A.

PowerMOS transistor BUZ78

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

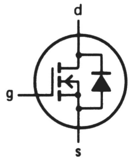
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	1,5	A
P_{tot}	Total power dissipation	40	W
$R_{DS(ON)}$	Drain-source on-state resistance	8,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



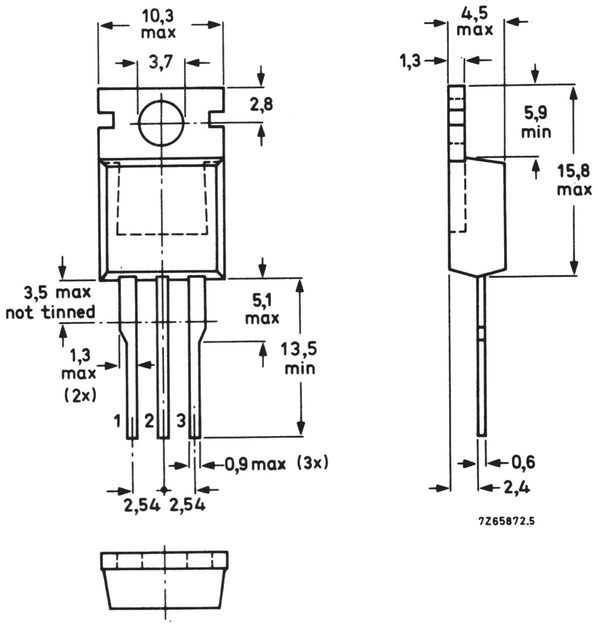

10,3 max
3,7
2,8
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54 2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	1,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	0,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	6,0	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	40	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 3,1 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,0 A	–	7,0	8,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,0 A	1,0	2,3	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	450	750	pF
C_{oss}	Output capacitance		–	42	70	pF
C_{rss}	Feedback capacitance		–	15	30	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1,7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	15	20	ns
t_r	Turn-on rise time		–	25	40	ns
$t_{d\ off}$	Turn-off delay time		–	50	65	ns
t_f	Turn-off fall time		–	30	40	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	1,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	6,0	A
V_{SD}	Diode forward on-voltage	I_F = 3,0 A; V_{GS} = 0 V	–	1,0	1,4	V
t_{rr}	Reverse recovery time	I_F = 1,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	230	–	ns
Q_{rr}	Reverse recovery charge		–	1,9	–	µC

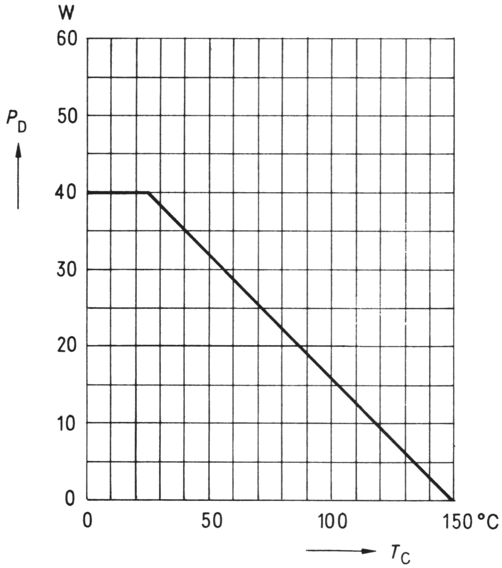


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

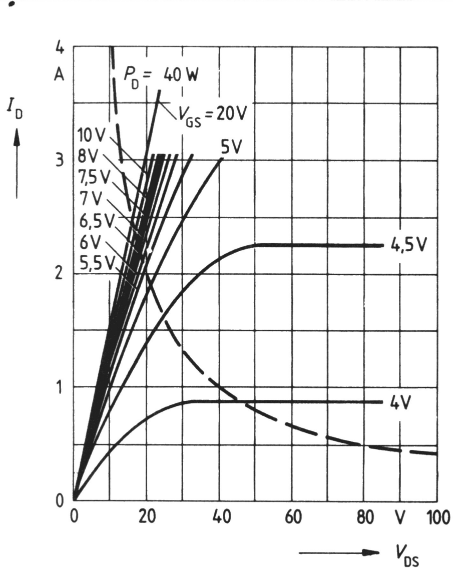


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$
Parameter: V_{GS}; *80 µs pulse test;*
$T_{mb} = 25$ *°C.*

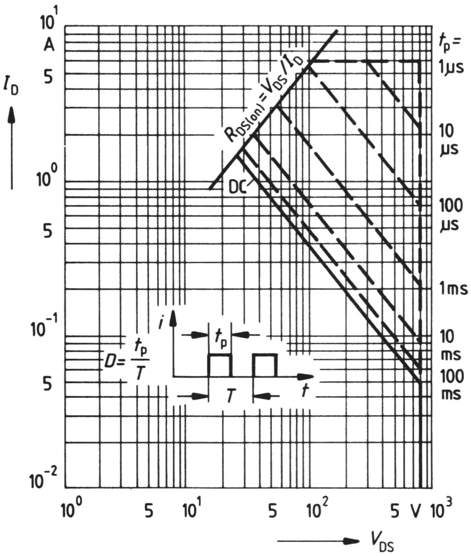


Fig.4 *Safe operating area* $I_D(DC)$ *and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ *°C.*

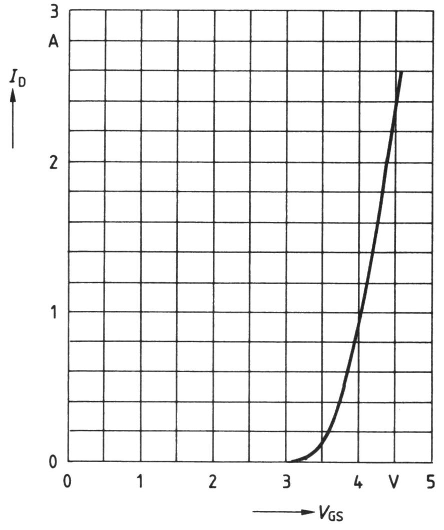


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ *V,*
$T_{mb} = 25$ *°C.*

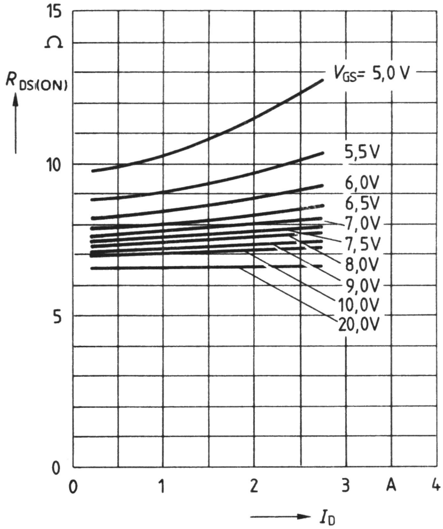


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; $T_j = 25$ °C.

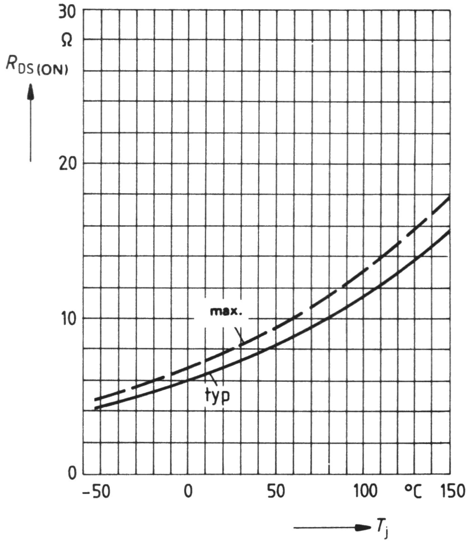


Fig. 7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

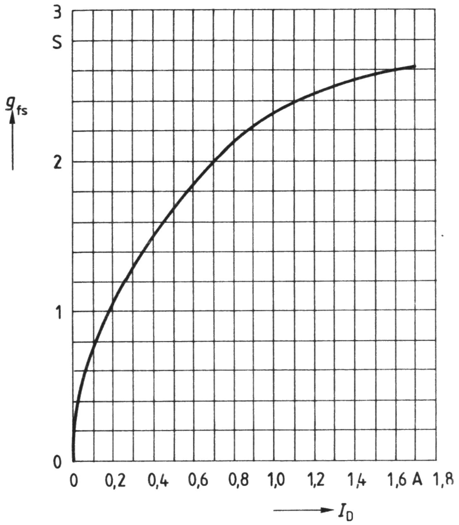


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 µs pulse test;* $V_{DS} = 25$ V; $T_j = 25$ °C.

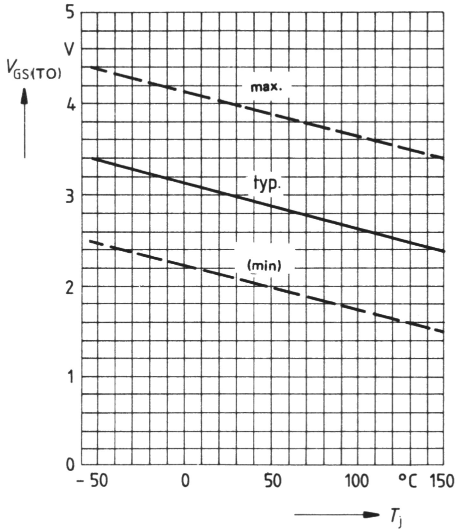


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; $I_D = 1$ mA.

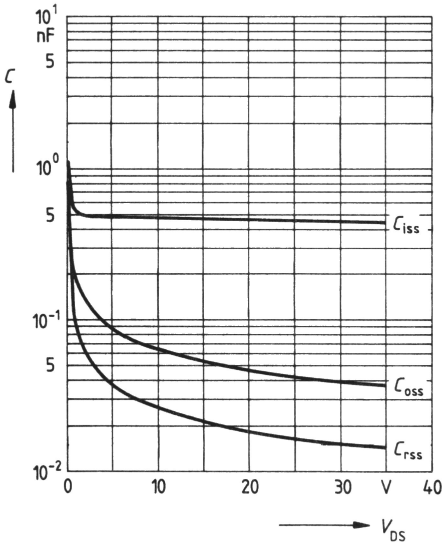


Fig. 10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

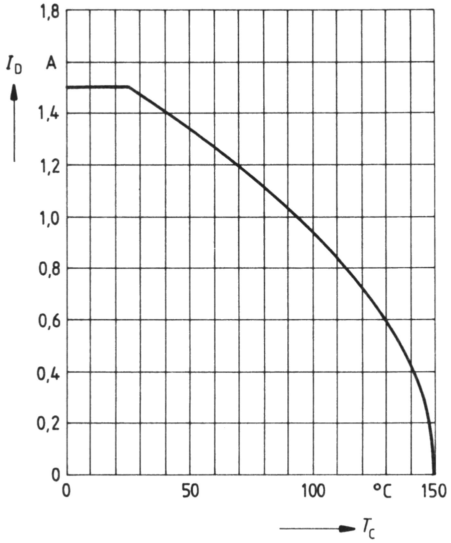


Fig. 11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

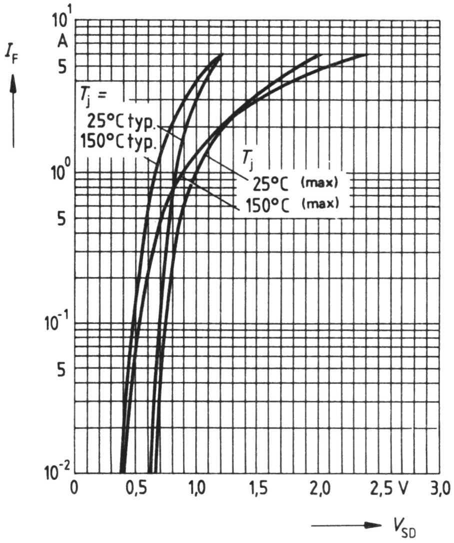


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

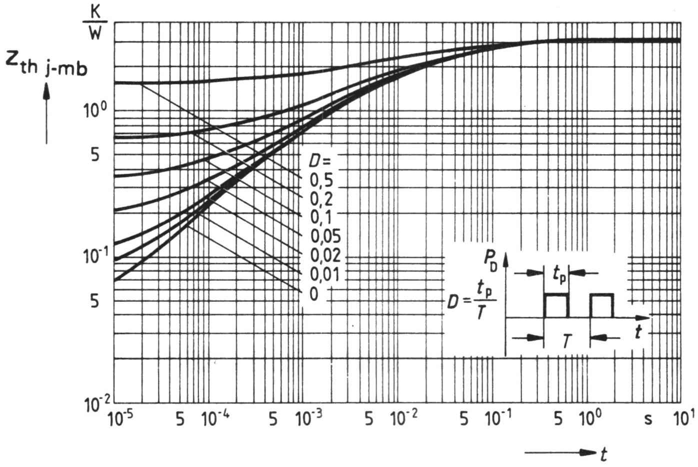


Fig.13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

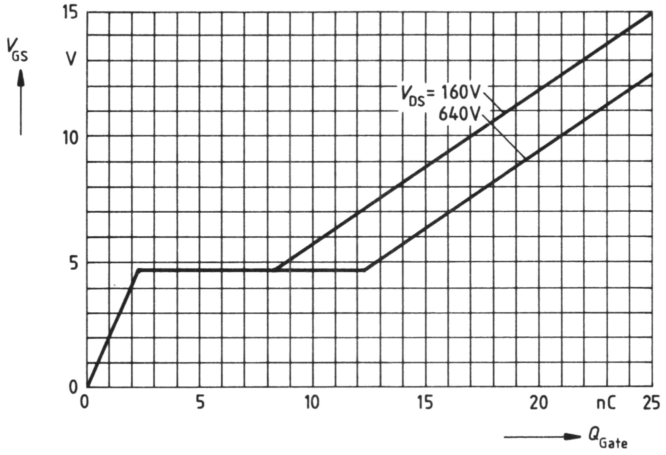


Fig.14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 2{,}25$ A.

PowerMOS transistor BUZ80

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

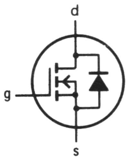
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	2,6	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	4,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



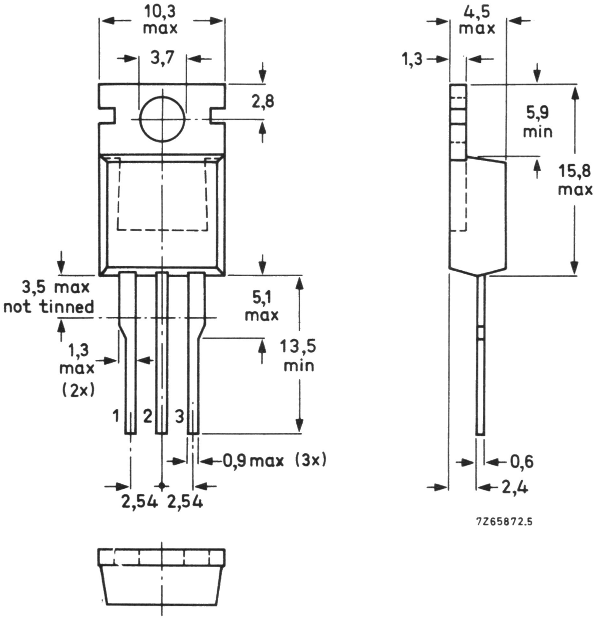

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\ k\Omega$	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 50\ °C$	–	2,6	A
I_D	Drain current (d.c.)	$T_{mb} = 100\ °C$	–	1,8	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\ °C$	–	10	A
P_{tot}	Total power dissipation	$T_{mb} = 25\ °C$	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1,67$ K/W
From junction to ambient	$R_{th\ j\text{-}a} = 75$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\ V$; $I_D = 0,25\ mA$	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\ mA$	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 800\ V$; $V_{GS} = 0\ V$; $T_j = 25\ °C$	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 800\ V$; $V_{GS} = 0\ V$; $T_j = 125\ °C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\ V$; $V_{DS} = 0\ V$	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 1,7\ A$	–	3,5	4,0	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\ V$; $I_D = 1,7\ A$	1,0	1,8	–	S
C_{iss}	Input capacitance	$V_{GS} = 0\ V$; $V_{DS} = 25\ V$; $f = 1\ MHz$	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\ V$; $I_D = 2,1\ A$; $V_{GS} = 10\ V$; $R_{GS} = 50\ \Omega$; $R_{gen} = 50\ \Omega$	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,6	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5,2 A; V_{GS} = 0 V	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,6 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	1800	–	ns
Q_{rr}	Reverse recovery charge		–	12	–	μC

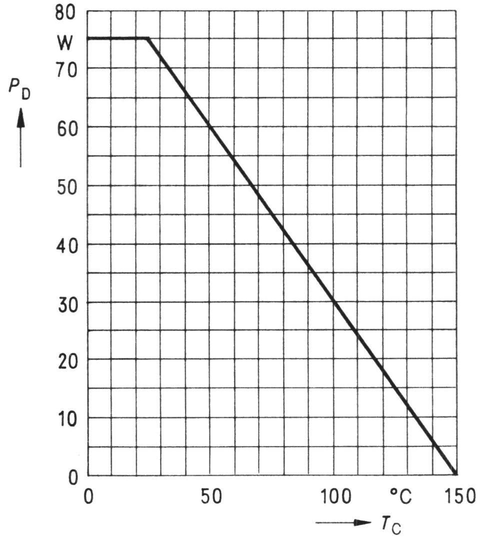


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

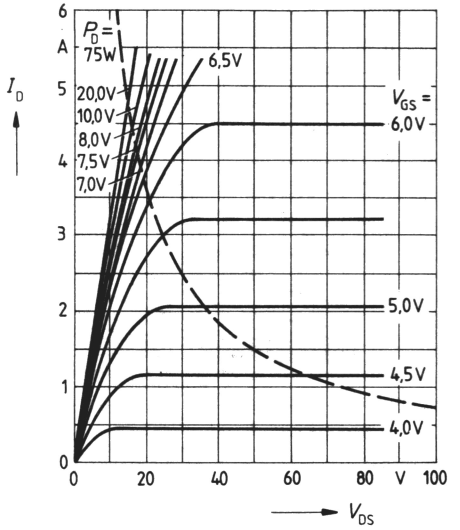


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

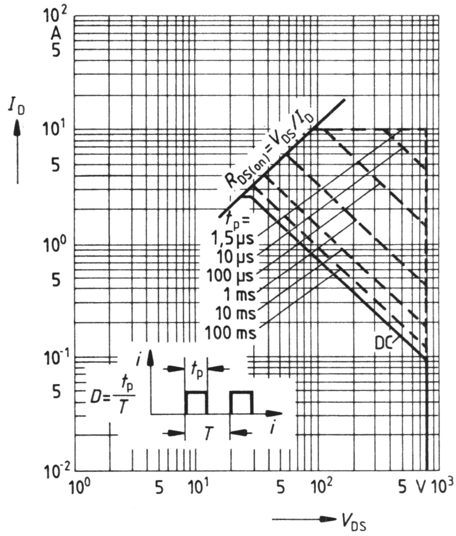


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

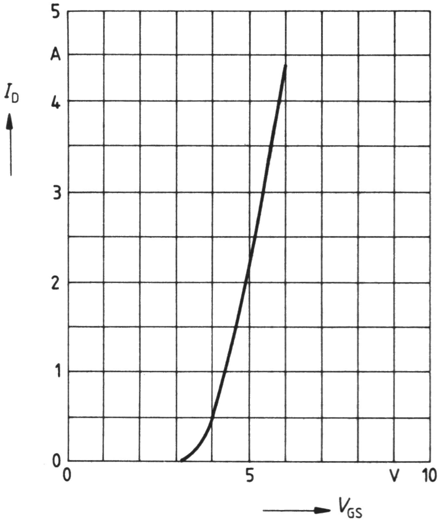


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

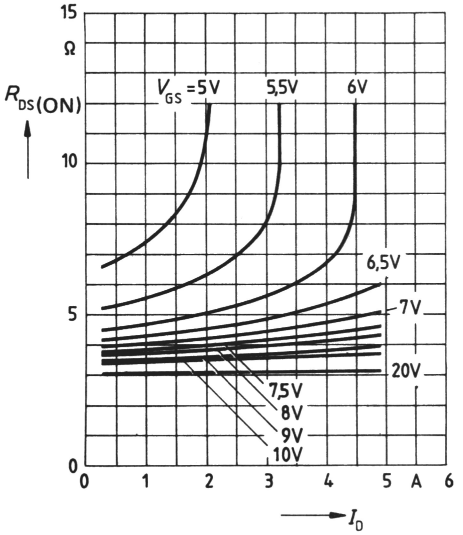


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

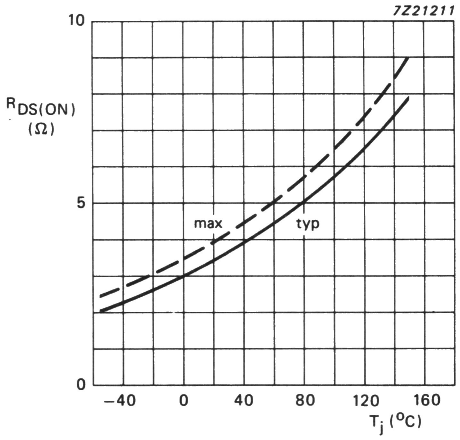


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 1,7 A; V_{GS} = 10 V.

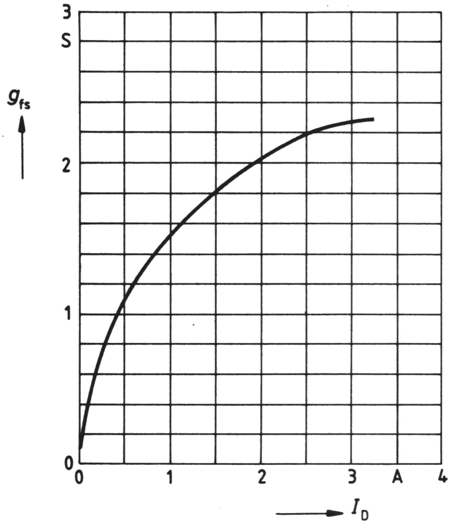


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

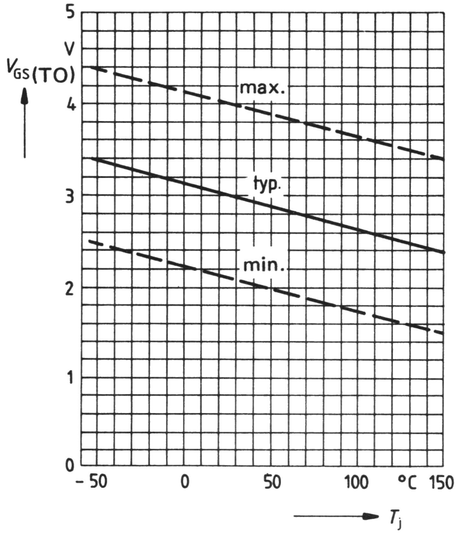


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

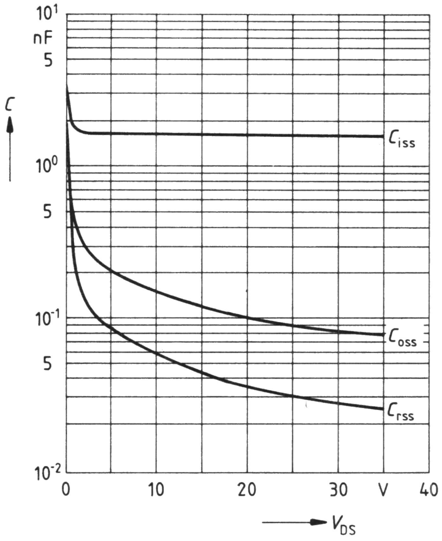


Fig. 10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

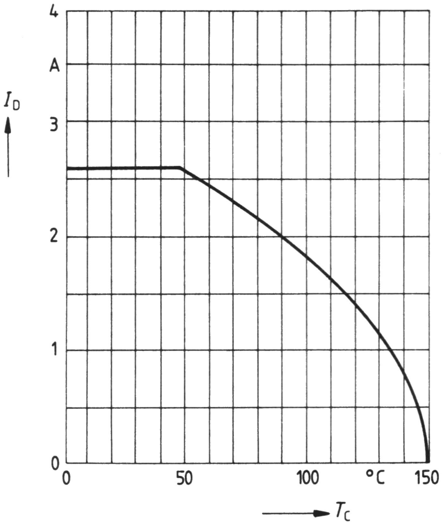


Fig. 11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

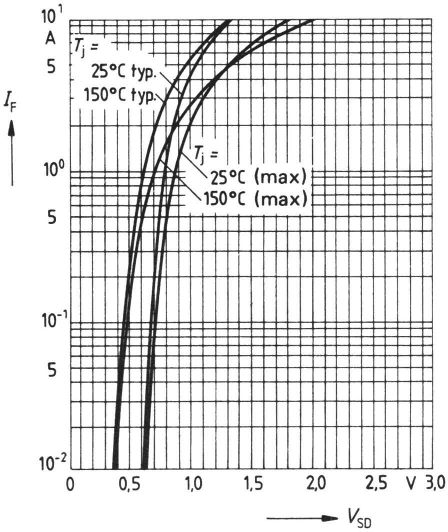


Fig. 12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

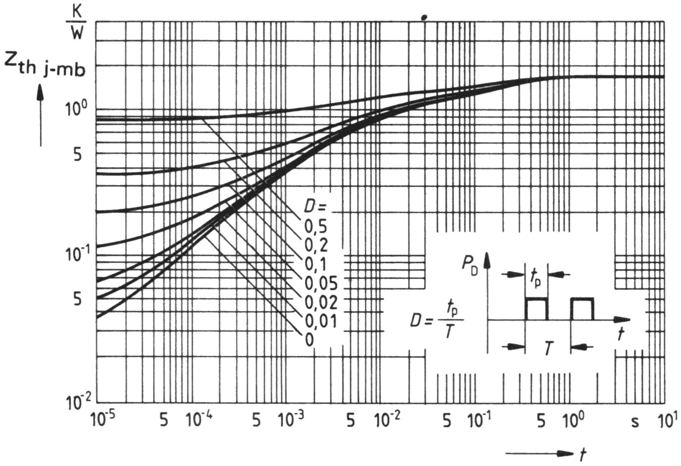


Fig. 13 Transient thermal impedance $Z_{th\ j-mb} = f(t)$
Parameter: $D = t_p/T$.

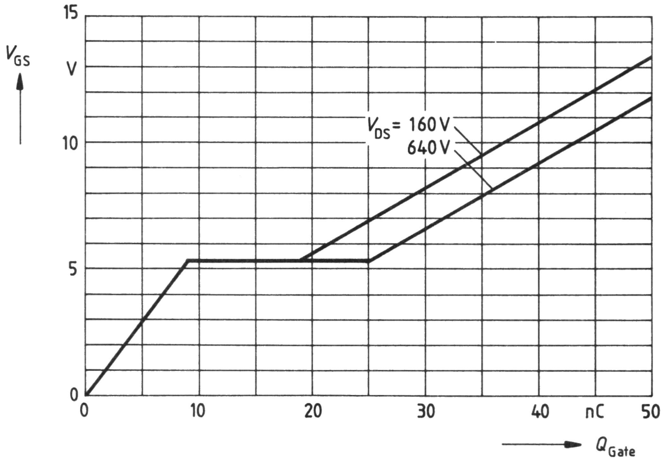


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5$ A.

PowerMOS transistor BUZ80A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

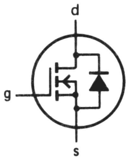
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	3,0	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	3,0	Ω

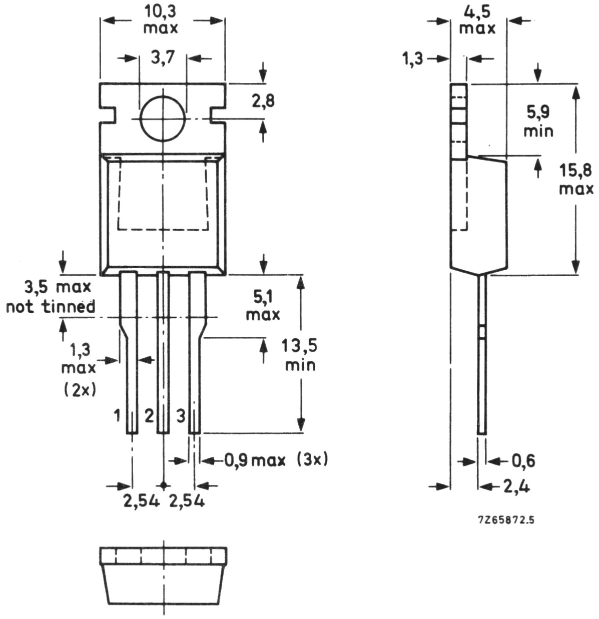
MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source





10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
1,3 max (2x)
13,5 min
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 50 °C	–	3,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,7 A	–	2,7	3,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,7 A	1,0	1,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	3,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	12	A
V_{SD}	Diode forward on-voltage	I_F = 6,0 A; V_{GS} = 0 V	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 3 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1800	–	ns
Q_{rr}	Reverse recovery charge		–	12	–	µC

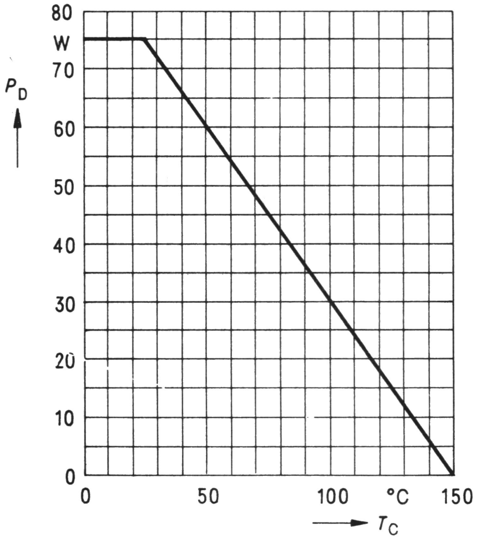


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

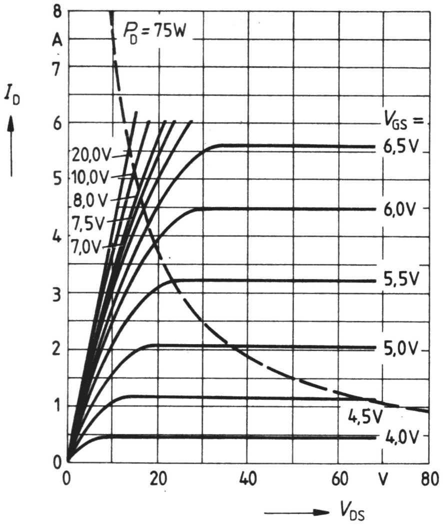


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

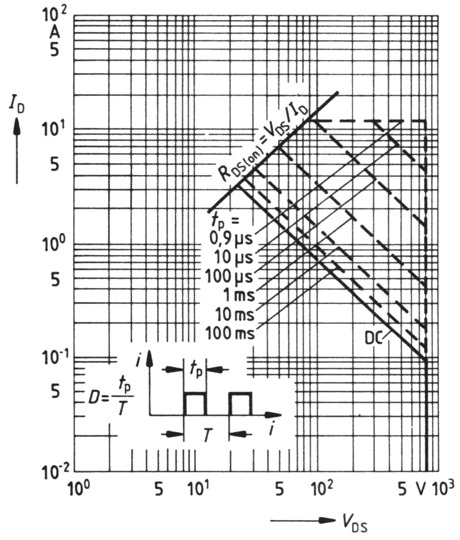


Fig. 4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

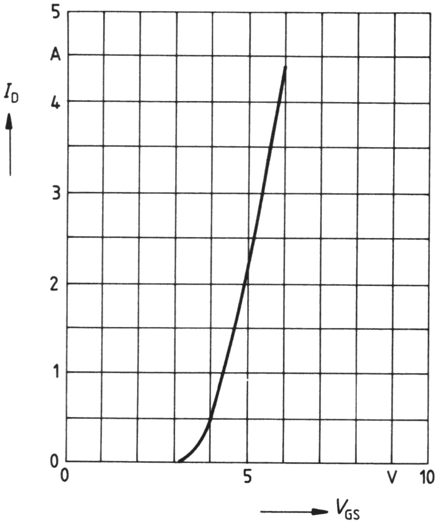


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

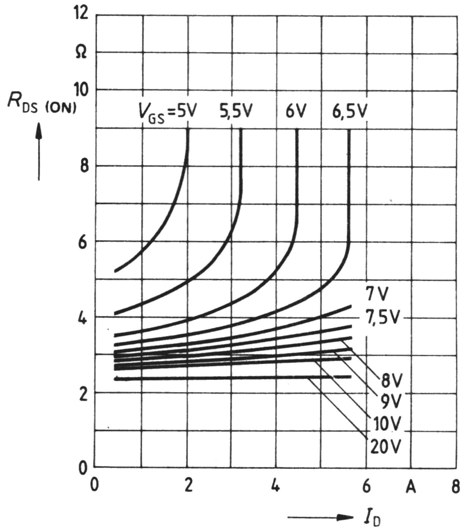


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\ °C$.

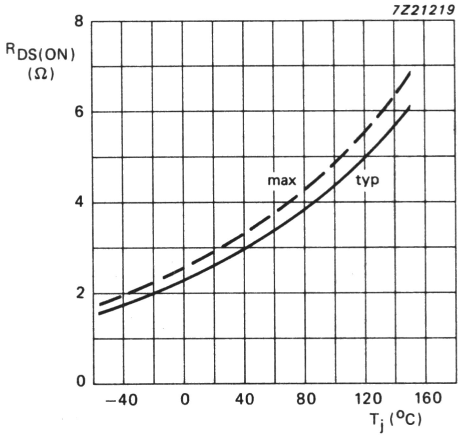


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}7\ A$; $V_{GS} = 10\ V$.

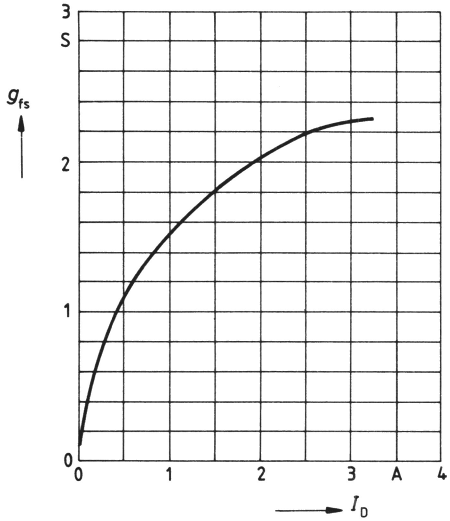


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\ °C$.

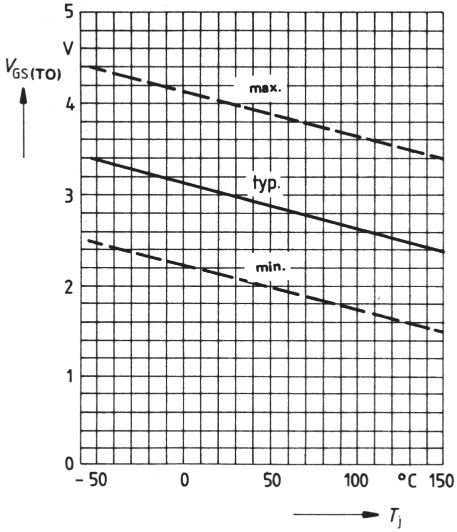


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

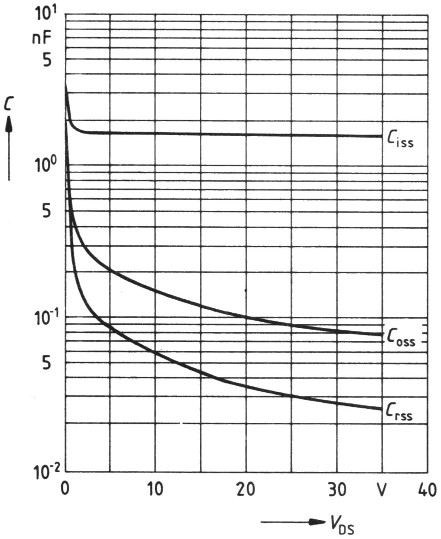


Fig. 10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

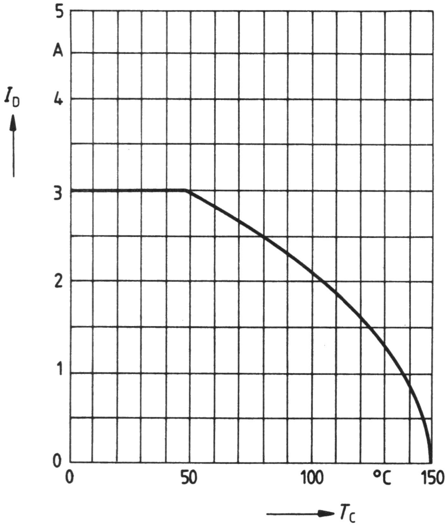


Fig. 11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

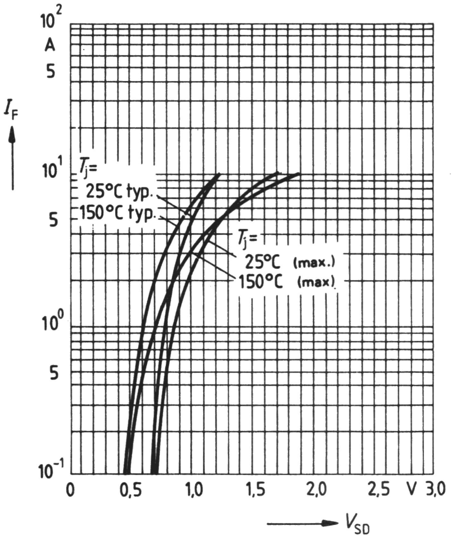


Fig. 12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80\ \mu s$.

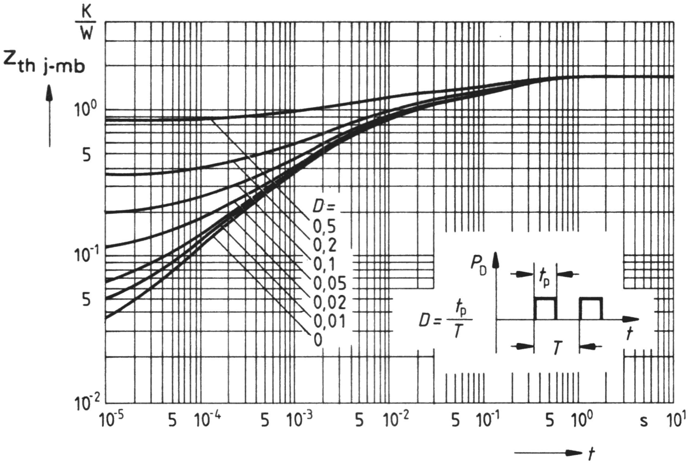


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

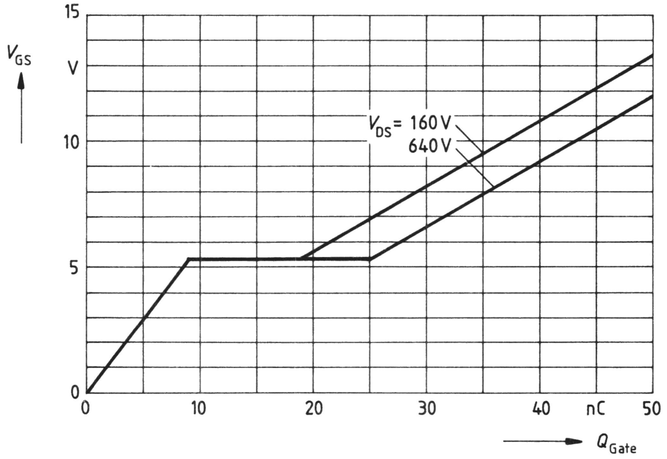


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5\ A$.

PowerMOS transistor BUZ50A

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

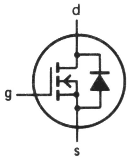
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	5,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



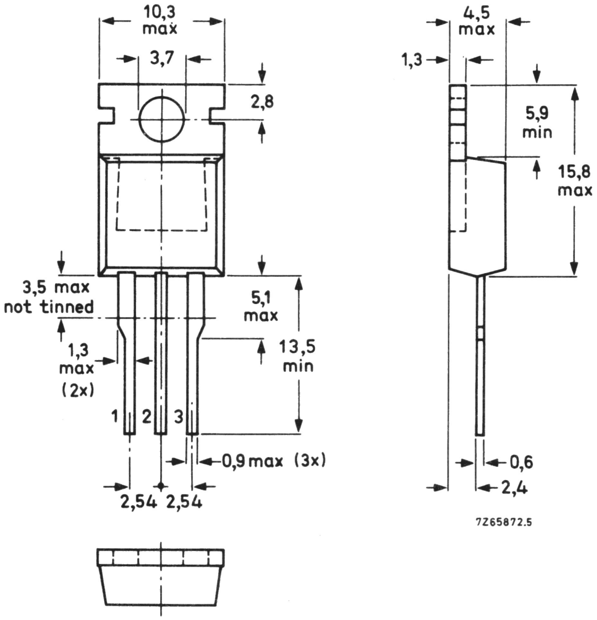

10,3 max
3,7
2,8
3,5 max not tinned
1,3 max (2x)
5,1 max
13,5 min
1
2
3
0,9 max (3x)
2,54 2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	4,5	5,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	0,7	1,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	50	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5,0 A; V_{GS} = 0 V	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	2000	–	ns
Q_{rr}	Reverse recovery charge		–	15	–	µC

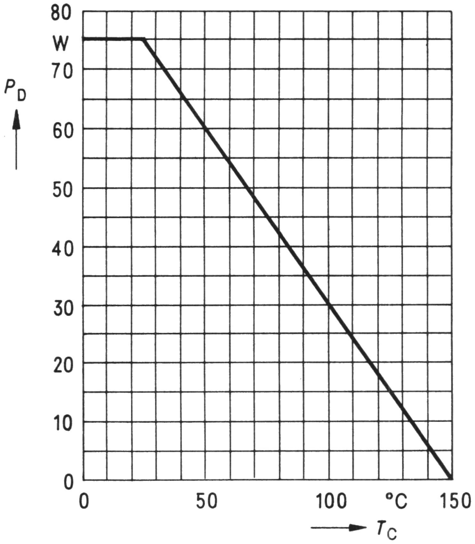


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

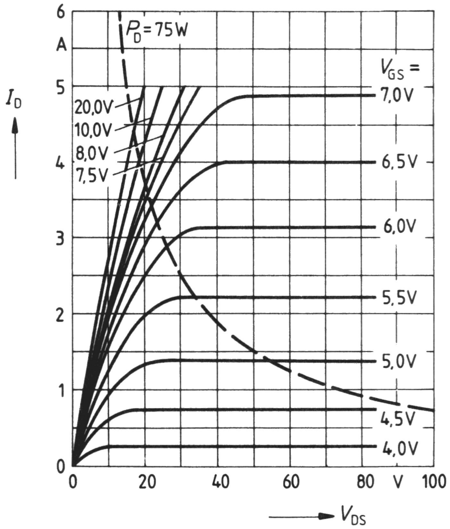


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

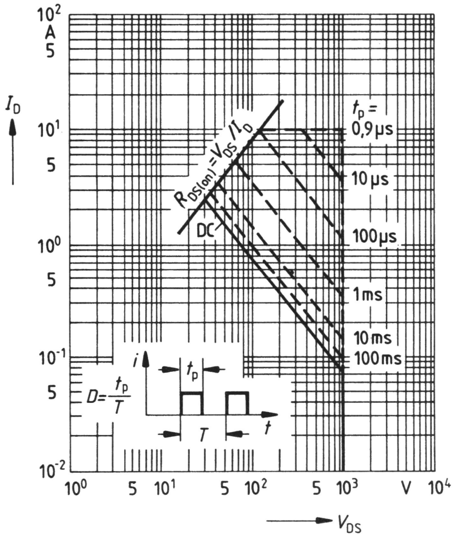


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

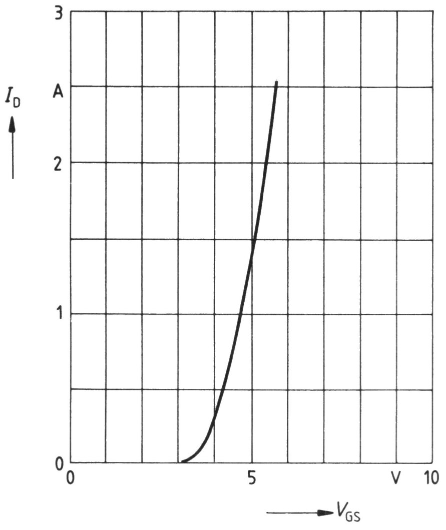


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

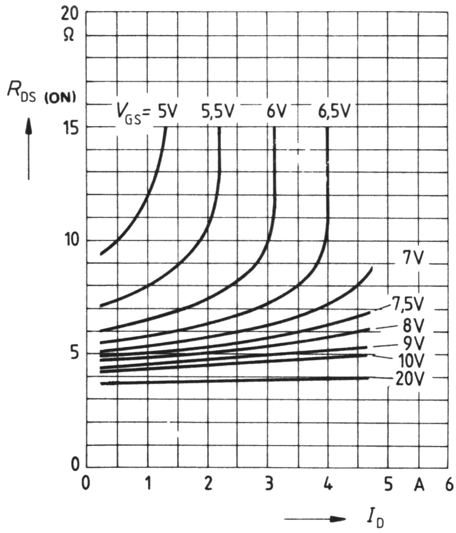


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

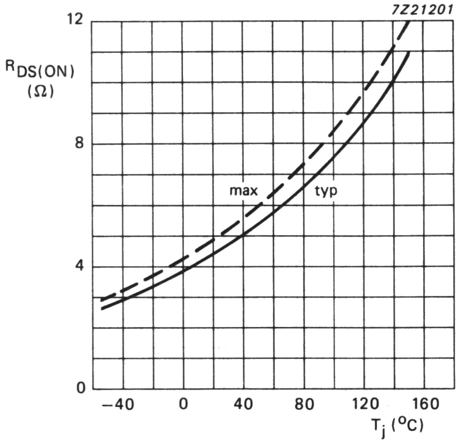


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

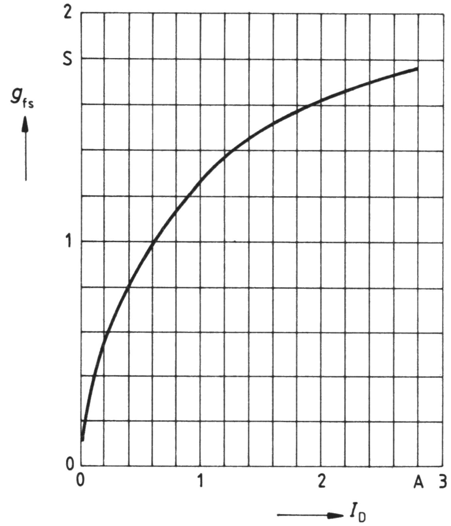


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

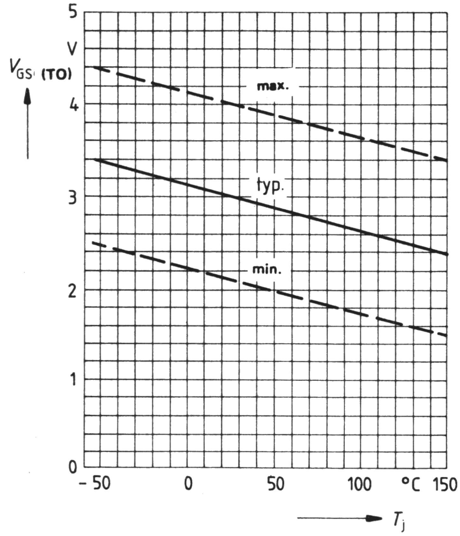


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

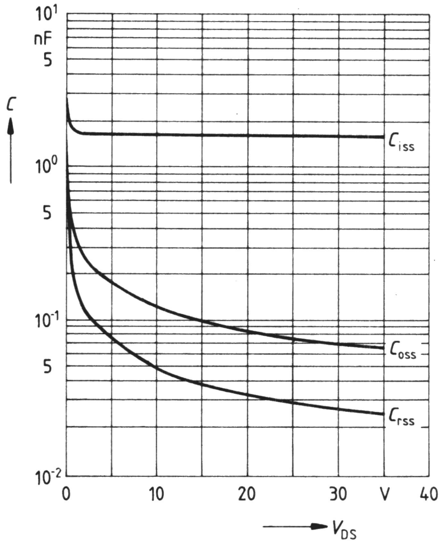


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

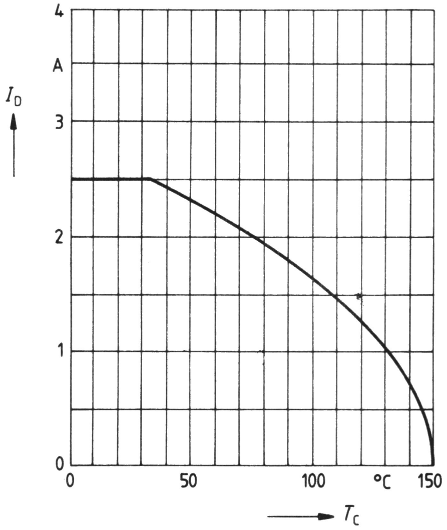


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

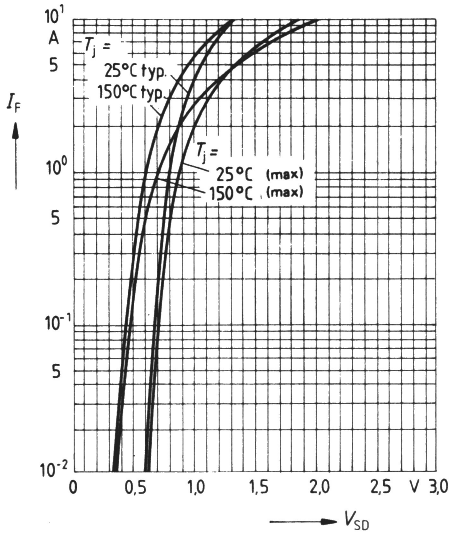


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

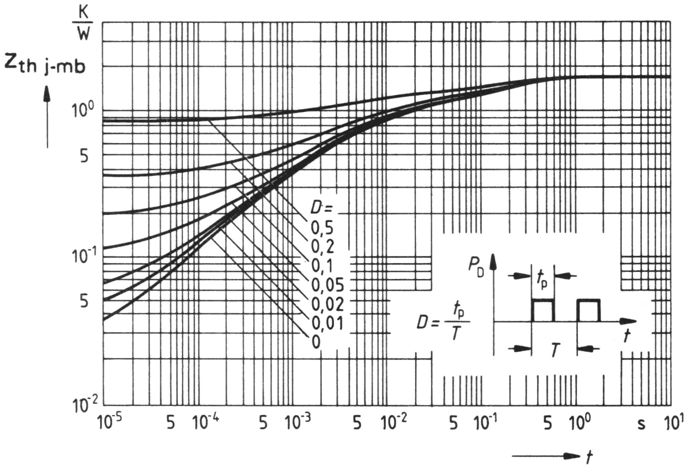


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

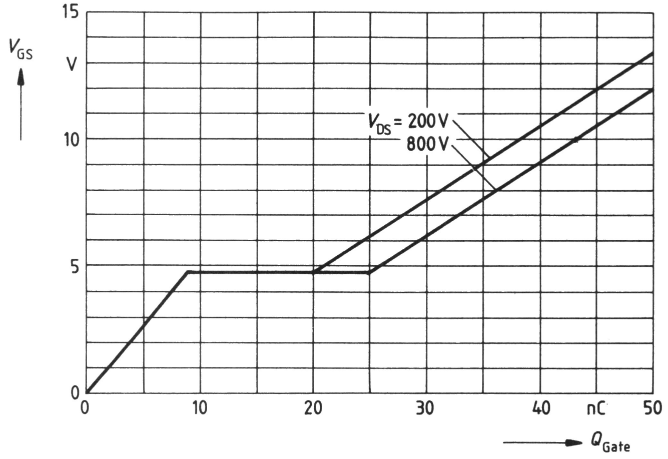


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 3{,}75\ A$.

PowerMOS transistor BUZ50B

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

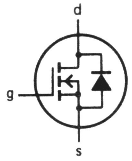
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,0	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	8,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



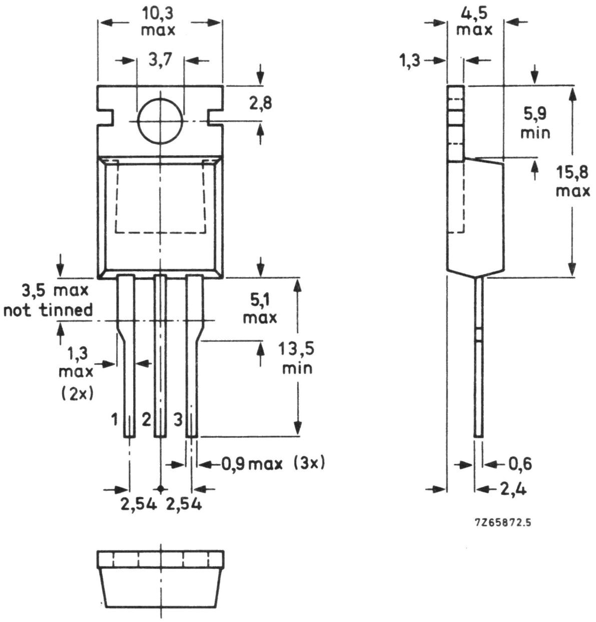

10,3 max
3,7
2,8
3,5 max not tinned
1,3 max (2x)
5,1 max
13,5 min
1
2
3
0,9 max (3x)
2,54 2,54
4,5 max
1,3
5,9 min
15,8 max
0,6
2,4
7Z65872.5

Fig.1 TO220AB; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	8,0	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 75 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	6,5	8,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	0,7	1,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1,7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	8,0	A
V_{SD}	Diode forward on-voltage	I_F = 4,0 A; V_{GS} = 0 V	–	1,05	1,30	V
t_{rr}	Reverse recovery time	I_F = 2 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	2000	–	ns
Q_{rr}	Reverse recovery charge		–	15	–	µC

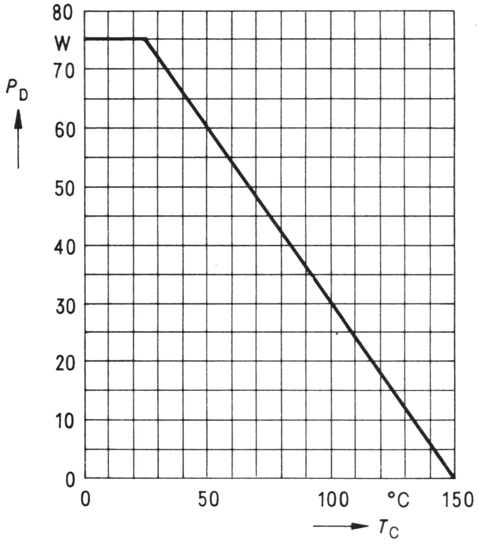


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

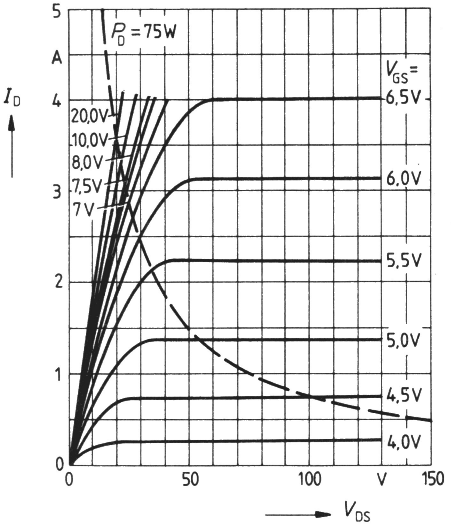


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$
Parameter: V_{GS}; *80 µs pulse test;*
$T_{mb} = 25\ °C$.

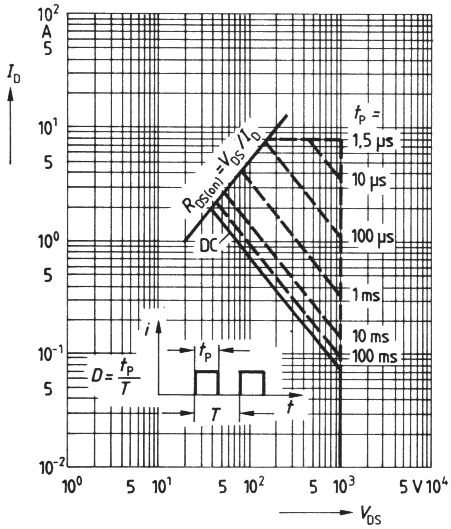


Fig.4 *Safe operating area* $I_D(DC)$ *and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\ °C$.

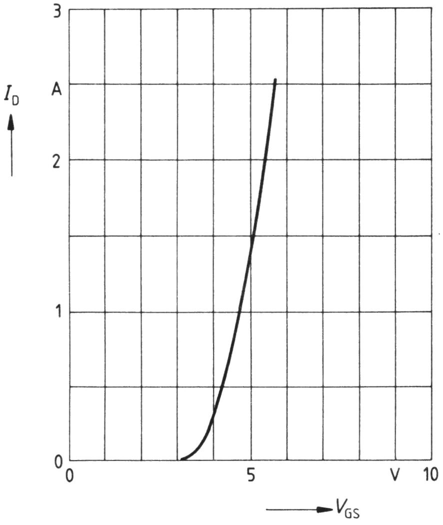


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25\ V$,
$T_{mb} = 25\ °C$.

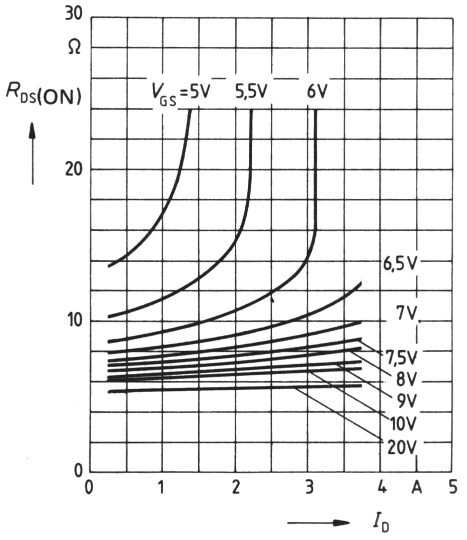


Fig. 6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; T_j = 25 °C.*

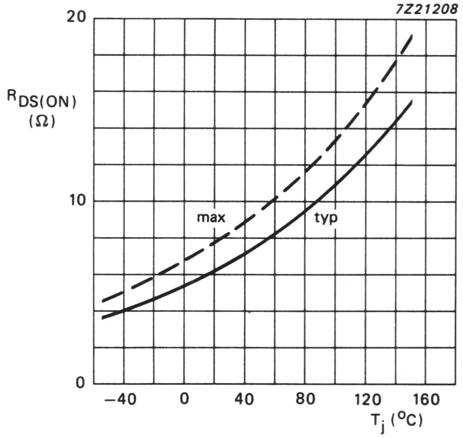


Fig. 7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: I_D = 2,5 A; V_{GS} = 10 V.*

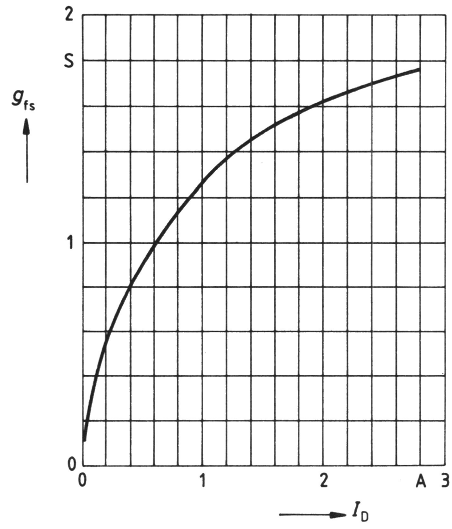


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 μs pulse test; V_{DS} = 25 V; T_j = 25 °C.*

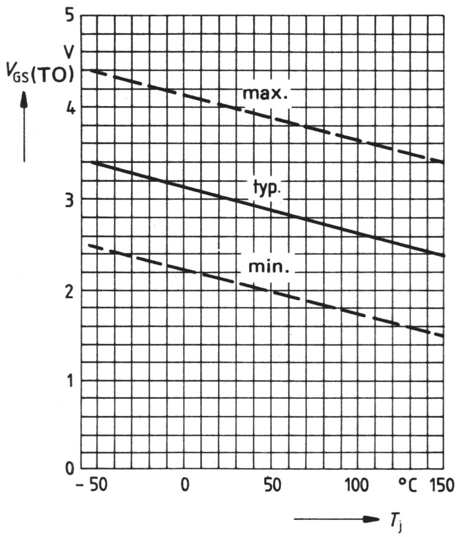


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.*

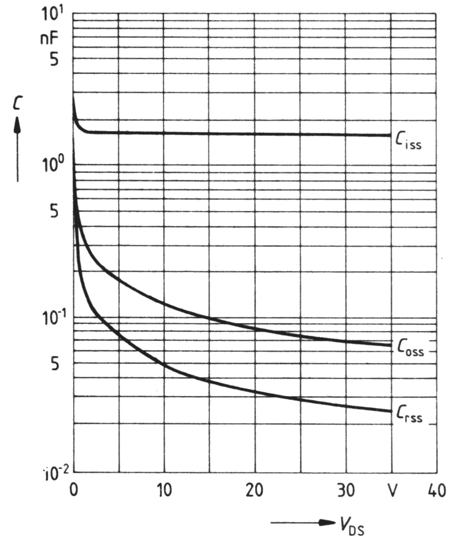


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

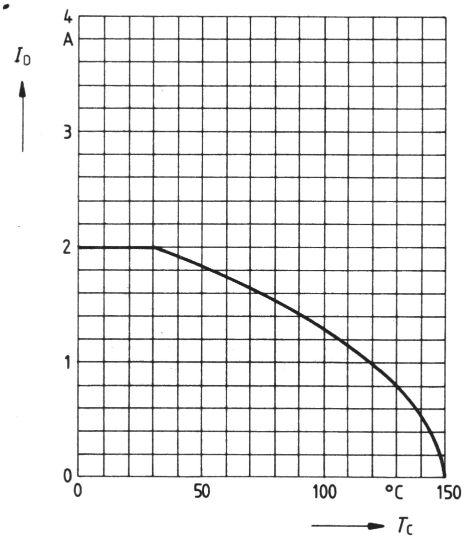


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

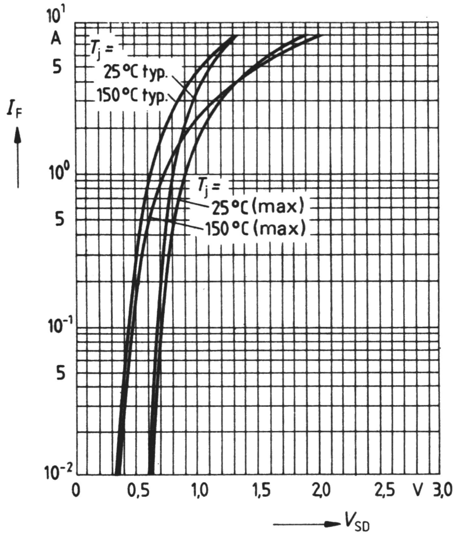


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

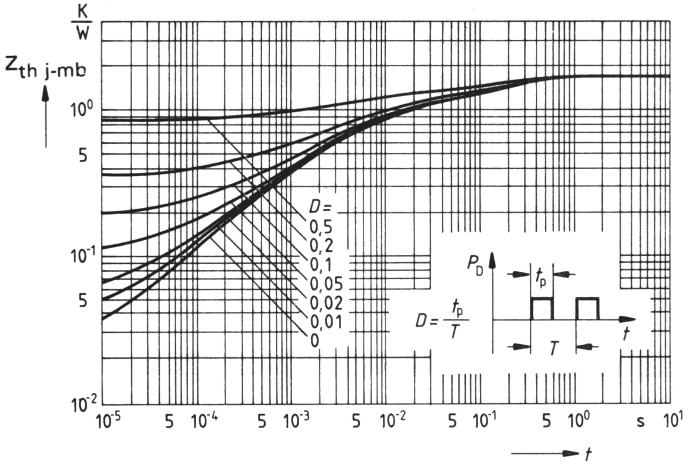


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

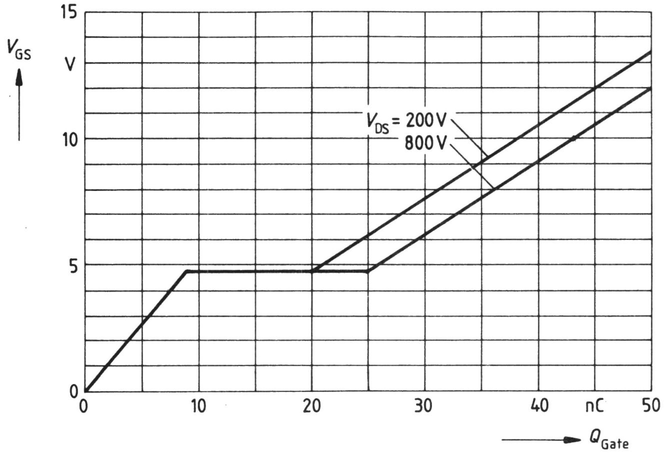


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 3,75 A.

PowerMOS transistor BUZ50C

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

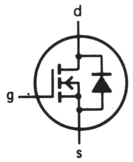
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,3	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	6,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 2 g

Pinning:
1 = Gate
2 = Drain
3 = Source



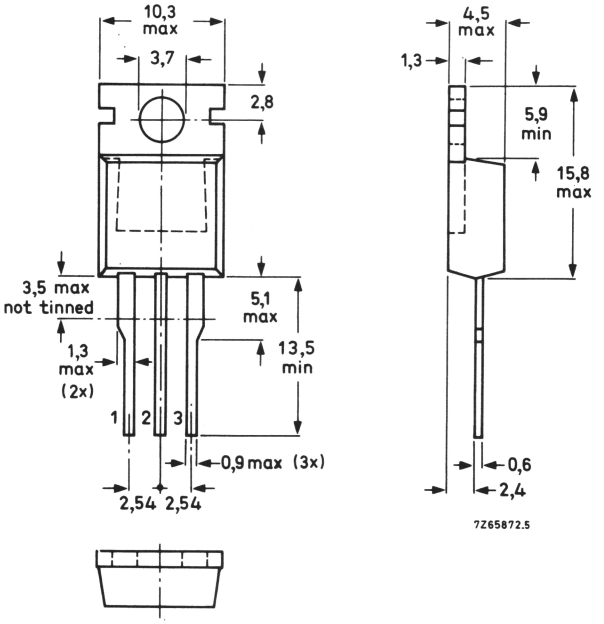

10,3 max
3,7
2,8
4,5 max
1,3
5,9 min
15,8 max
3,5 max not tinned
5,1 max
13,5 min
1,3 max (2x)
1
2
3
0,9 max (3x)
2,54
2,54
0,6
2,4
7Z65872.5

Fig. 1 *TO220AB; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO220 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20$ kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 25$ °C	–	2,3	A
I_D	Drain current (d.c.)	$T_{mb} = 100$ °C	–	1,5	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25$ °C	–	9,0	A
P_{tot}	Total power dissipation	$T_{mb} = 25$ °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1{,}67$ K/W
From junction to ambient	$R_{th\ j\text{-}a} = 75$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0{,}25$ mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 1000$ V; $V_{GS} = 0$ V; $T_j = 25$ °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 1000$ V; $V_{GS} = 0$ V; $T_j = 125$ °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 1{,}5$ A	–	5,0	6,0	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25$ °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 1{,}5$ A	0,7	1,5	–	S
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30$ V; $I_D = 1{,}9$ A; $V_{GS} = 10$ V; $R_{GS} = 50$ Ω; $R_{gen} = 50$ Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	3,5	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	4,5	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	7,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,3	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	9,0	A
V_{SD}	Diode forward on-voltage	I_F = 4,6 A; V_{GS} = 0 V	–	1,05	1,30	V
t_{rr}	Reverse recovery time	I_F = 2,3 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	2000	–	ns
Q_{rr}	Reverse recovery charge		–	15	–	μC

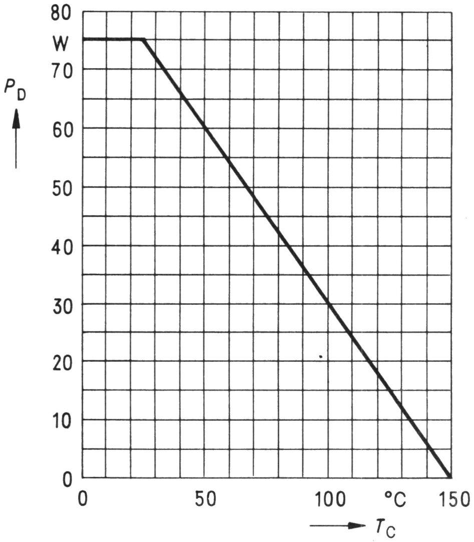


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

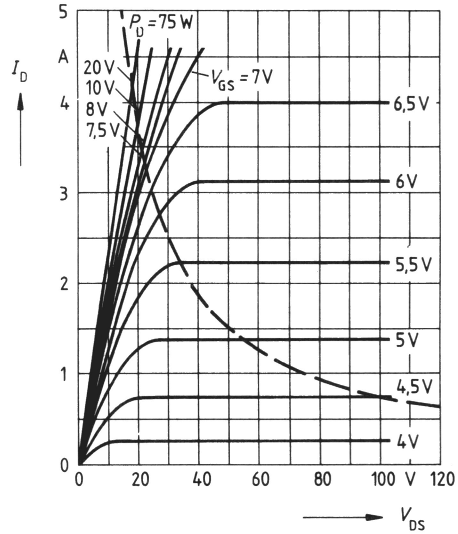


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

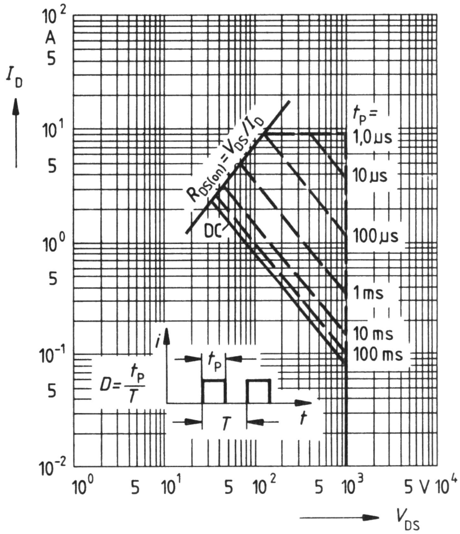


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

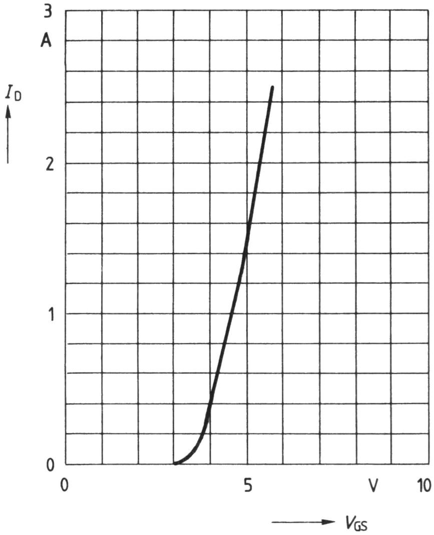


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

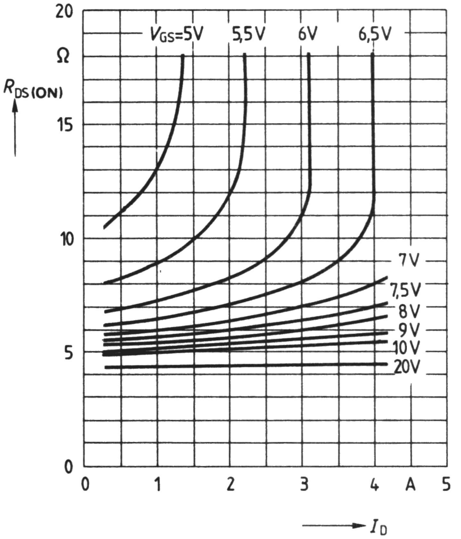


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

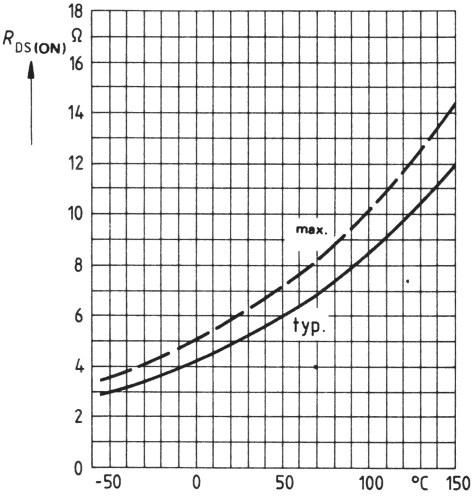


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

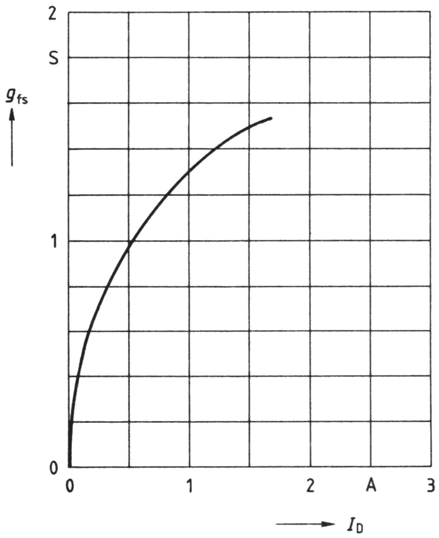


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

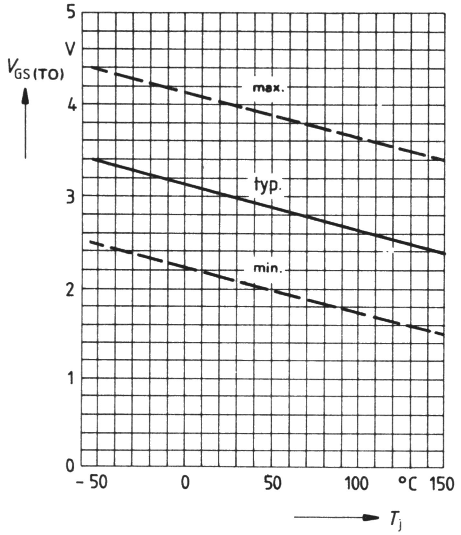


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

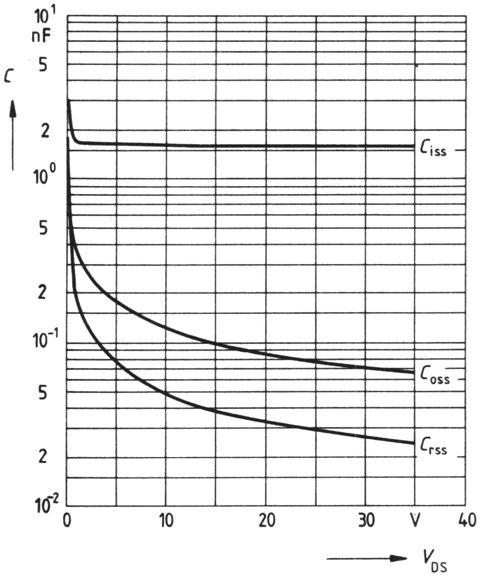


Fig. 10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

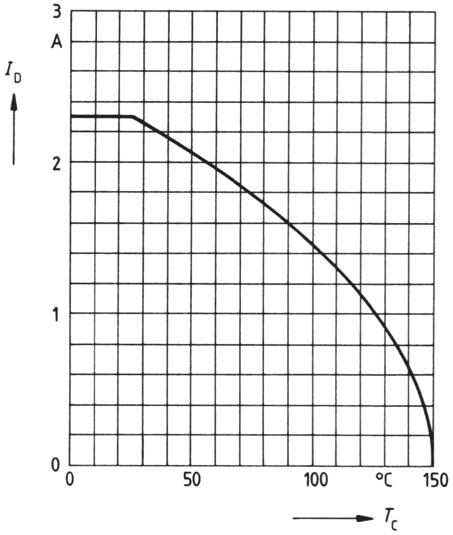


Fig. 11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

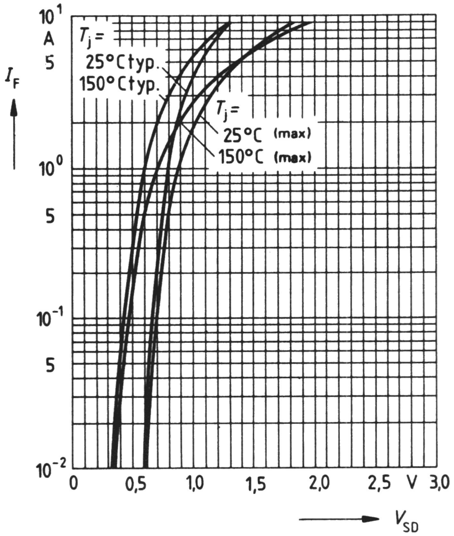


Fig. 12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *μs.*

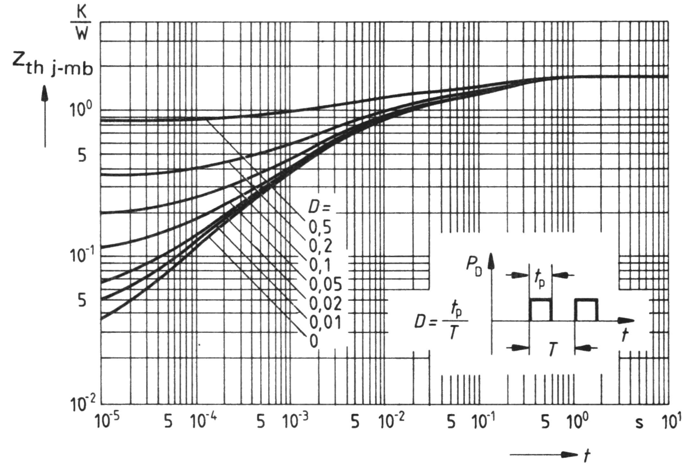


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

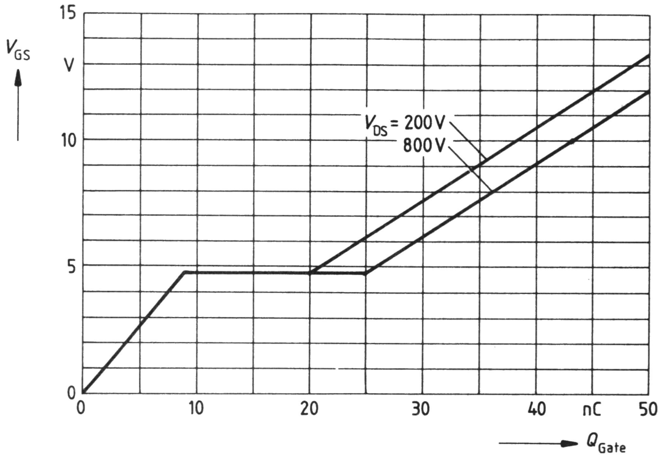


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 3,75$ A.

PowerMOS transistor

BUZ14

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

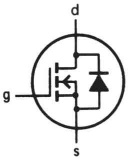
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	39	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,04	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



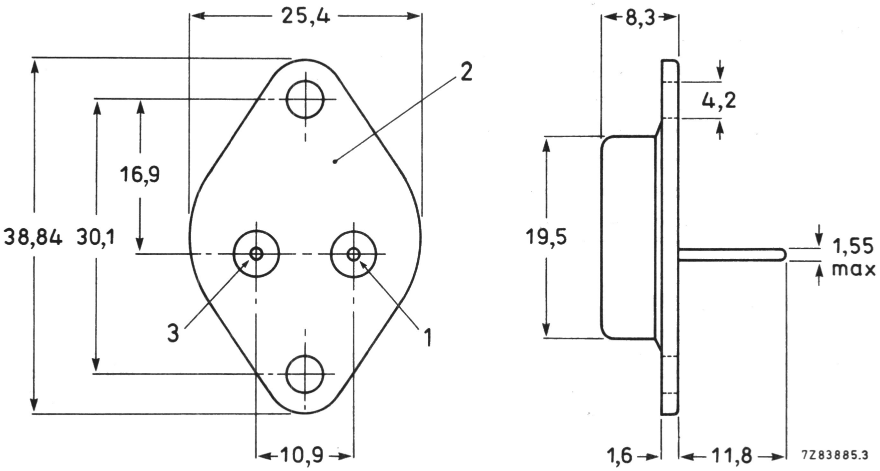


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	39	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	24,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	155	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	65	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A	–	0,035	0,04	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 22 A	7,0	18	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	1300	2000	pF
C_{rss}	Feedback capacitance		–	500	800	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	110	170	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	250	330	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	39	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	155	A
V_{SD}	Diode forward on-voltage	I_F = 78 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	2,2	V
t_{rr}	Reverse recovery time	I_F = 39 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 C;	–	150	–	ns
Q_{rr}	Reverse recovery charge	V_R = 30 V	–	1,0	–	μC

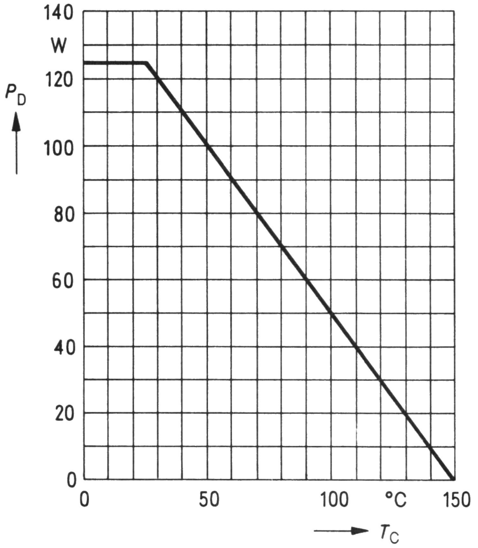


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

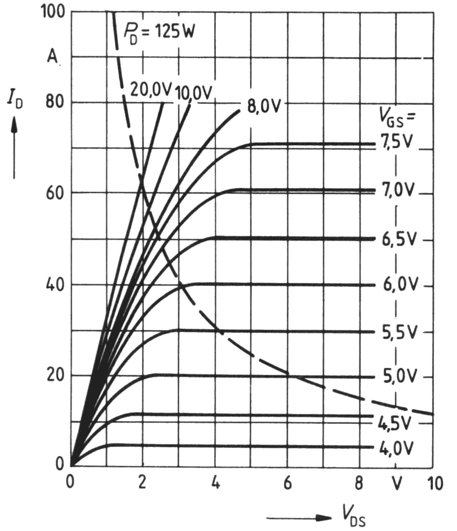


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

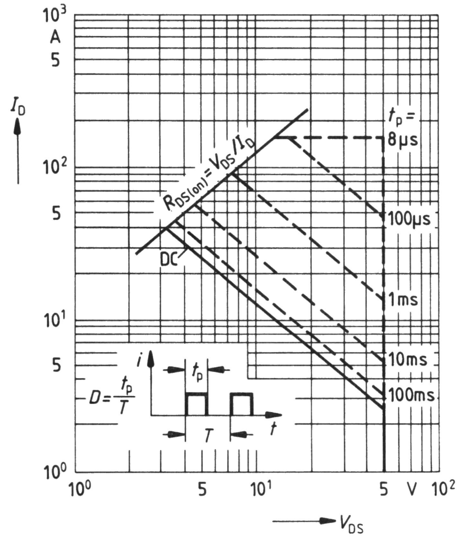


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

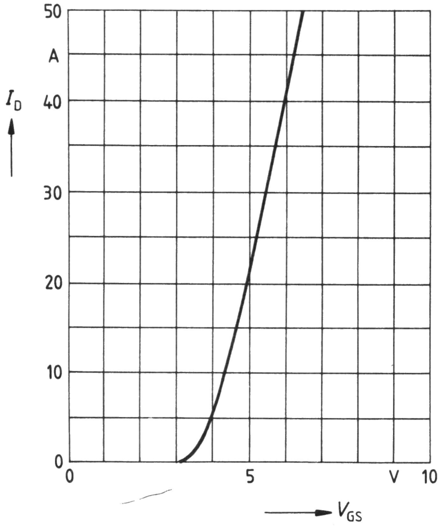


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

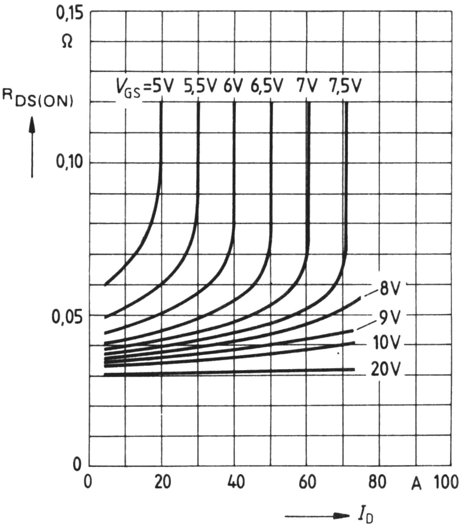


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

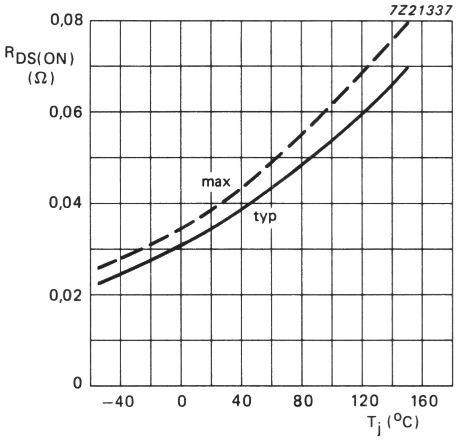


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 22\,A$; $V_{GS} = 10\,V$.

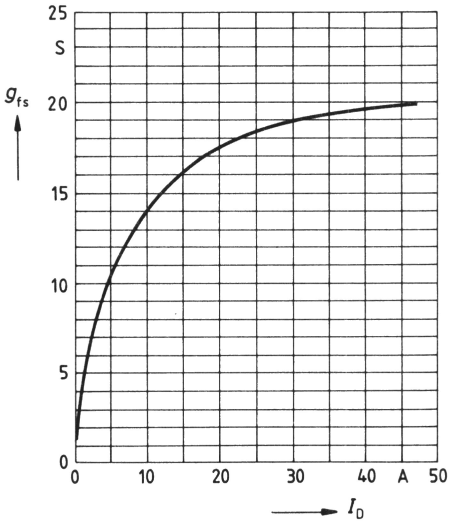


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\,V$; $T_j = 25\,°C$.

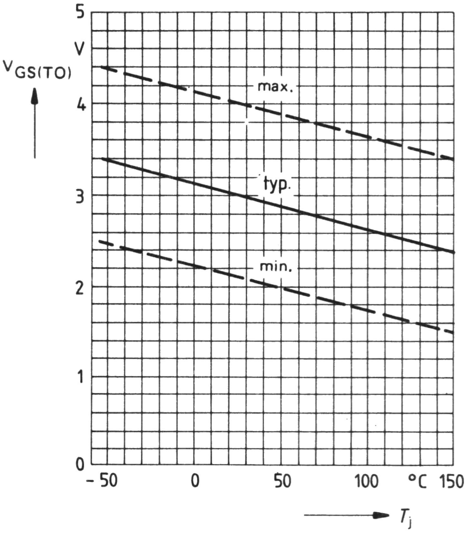


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

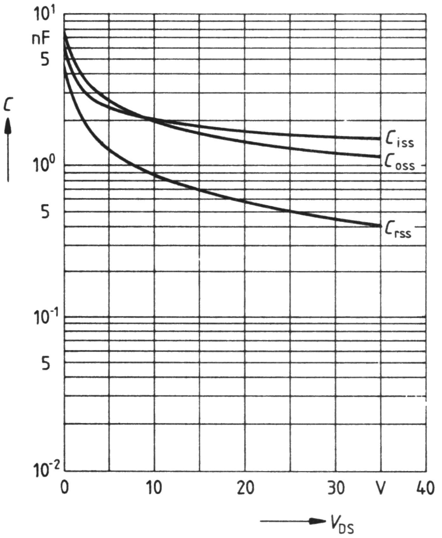


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

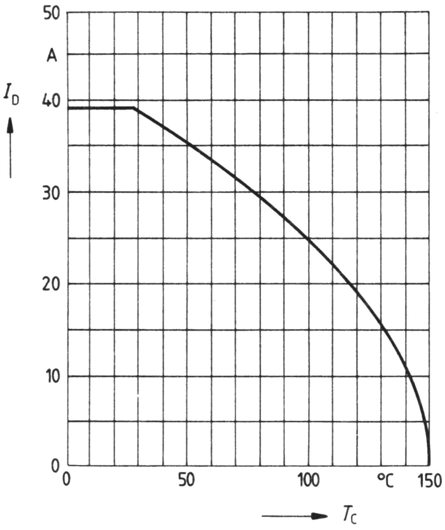


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

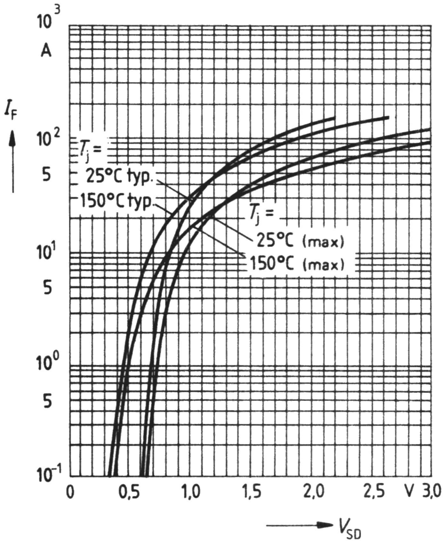


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

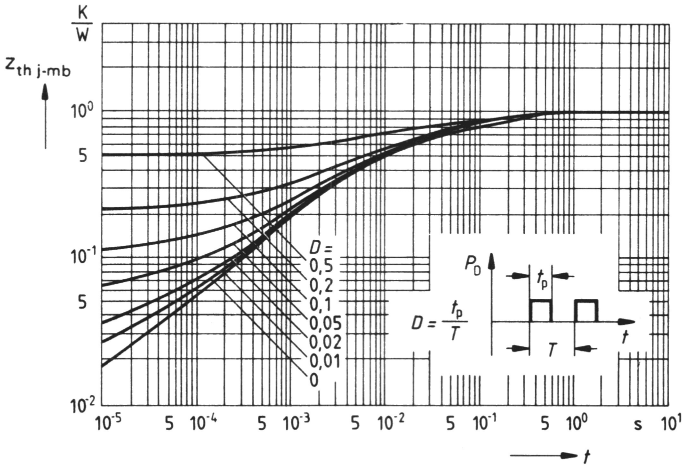


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

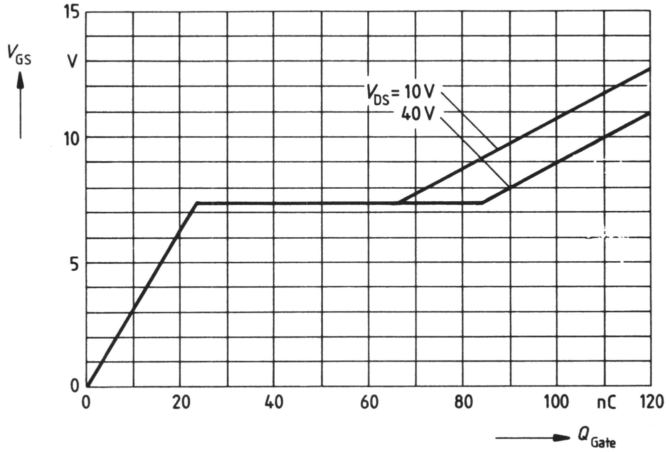


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 67{,}5$ A.

PowerMOS transistor BUZ15

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

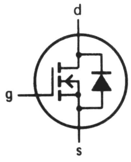
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	45	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,03	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



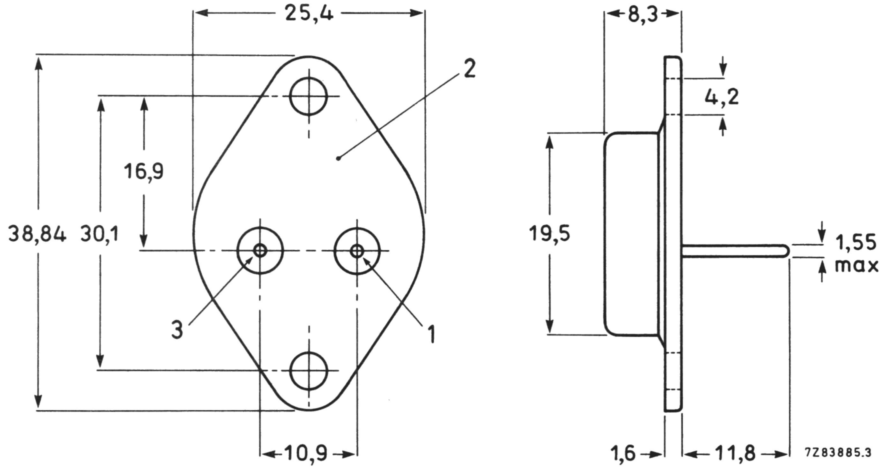


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	45	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	28,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	180	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	65	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 22 A	–	0,025	0,03	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 22 A	7,0	18	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	1300	2000	pF
C_{rss}	Feedback capacitance		–	500	800	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	110	170	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	250	330	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0		nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	45	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	180	A
V_{SD}	Diode forward on-voltage	I_F = 90 A; V_{GS} = 0 V T_j = 25 °C	–	1,6	2,4	V
t_{rr}	Reverse recovery time	I_F = 45 A; T_j = 25 °C $-dI_F/dt$ = 100 A/µs; T_j = 25 °C V_{GS} = 0 V;	–	150	–	ns
$-Q_{rr}$	Reverse recovery charge	V_R = 30 V	–	1,0	–	µC

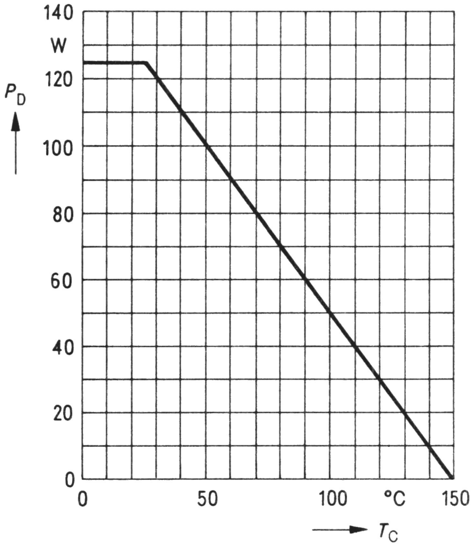


Fig.2 Power dissipation $P_D = f(T_{mb})$.

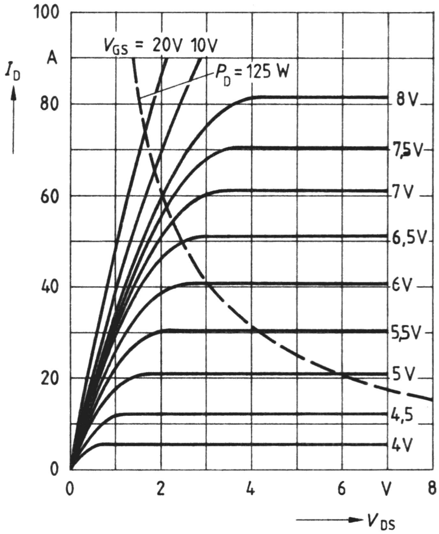


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25\,°C$.

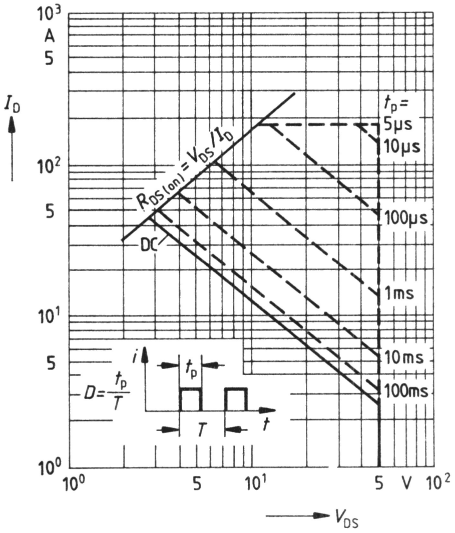


Fig.4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\,°C$.

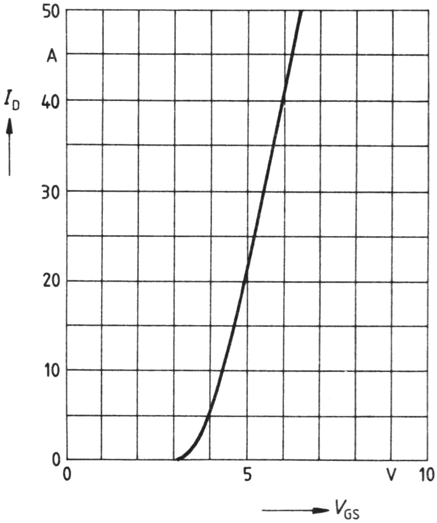


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25\,°C$.

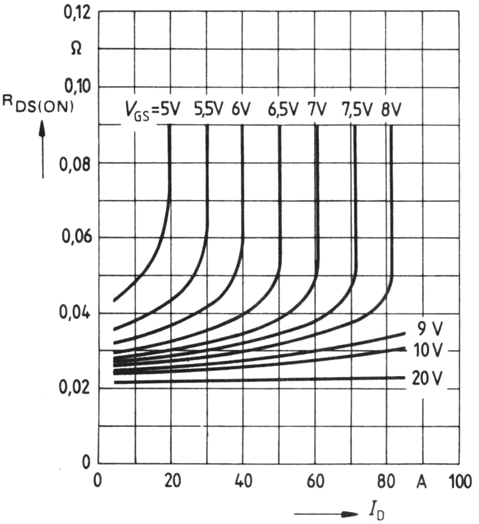


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

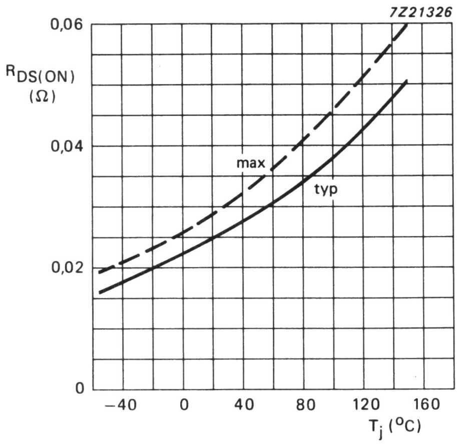


Fig.7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 22\,A$; $V_{GS} = 10\,V$.

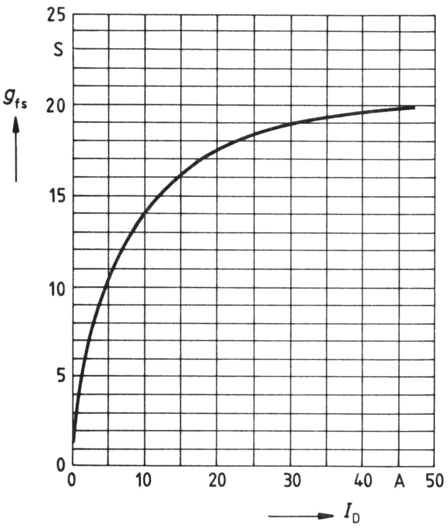


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\,V$; $T_j = 25\,°C$.

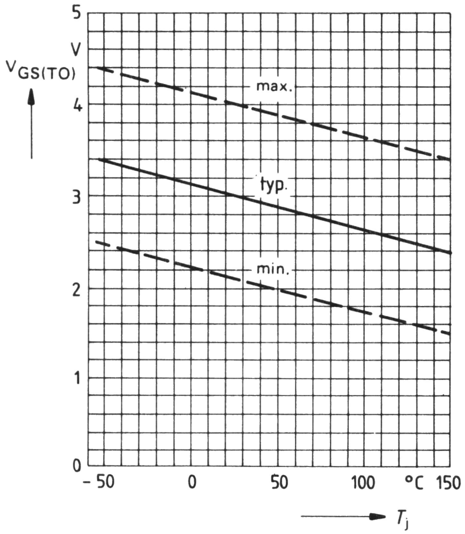


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$.
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

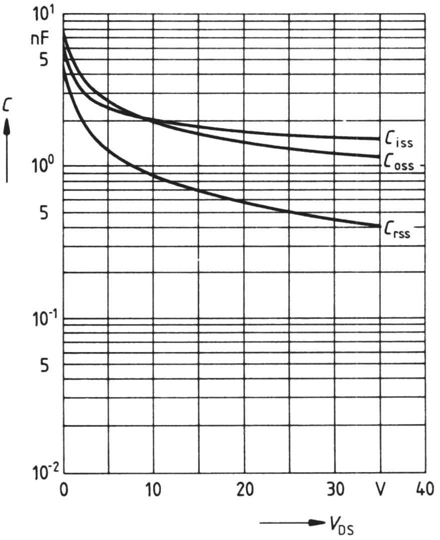


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

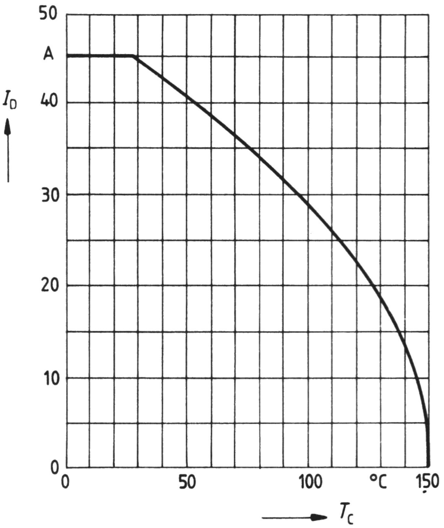


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

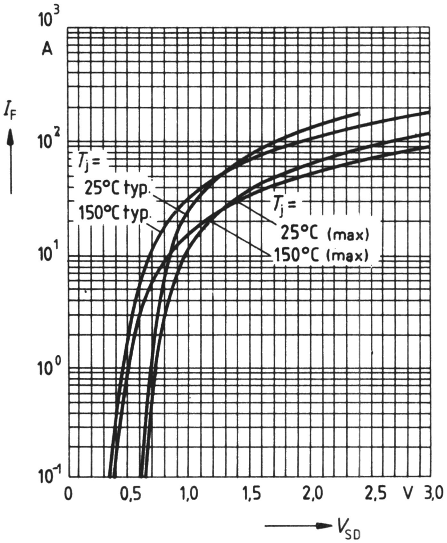


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

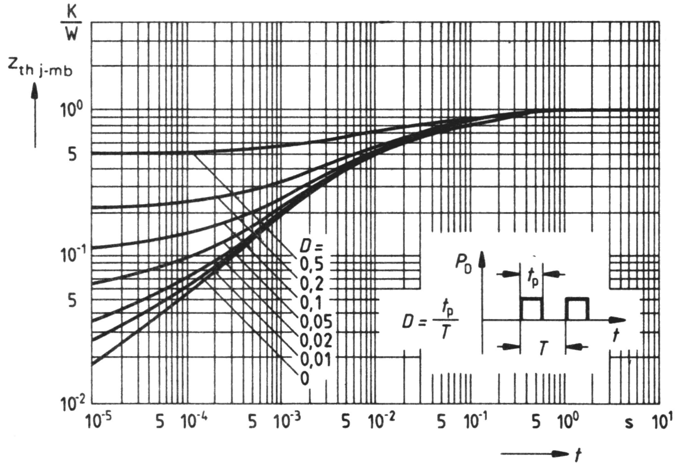


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

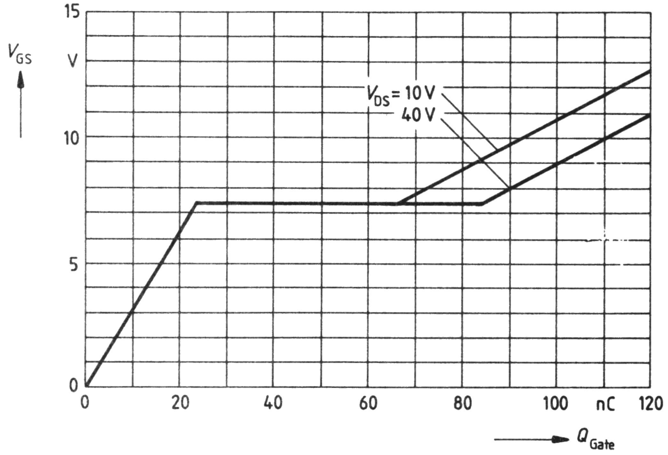


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 67,5 A.

PowerMOS transistor BUZ23

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

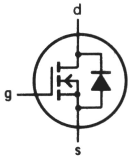
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	10	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,2	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



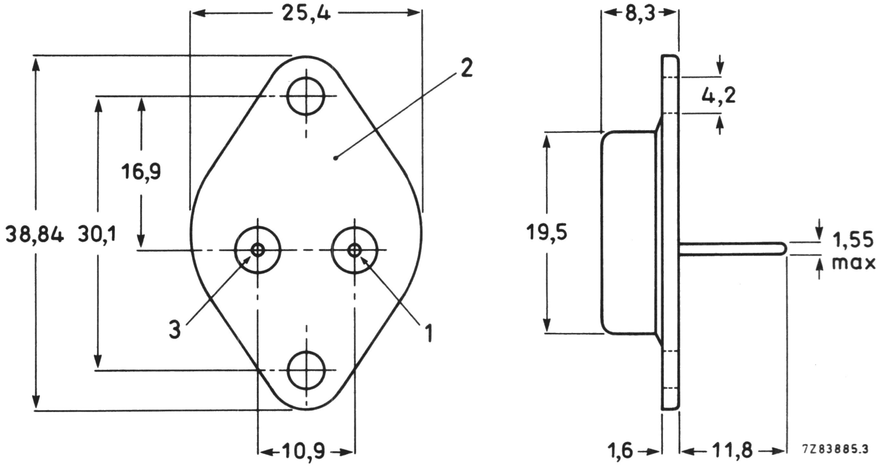


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain-current (d.c.)	T_{mb} = 85 °C	–	10	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	8,8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6 A	–	0,15	0,2	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6 V	2,7	4,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	300	500	pF
C_{rss}	Feedback capacitance		–	80	140	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	50	75	ns
$t_{d\,off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	10	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	40	A
V_{SD}	Diode forward on-voltage	I_F = 20 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,6	V
t_{rr}	Reverse recovery time	I_F = 10 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 30 V	–	1,6	–	μC

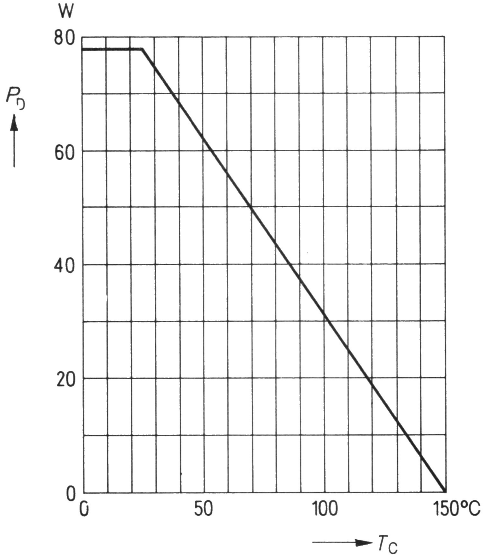


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

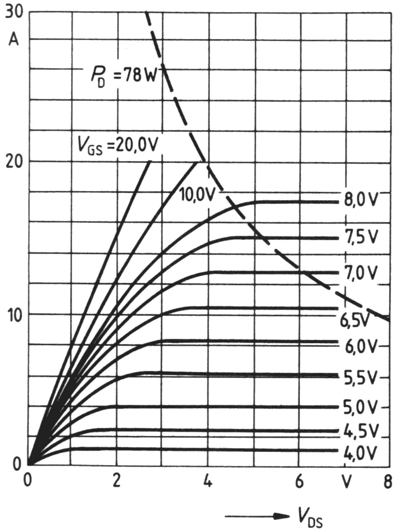


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

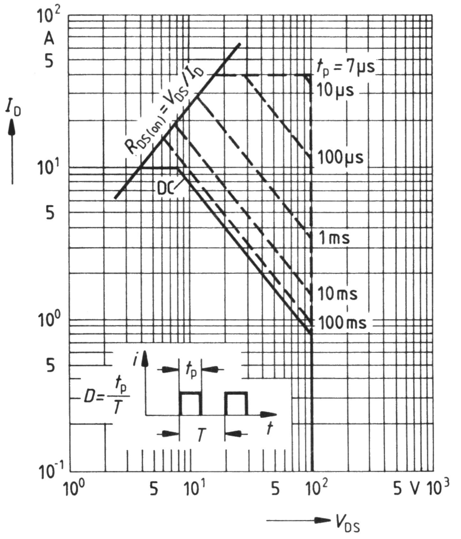


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

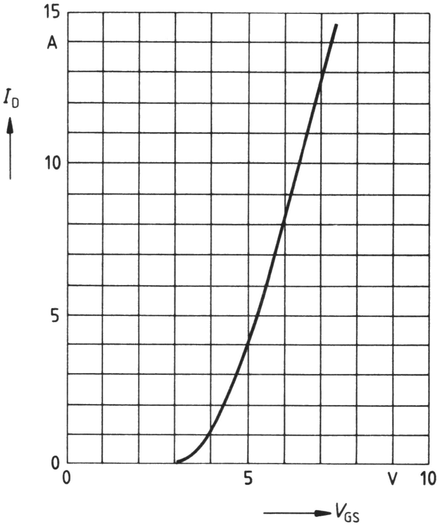


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

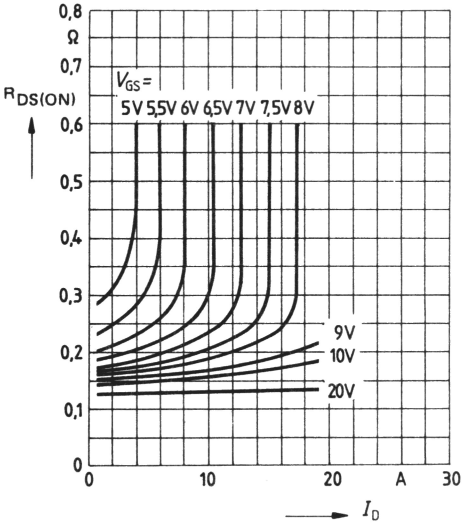


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

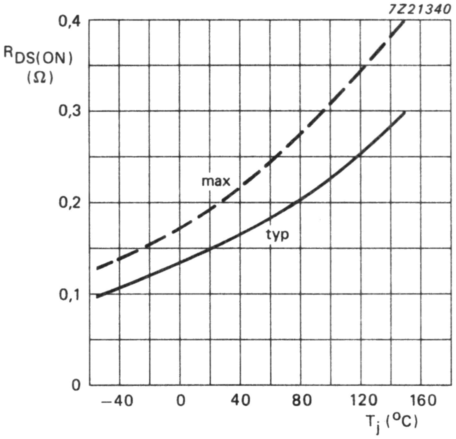


Fig. 7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 6\ A$; $V_{GS} = 10\ V$.

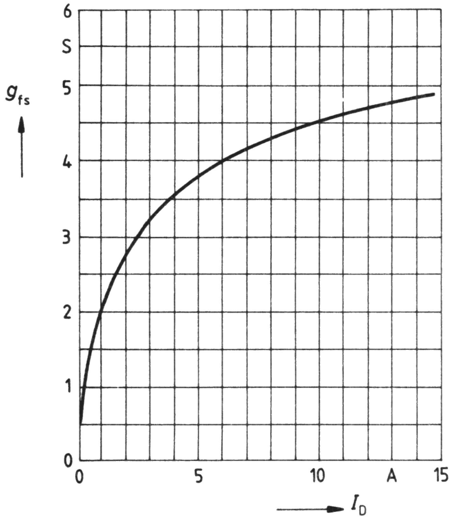


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\,°C$.

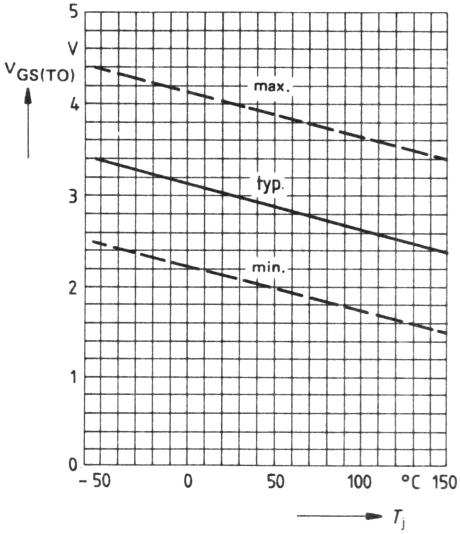


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

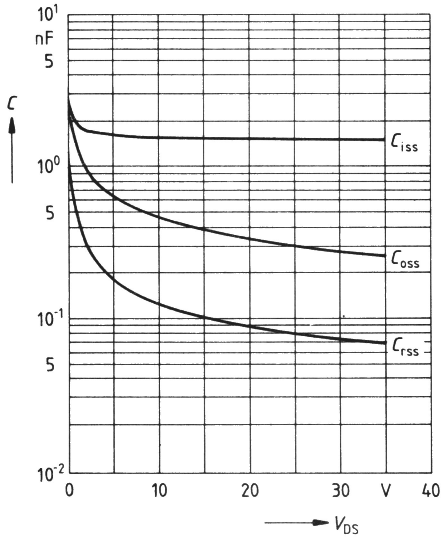


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

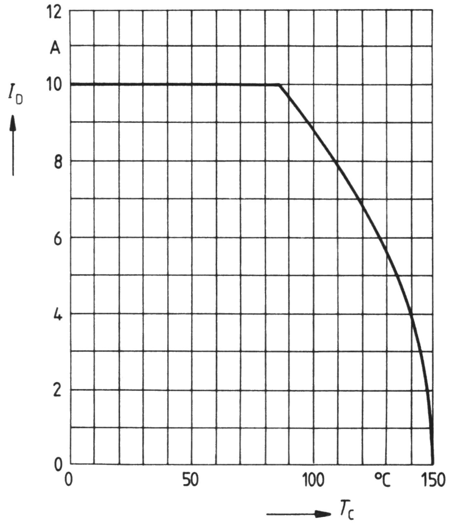


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

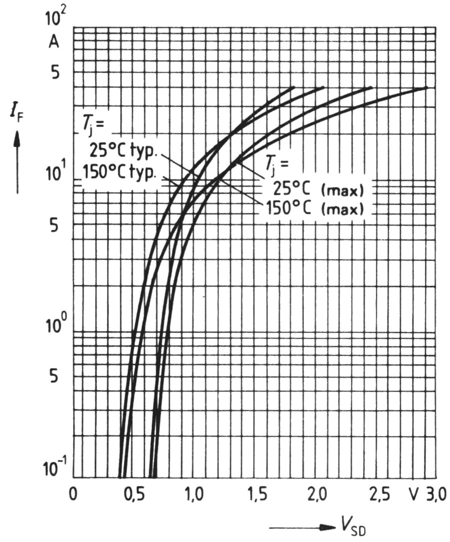


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

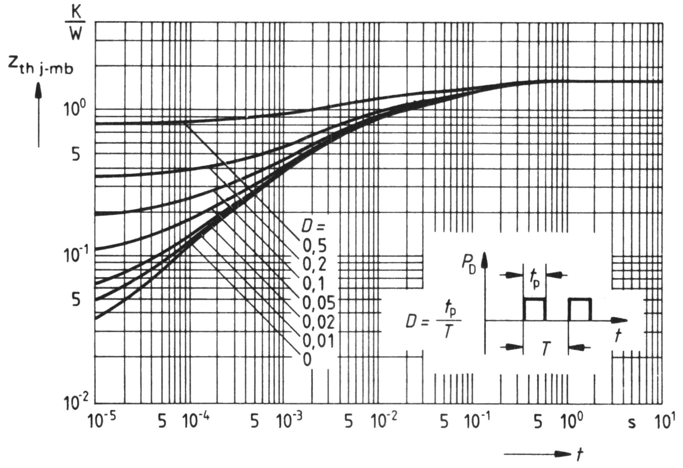


Fig.13 *Transient thermal impedance* $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

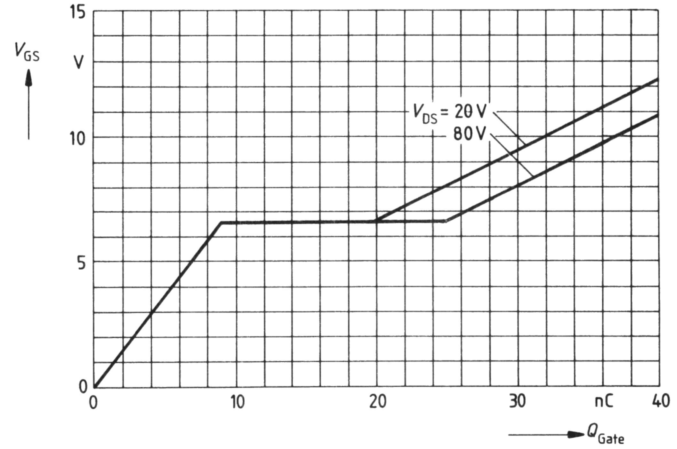


Fig.14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; *IDM = 18 A.*

PowerMOS transistor BUZ24

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	32	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,06	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source

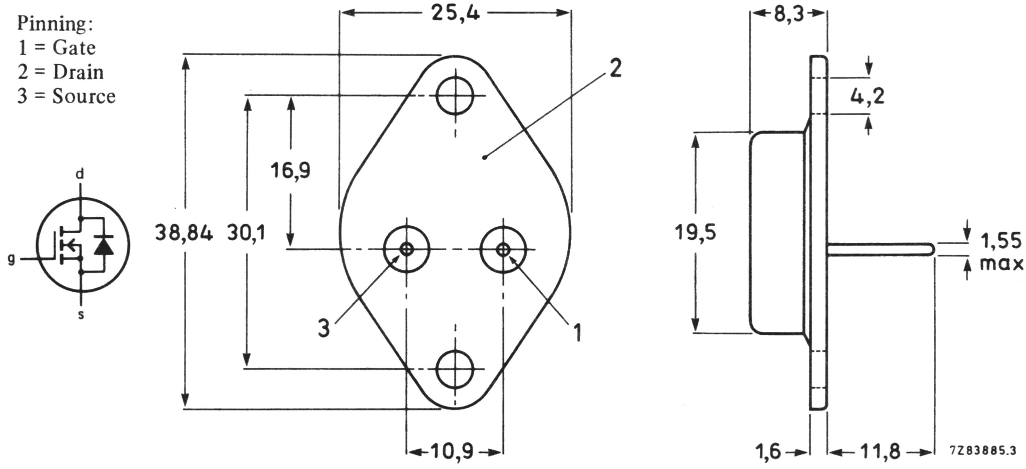


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain-current (d.c.)	T_{mb} = 25 °C	–	32	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	20,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	125	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 16 A	–	0,045	0,06	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 16 A	6,0	10,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	800	1200	pF
C_{rss}	Feedback capacitance		–	300	500	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	170	220	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	32	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	125	A
V_{SD}	Diode forward on-voltage	I_F = 64 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	2,0	V
t_{rr}	Reverse recovery time	I_F = 32 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 30 V	–	1,6	–	μC

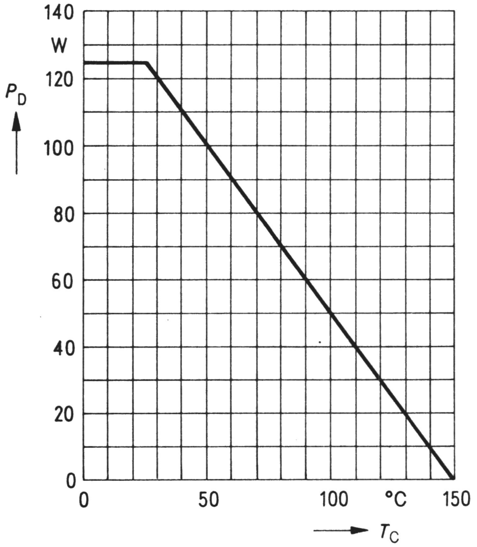


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

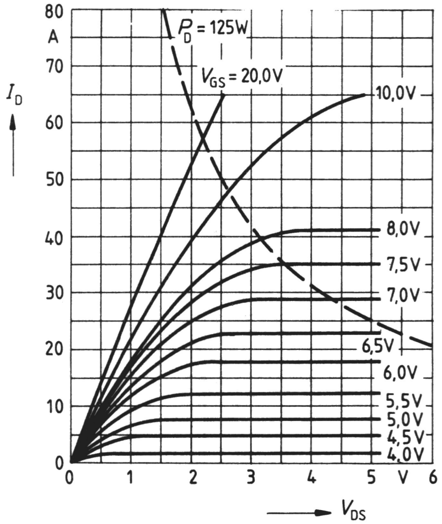


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

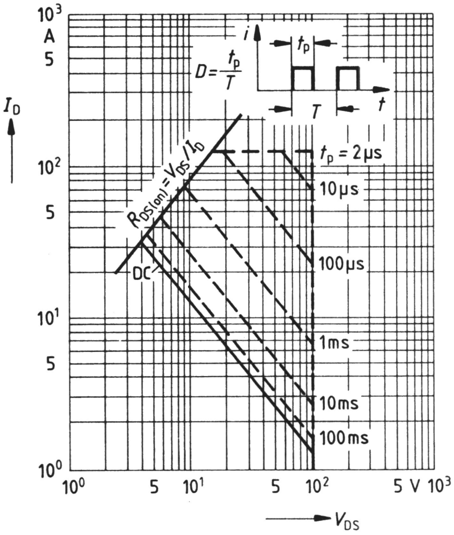


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

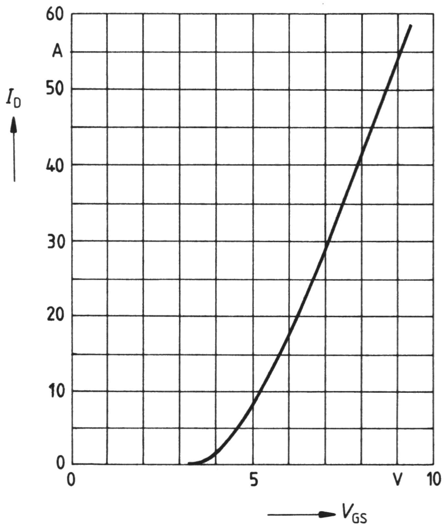


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

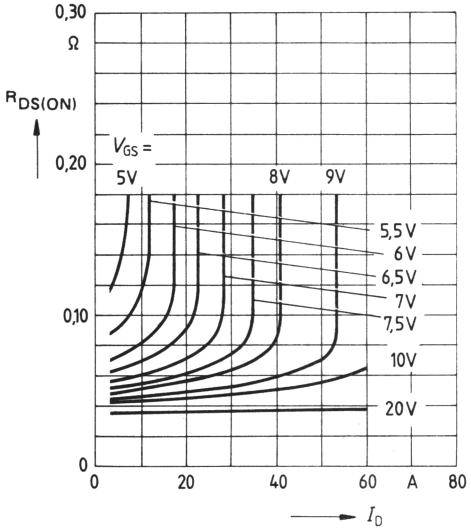


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; $T_j = 25\,°C$.*

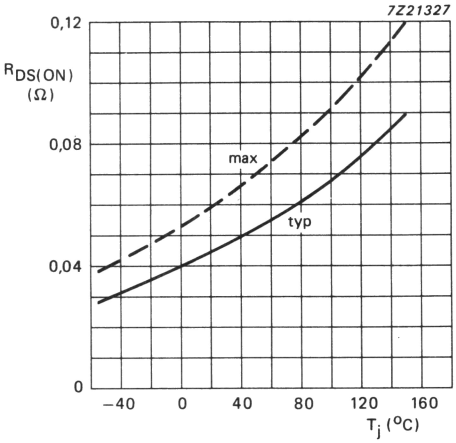


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: $I_D = 16$ A; $V_{GS} = 10$ V.*

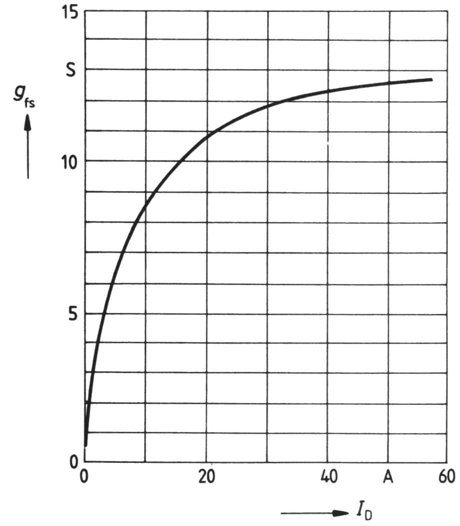


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 μs pulse test; $V_{DS} = 25$ V; $T_j = 25\,°C$.*

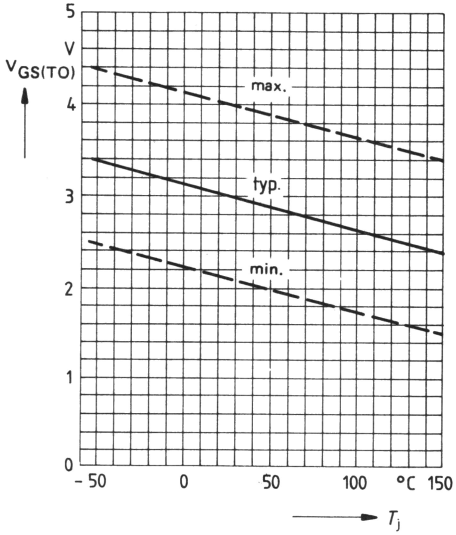


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.*

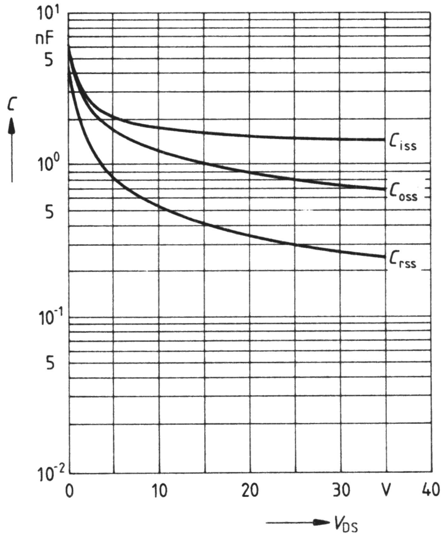


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

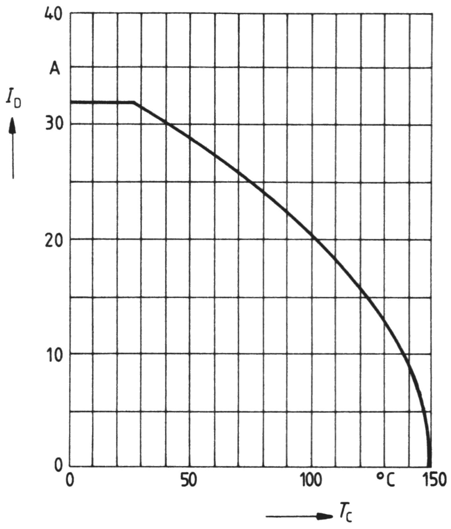


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

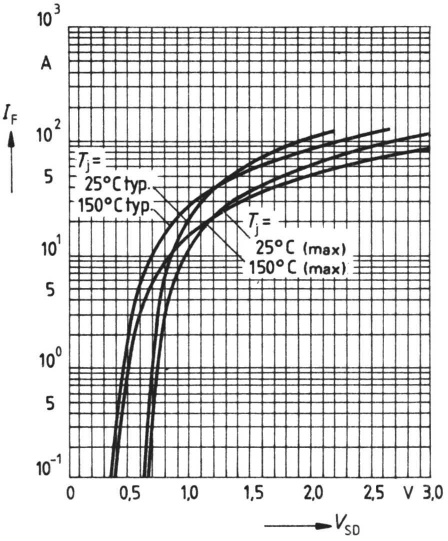


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

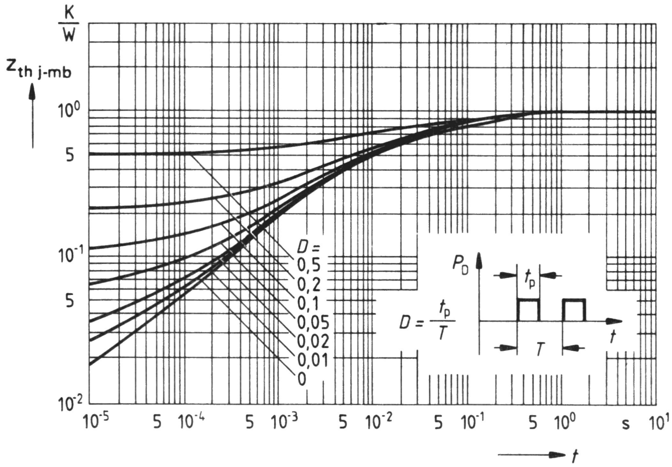


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

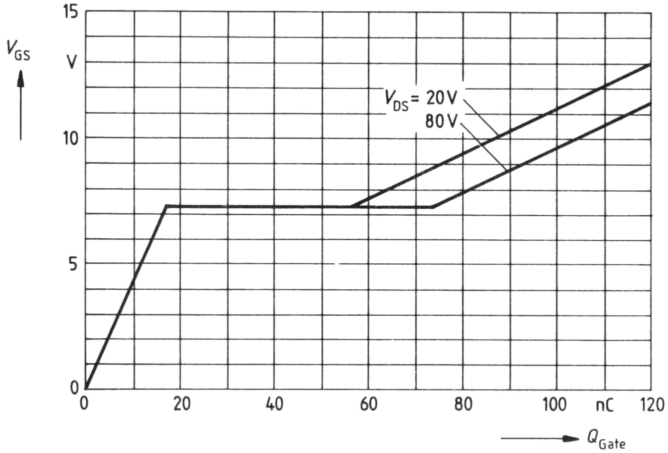


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 48A$.

PowerMOS transistor BUZ25

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

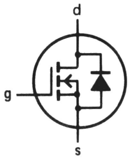
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	19	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,1	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



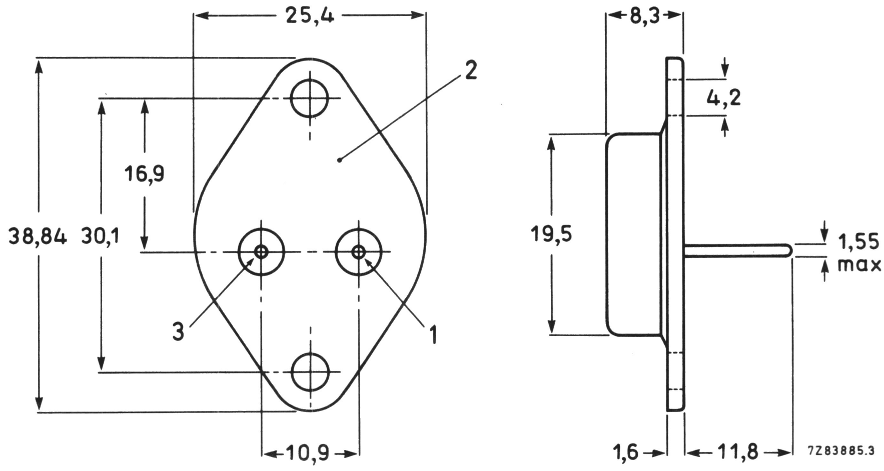


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain-current (d.c.)	T_{mb} = 35 °C	–	19	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	12,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	75	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature		–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 9 A	–	0,09	0,1	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 9 A	4,0	8,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	450	700	pF
C_{rss}	Feedback capacitance		–	150	240	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	50	75	ns
$t_{d\,off}$	Turn-off delay time		–	170	220	ns
t_f	Turn-off fall time		–	80	110	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	19	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	75	A
V_{SD}	Diode forward on-voltage	I_F = 38 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	2,1	V
t_{rr}	Reverse recovery time	I_F = 19 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 30 V	–	0,25	–	μC

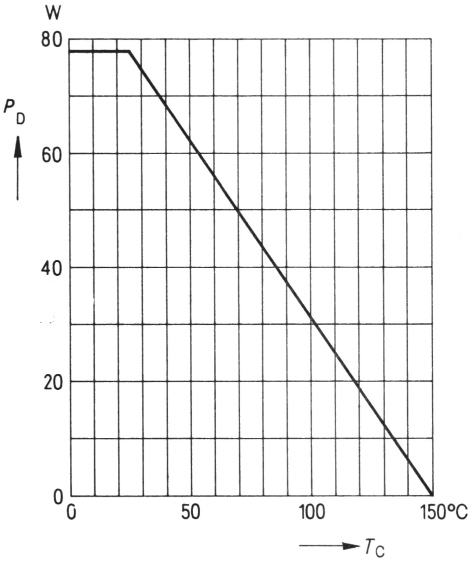


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

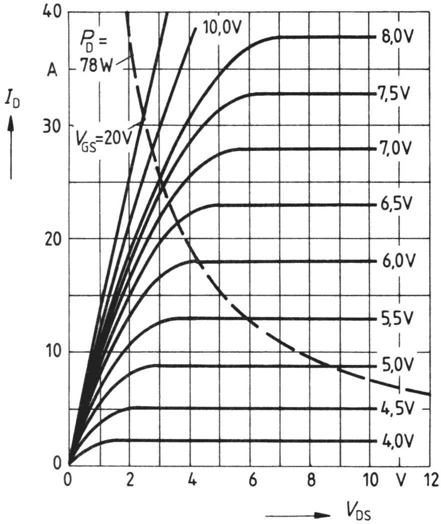


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

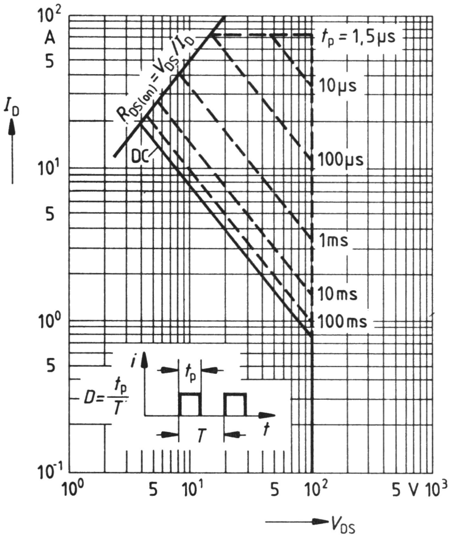


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

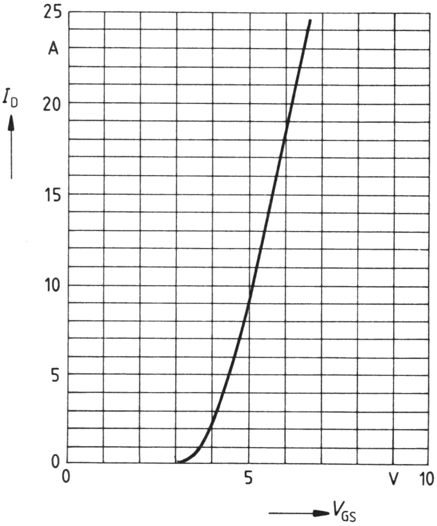


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

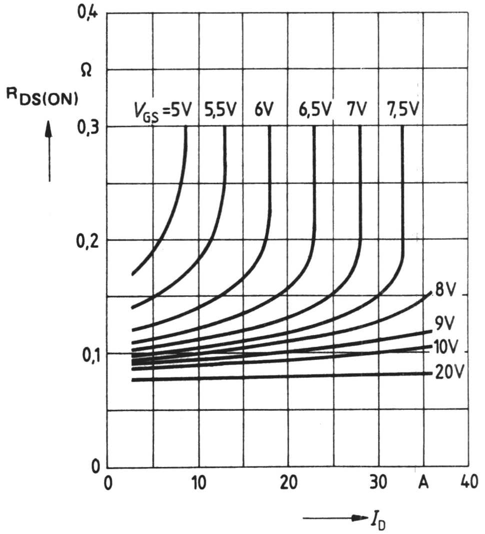


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; T_j = 25 °C.*

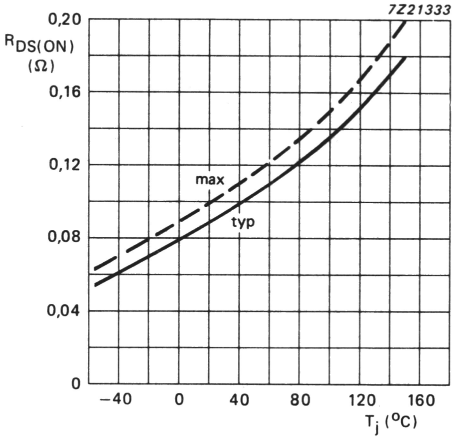


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: I_D = 9 A; V_{GS} = 10 V.*

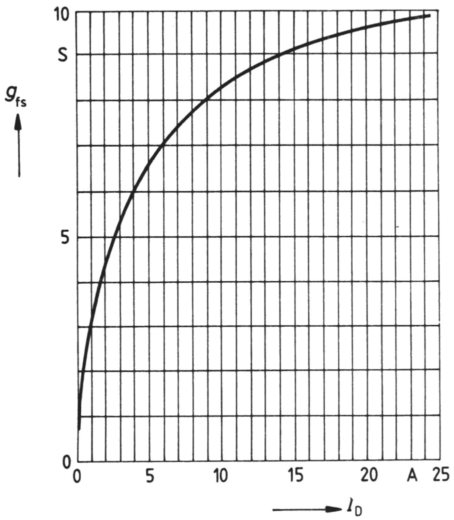


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 µs pulse test; V_{DS} = 25 V; T_j = 25 °C.*

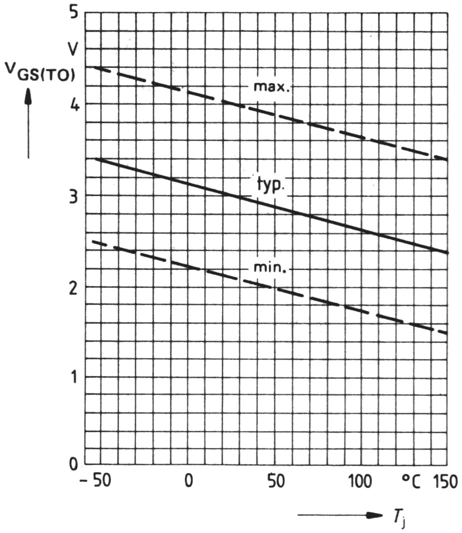


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.*

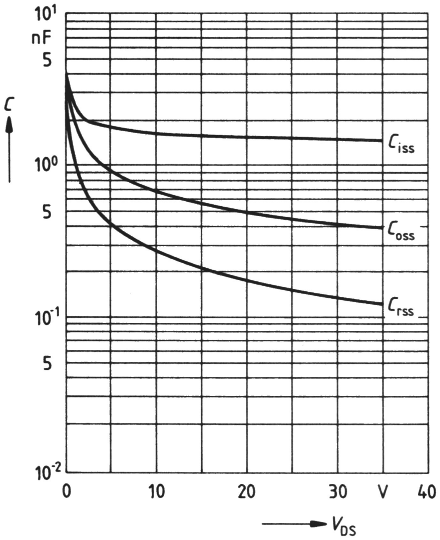


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

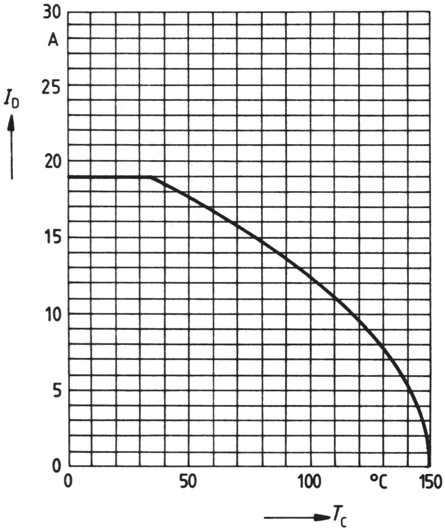


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

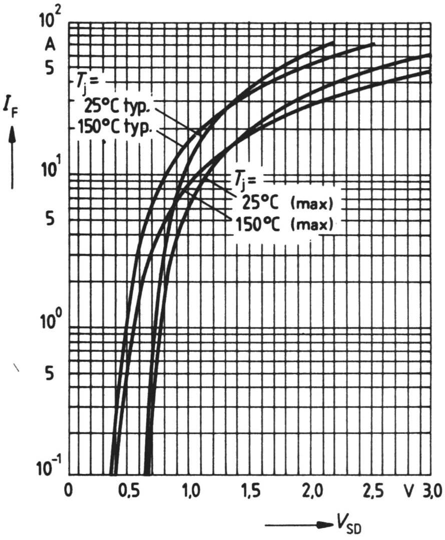


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

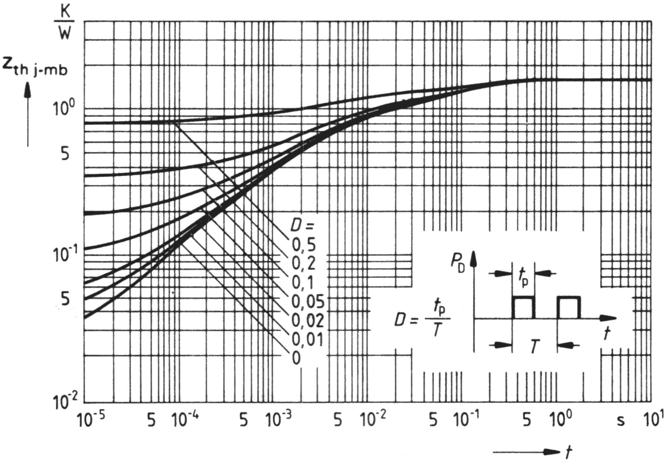


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

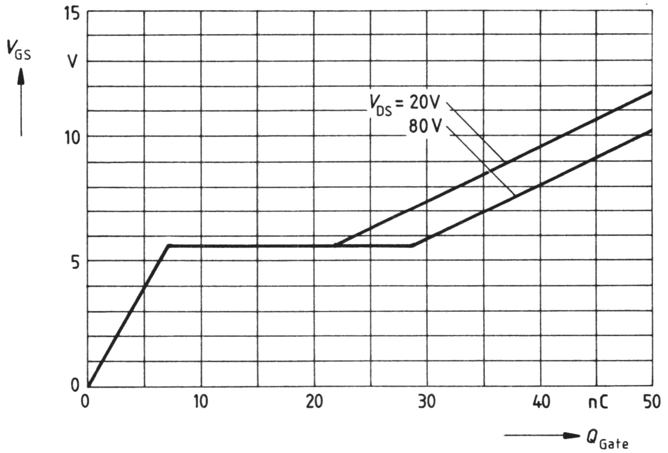


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 28,5 A.

PowerMOS transistor BUZ34

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

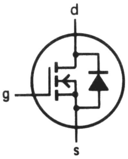
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	14	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,2	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



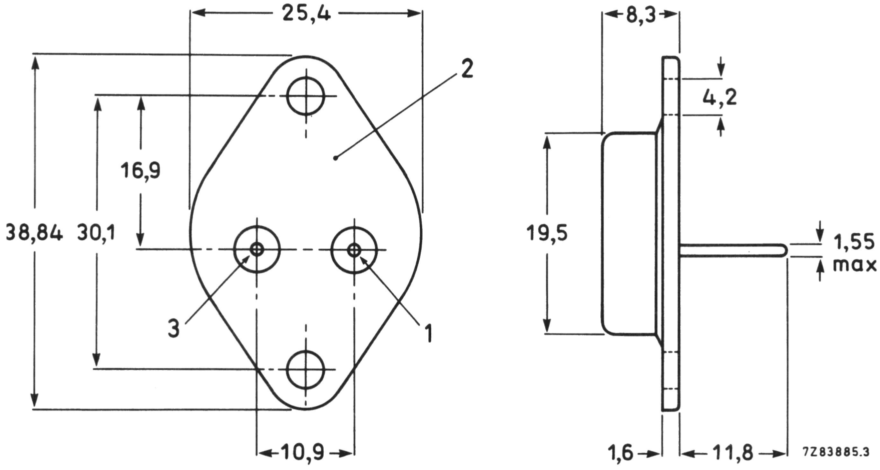


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\,k\Omega$	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 25\,°C$	–	14	A
I_D	Drain current (d.c.)	$T_{mb} = 100\,°C$	–	8,9	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\,°C$	–	56	A
P_{tot}	Total power dissipation	$T_{mb} = 25\,°C$	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb} = 1{,}6$ K/W
From junction to ambient	$R_{th\,j\text{-}a} = 35$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25\,°C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0{,}25$ mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 25\,°C$	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 125\,°C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 7$ A	–	0,17	0,2	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\,°C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 7$ A	3,0	5,0	–	S
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; f = 1 MHz	–	900	1400	pF
C_{oss}	Output capacitance		–	300	500	pF
C_{rss}	Feedback capacitance		–	140	250	pF
$t_{d\,on}$	Turn-on delay time	$V_{DD} = 30$ V; $I_D = 2{,}9$ A; $V_{GS} = 10$ V; $R_{GS} = 50\,\Omega$; $R_{gen} = 50\,\Omega$	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\,off}$	Turn-off delay time		–	170	220	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	14	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	56	A
V_{SD}	Diode forward on-voltage	I_F = 28 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	1,9	V
t_{rr}	Reverse recovery time	I_F = 14 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	400	–	ns
Q_{rr}	Reverse recovery charge	V_R = 100 V	–	6,0	–	μC

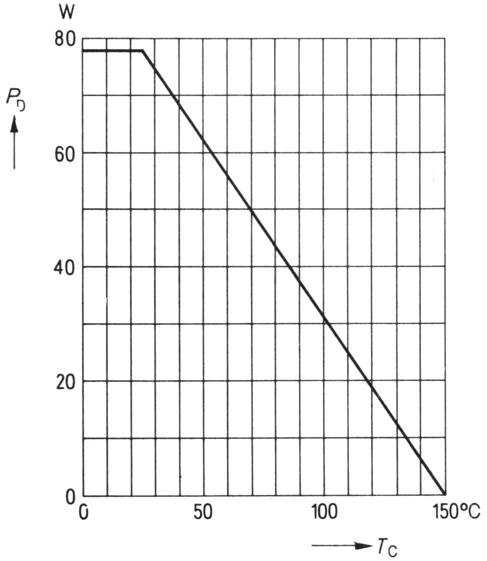


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

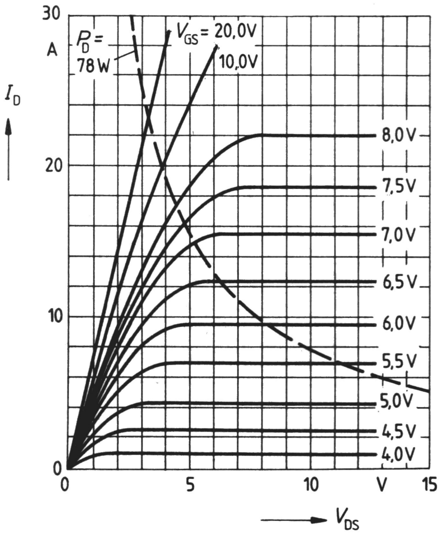


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$
Parameter: V_{GS}; *80 µs pulse test;*
$T_{mb} = 25\,°C$.

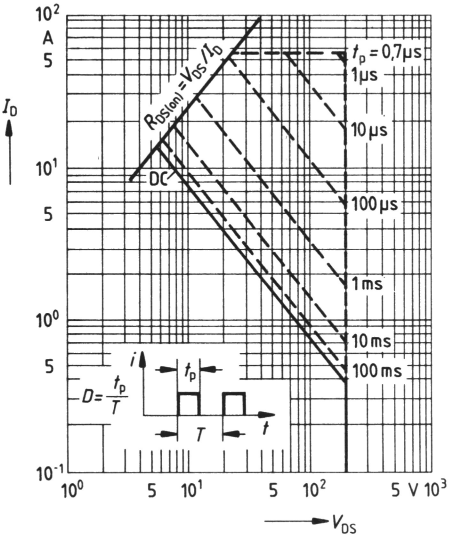


Fig.4 *Safe operating area* I_D*(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\,°C$.

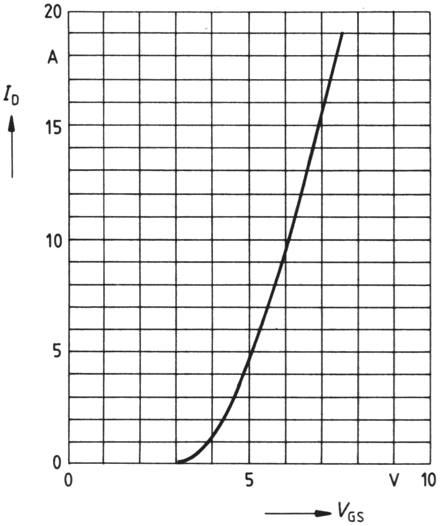


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ *V,*
$T_{mb} = 25\,°C$.

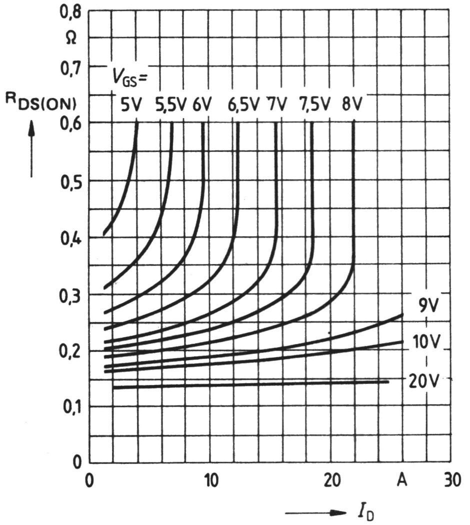


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; $T_j = 25\,°C$.

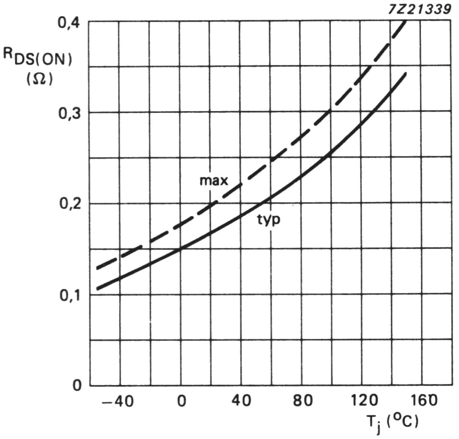


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* $I_D = 7\,A$; $V_{GS} = 10\,V$.

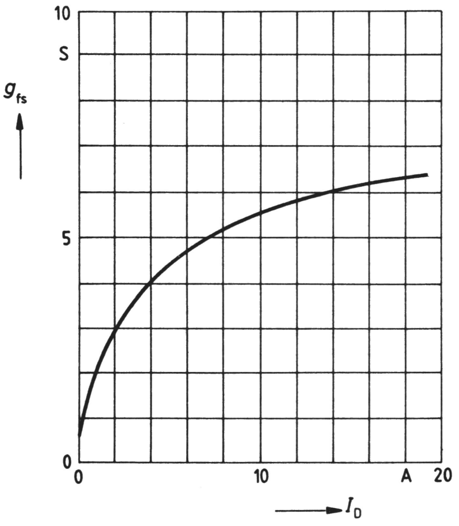


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 µs pulse test;* $V_{DS} = 25\,V$; $T_j = 25\,°C$.

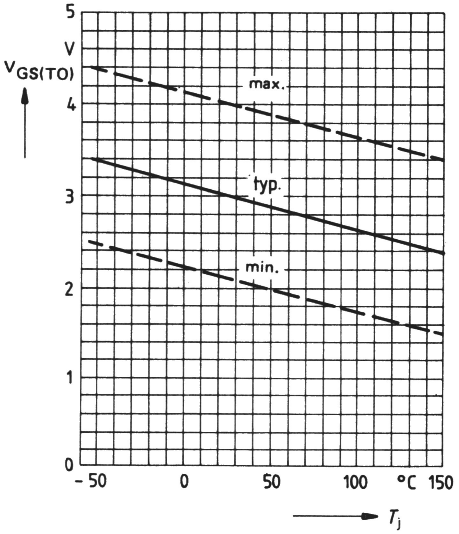


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

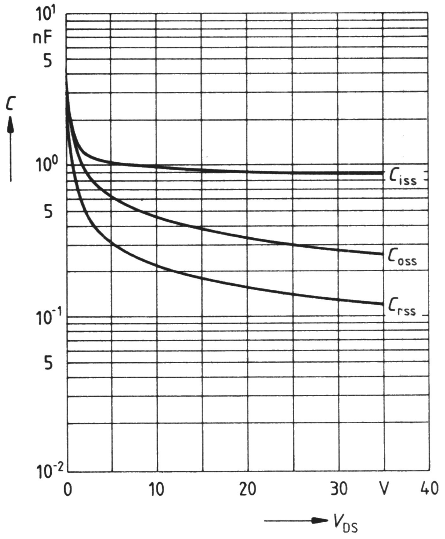


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

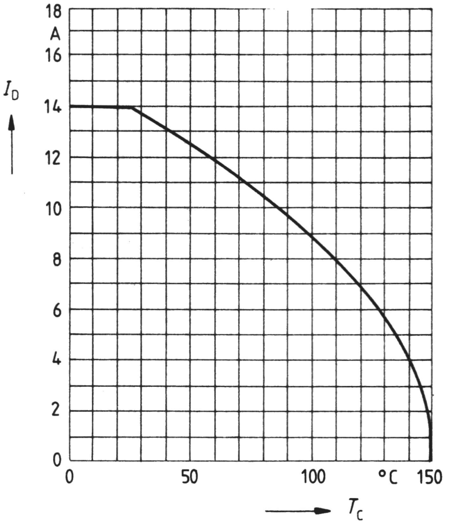


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

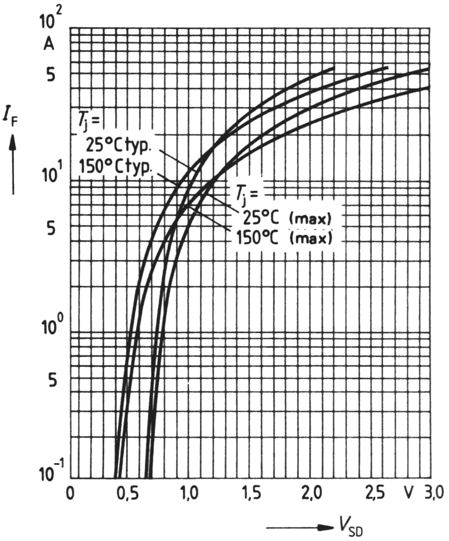


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

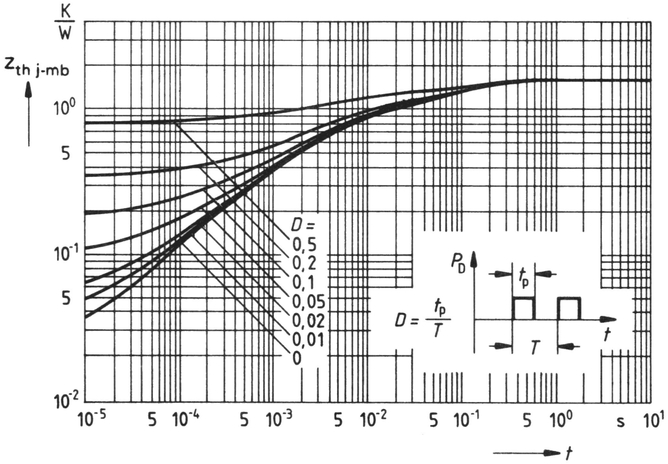


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$ Parameter: $D = t_p/T$.

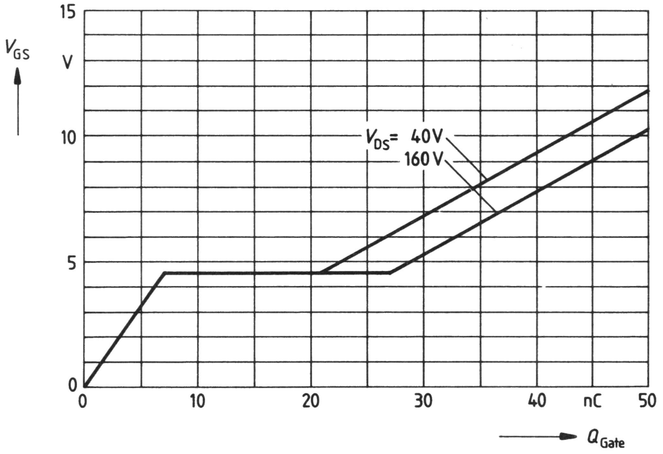


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$ Parameter: V_{DS}; $I_{DM} = 18{,}8$ A.

PowerMOS transistor BUZ35

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

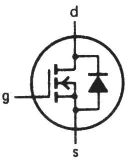
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	9,9	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,4	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



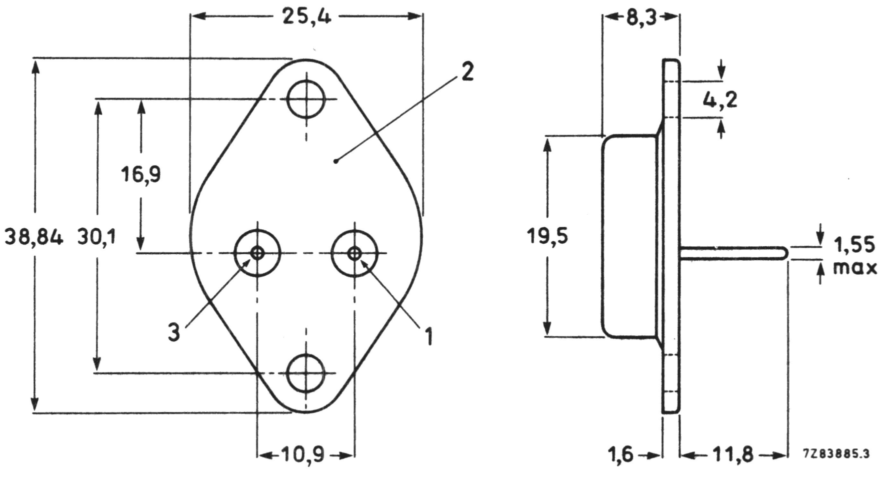


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	9,9	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	39	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 200 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 4,5 A	–	0,35	0,4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 4,5 A	2,2	5,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	70	120	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\,off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	9,9	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	39	A
V_{SD}	Diode forward on-voltage	I_F = 19,8 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 9,9 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	400	–	ns
Q_{rr}	Reverse recovery charge	V_R = 100 V	–	6,0	–	μC

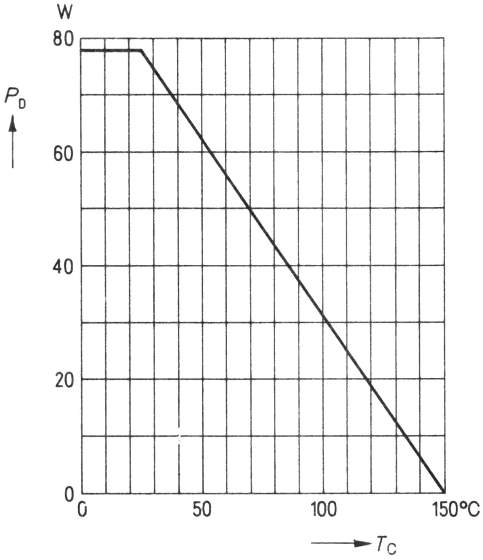


Fig.2 Power dissipation $P_D = f(T_{mb})$.

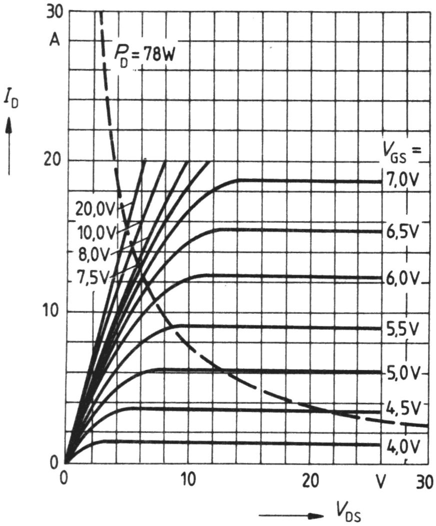


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25\,°C$.

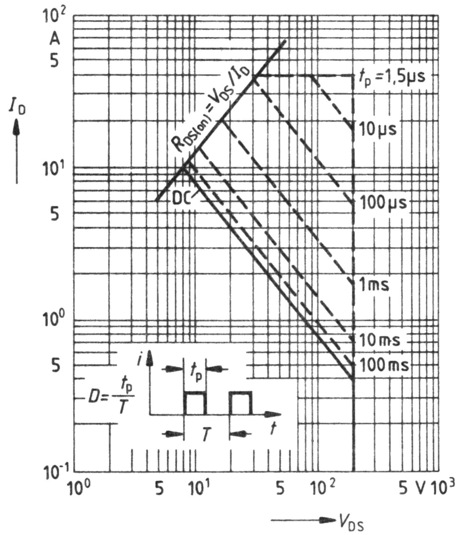


Fig.4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; $T_{mb} = 25\,°C$.

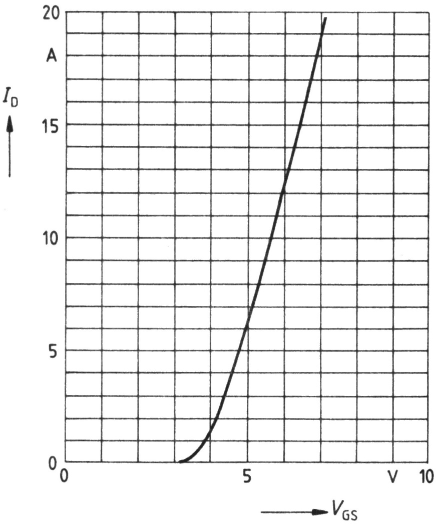


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25\,°C$.

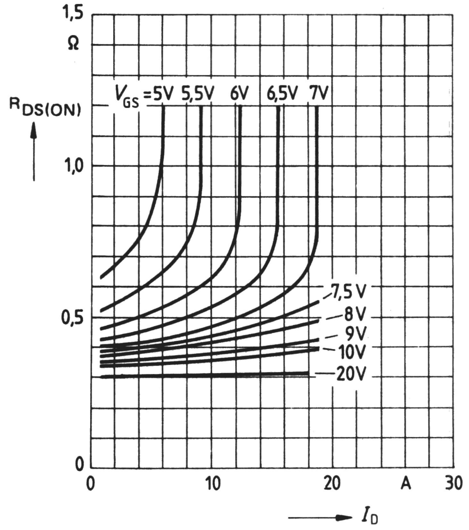


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$*
Parameter: V_{GS}; $T_j = 25\,°C$.

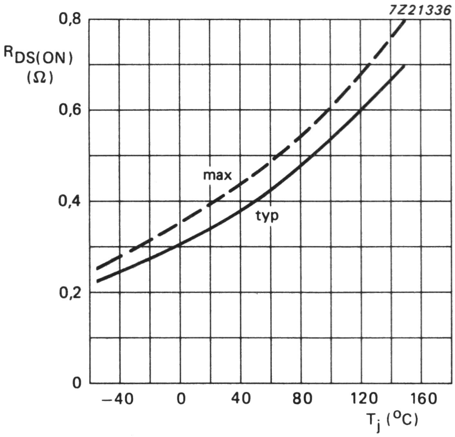


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$*
Conditions: $I_D = 4{,}5$ A; $V_{GS} = 10$ V.

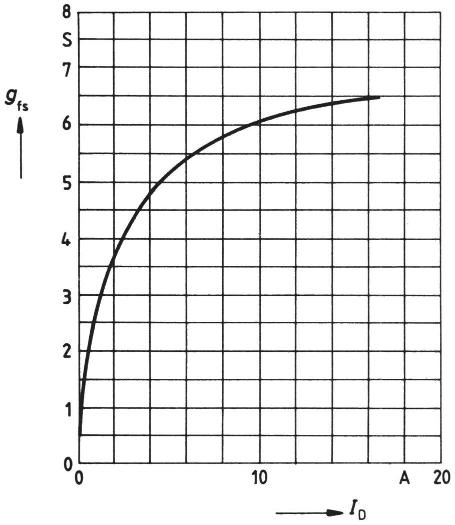


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

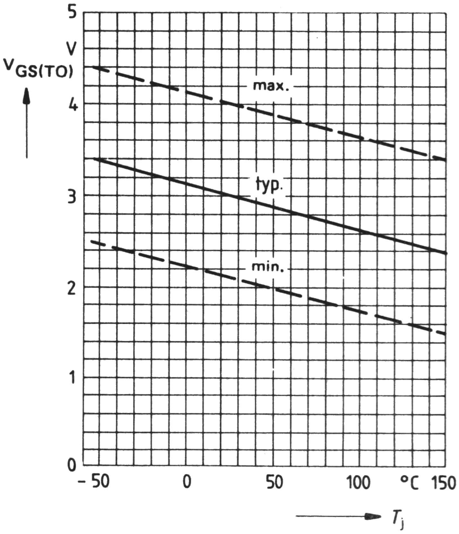


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

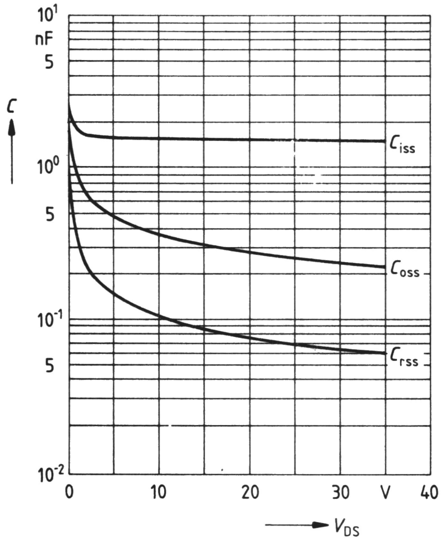


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

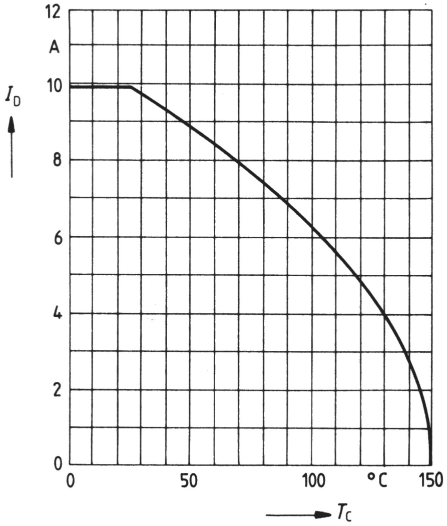


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

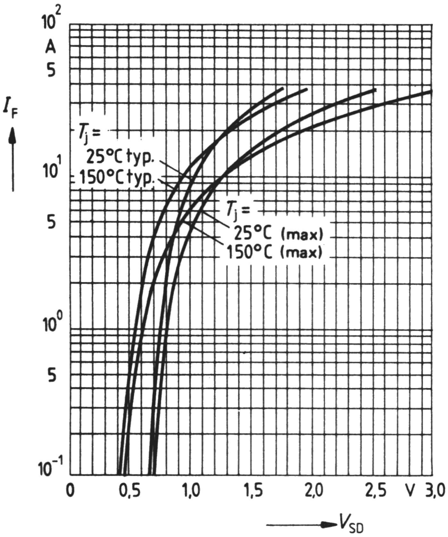


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

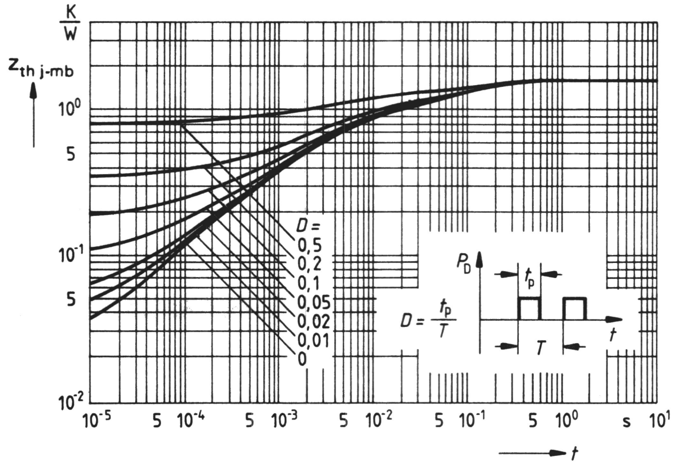


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

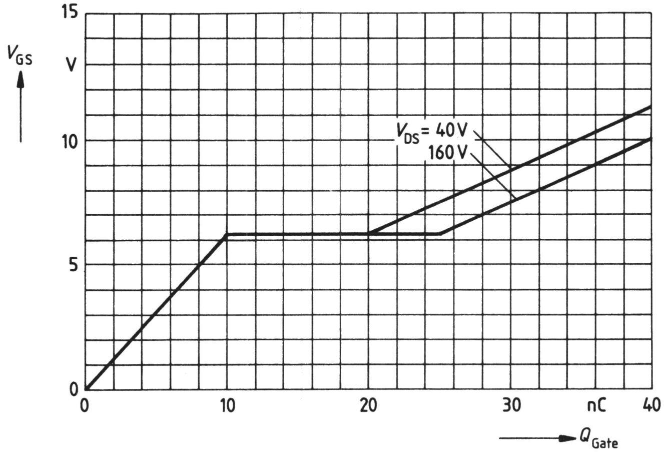


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 14,3 A.

PowerMOS transistor BUZ36

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

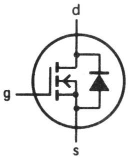
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	22	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,12	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



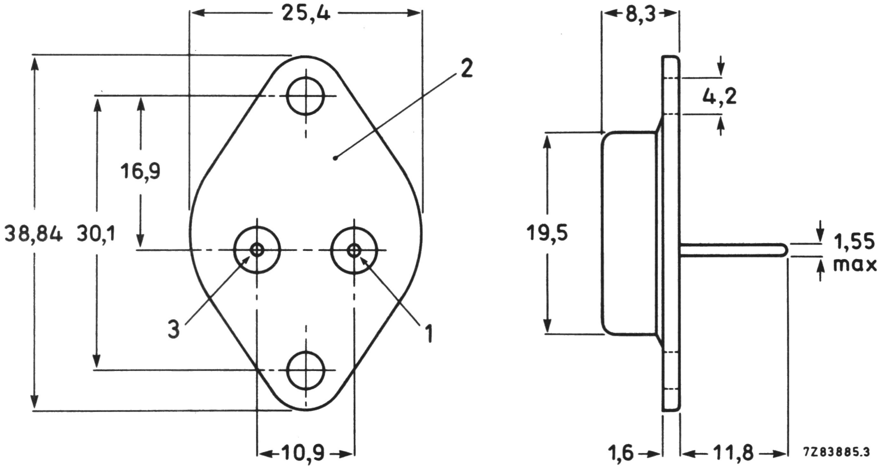


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\ k\Omega$	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 35\,°C$	–	22	A
I_D	Drain current (d.c.)	$T_{mb} = 100\,°C$	–	14,5	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\,°C$	–	85	A
P_{tot}	Total power disspation	$T_{mb} = 25\,°C$	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mouting base	$R_{th\ j\text{-}mb} = 1{,}0$ K/W
From junction to ambient	$R_{th\ j\text{-}a} = 35$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25\,°C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0$ V; $I_D = 0{,}25$ mA	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1$ mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 25\,°C$	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200$ V; $V_{GS} = 0$ V; $T_j = 125\,°C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20$ V; $V_{DS} = 0$ V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 11$ A	–	0,09	0,12	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\,°C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25$ V; $I_D = 11$ A	9,0	13,0	–	S
C_{iss}	Input capacitance	$V_{GS} = 0$ V; $V_{DS} = 25$ V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	500	800	pF
C_{rss}	Feedback capacitance		–	200	350	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30$ V; $I_D = 3$ A; $V_{GS} = 10$ V; $R_{GS} = 50\ \Omega$; $R_{gen} = 50\ \Omega$	–	30	45	ns
t_r	Turn-on rise time		–	70	110	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	120	160	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	22	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	85	A
V_{SD}	Diode forward on-voltage	I_F = 44 A; V_{GS} = 0 V; T_j = 25 °C	–	1,2	1,7	V
t_{rr}	Reverse recovery time	I_F = 22 A; T_j = 25 °C $-dI_F/dt$ = 100 A/µs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	400	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	µC

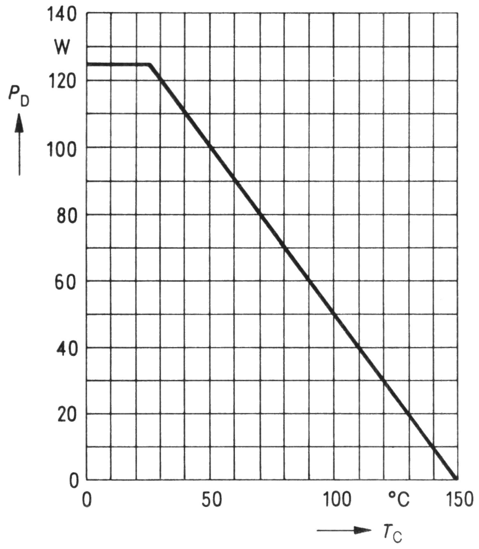


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

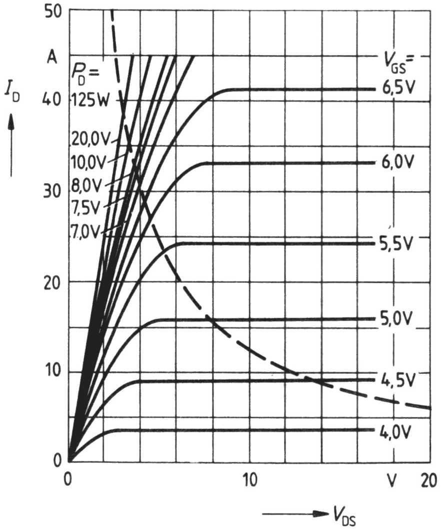


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 μs pulse test; T_{mb} = 25 °C.*

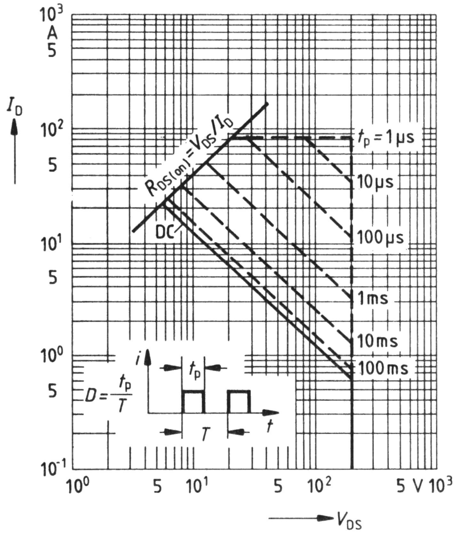


Fig.4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

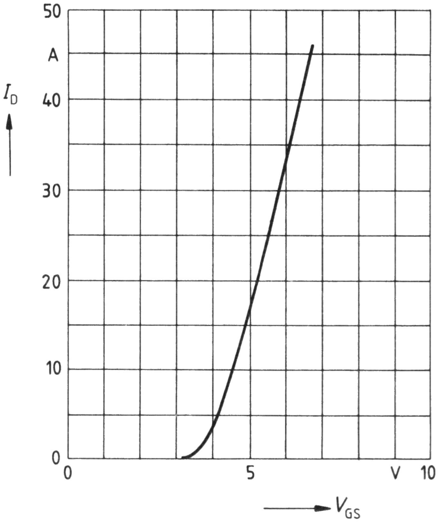


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 μs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

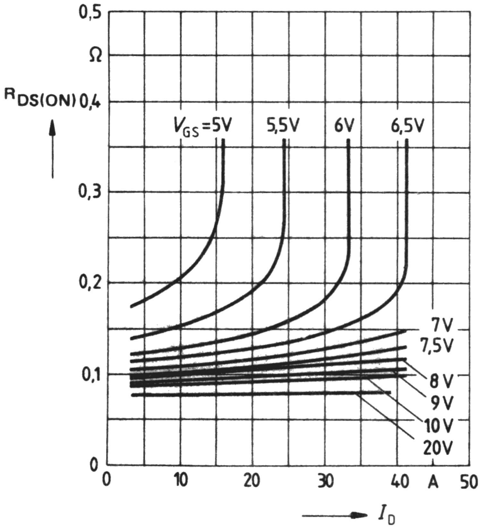


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; $T_j = 25\,°C$.

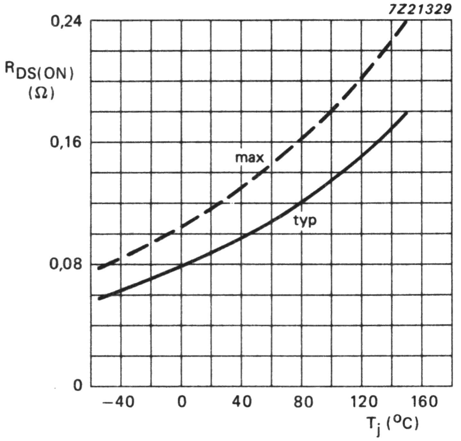


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* $I_D = 11$ A; $V_{GS} = 10$ V.

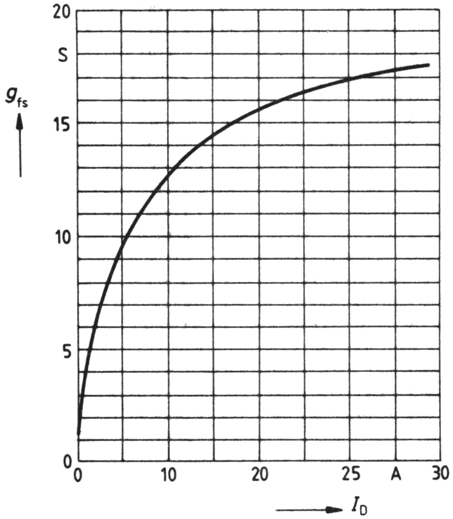


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 μs pulse test;* $V_{DS} = 25$ V; $T_j = 25\,°C$.

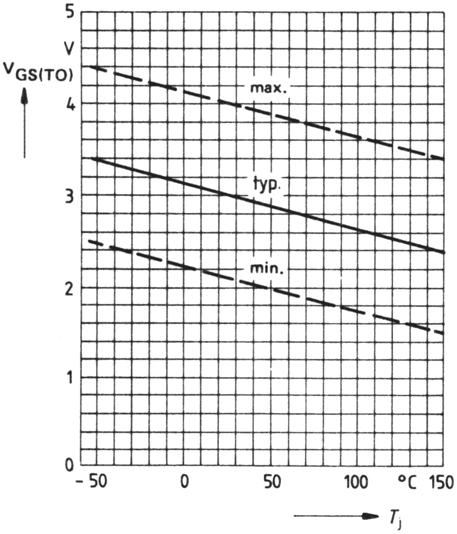


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; $I_D = 1$ mA.

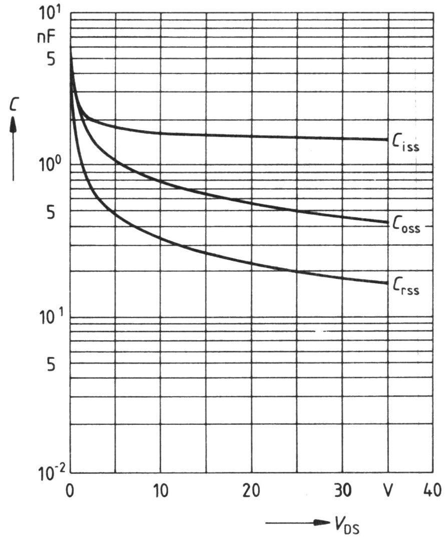


Fig.10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

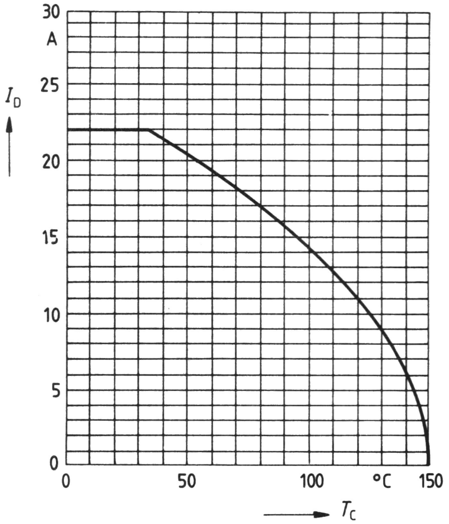


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

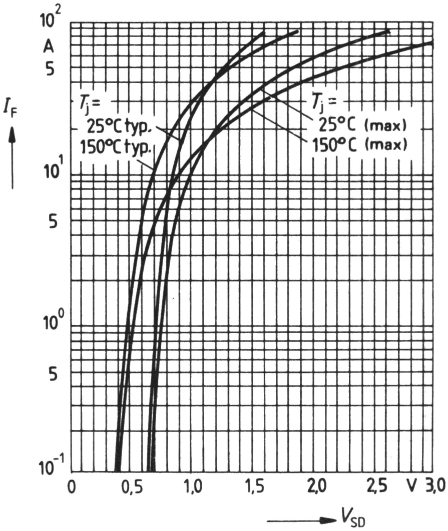


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

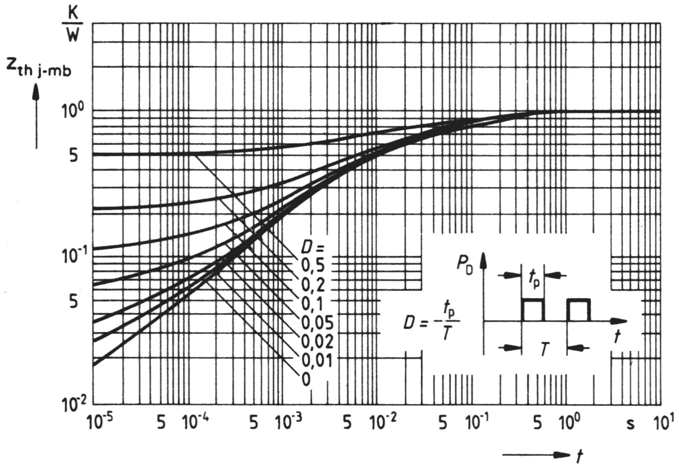


Fig.13 *Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

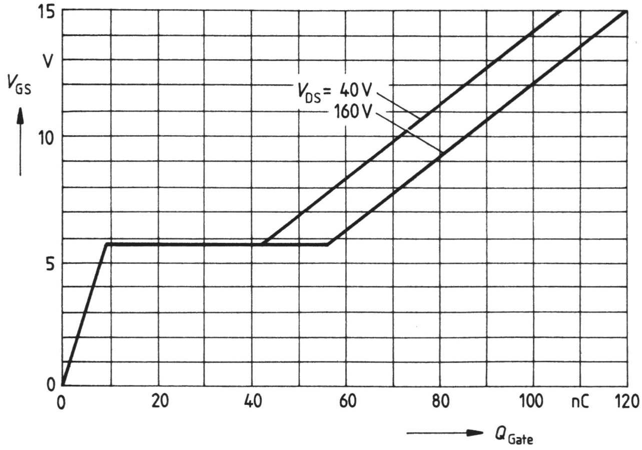


Fig.14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 33$ mA.

PowerMOS transistor BUZ63

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

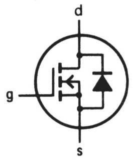
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	5,9	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



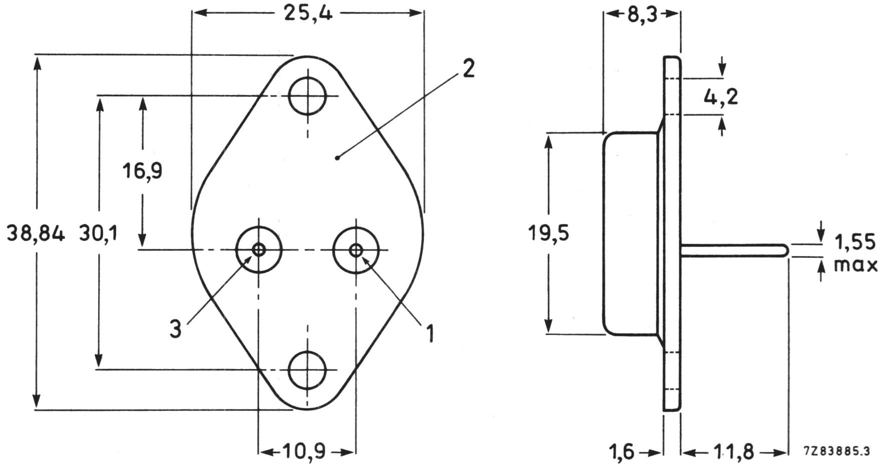


Fig. 1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	5,9	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	23	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,5 A	–	0,9	1,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,5 A	1,7	2,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	120	180	pF
C_{rss}	Feedback capacitance		–	35	60	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	50	65	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,9	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	23	A
V_{SD}	Diode forward on-voltage	I_F = 11,8 A; V_{GS} = 0 V; T_j = 25 °C	–	1,2	1,65	V
t_{rr}	Reverse recovery time	I_F = 5,9 A; T_j = 25 °C	–	1000	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/µs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	5,0	–	µC

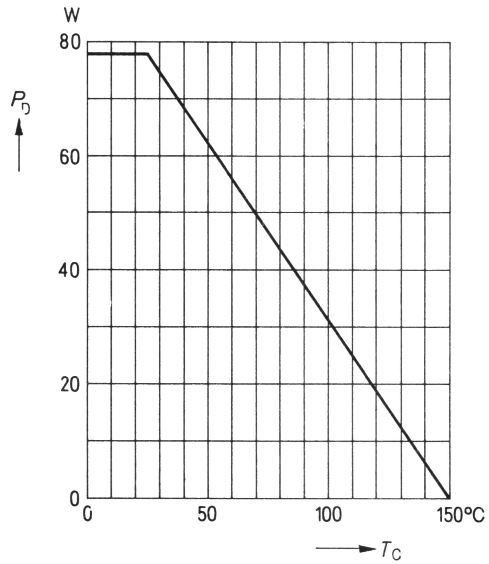


Fig. 2 Power dissipation $P_D = f(T_{mb})$.

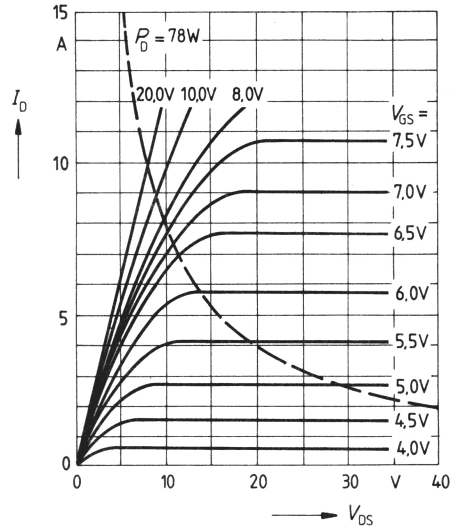


Fig. 3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25\,°C$.

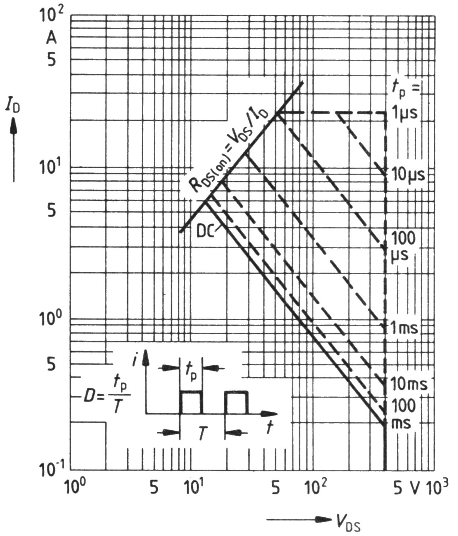


Fig. 4 Safe operating area $I_D(DC)$ and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25\,°C$.

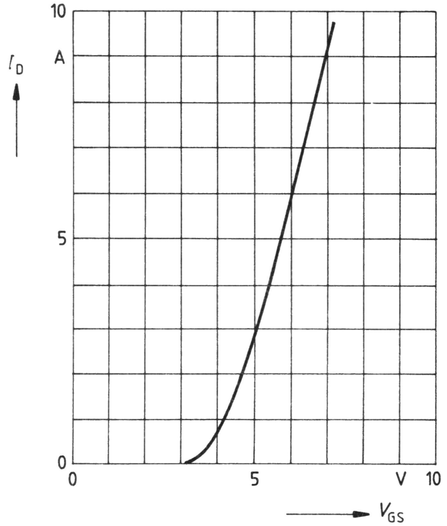


Fig. 5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25\,°C$.

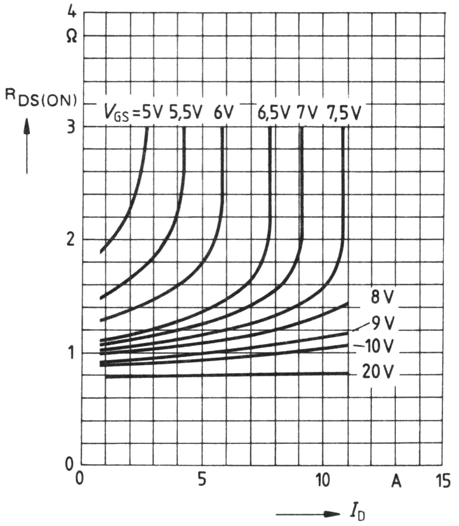


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

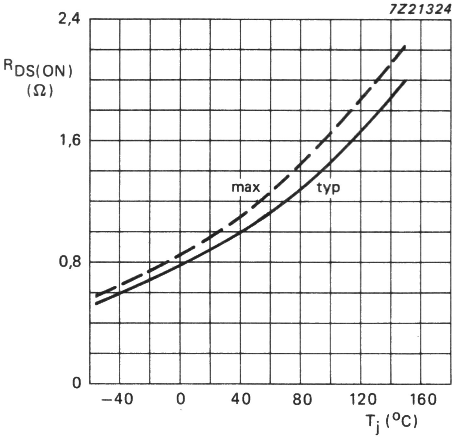


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 2{,}5\ A$; $V_{GS} = 10\ V$.

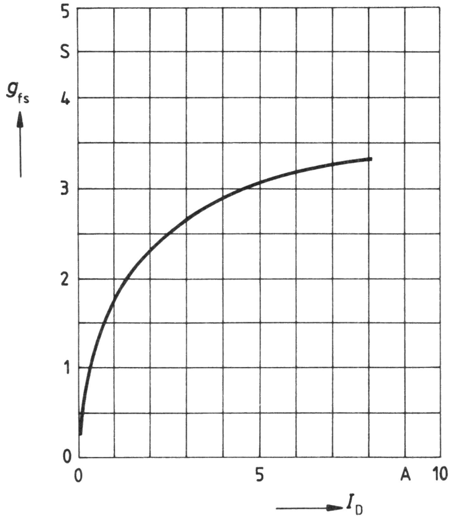


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\,°C$.

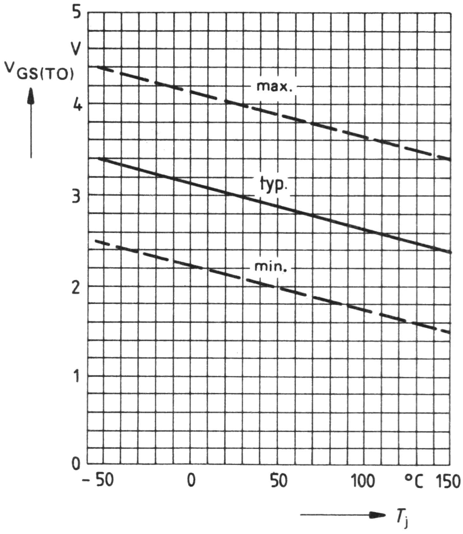


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

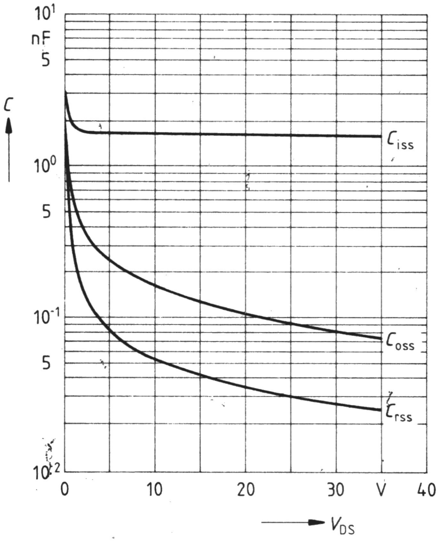


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

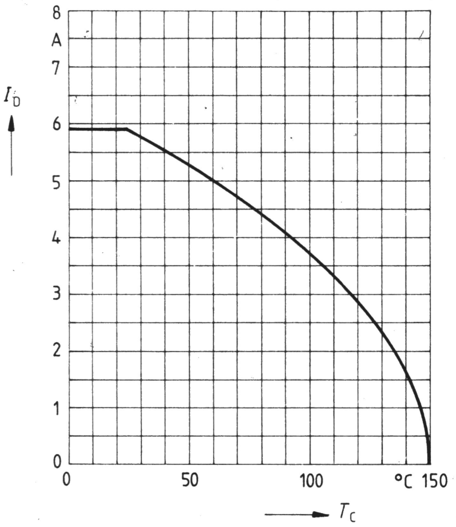


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

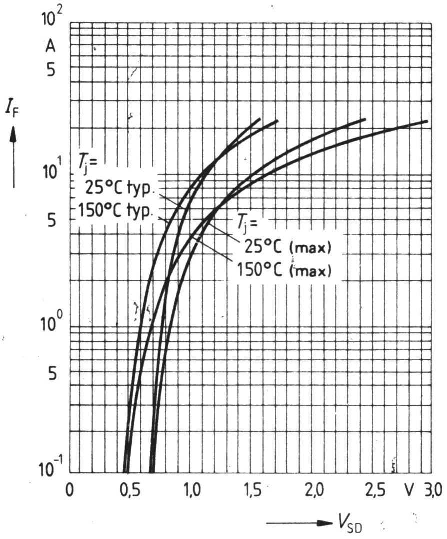


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

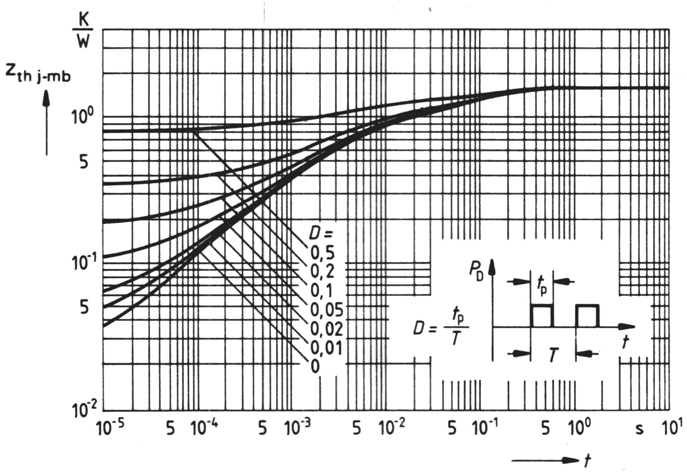


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

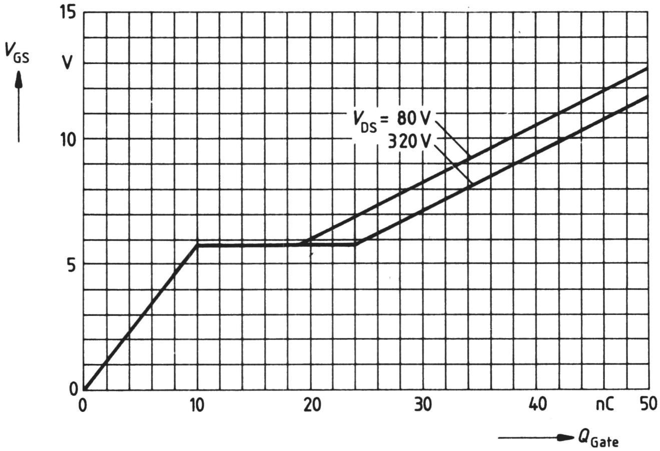


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 8{,}3$ A.

PowerMOS transistor BUZ64

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

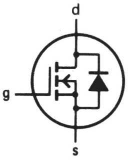
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	11,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,4	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



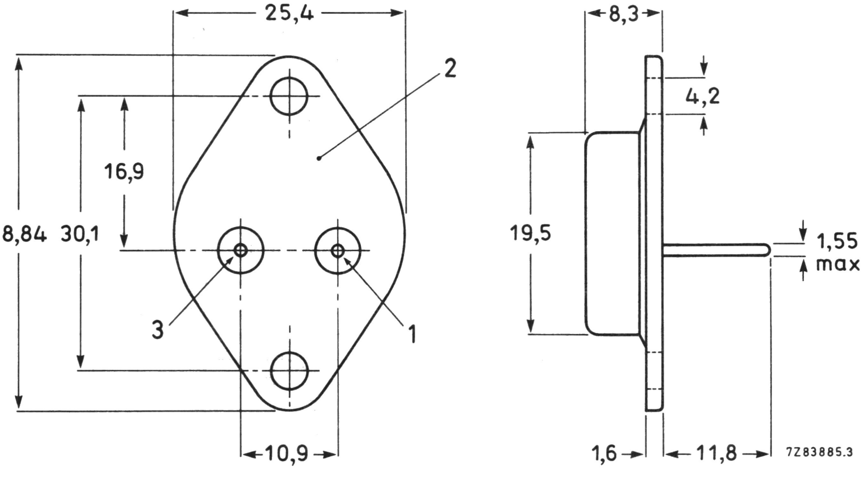


Fig. 1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	11,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	7,4	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	46	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5,5 A	–	0,35	0,40	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5,5 A	3,3	4,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	300	500	pF
C_{rss}	Feedback capacitance		–	120	200	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	11,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	46	A
V_{SD}	Diode forward on-voltage	I_F = 23 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 11,5 A; T_j = 25 °C	–	1000	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/µs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	10	–	µC

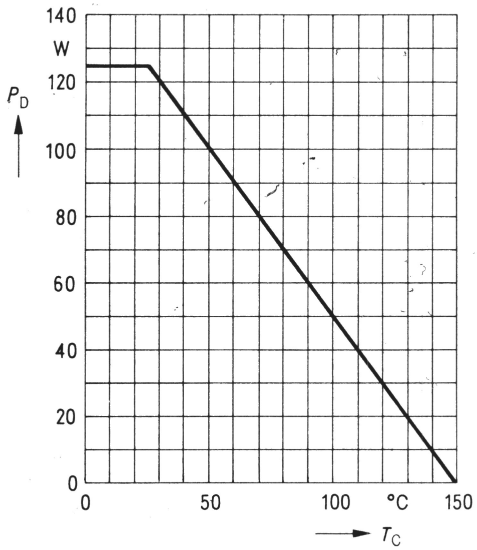


Fig.2 Power dissipation $P_D = f(T_{mb})$.

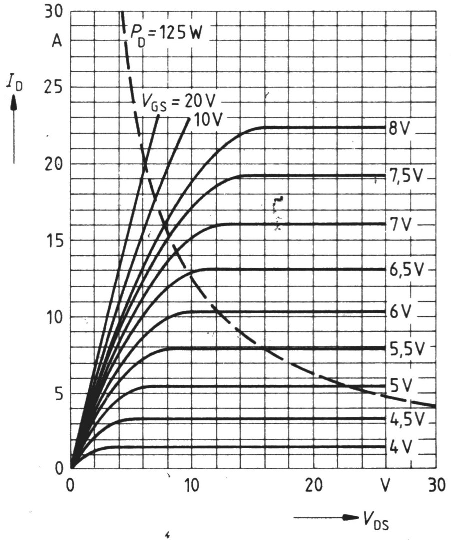


*Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25\,°C$.*

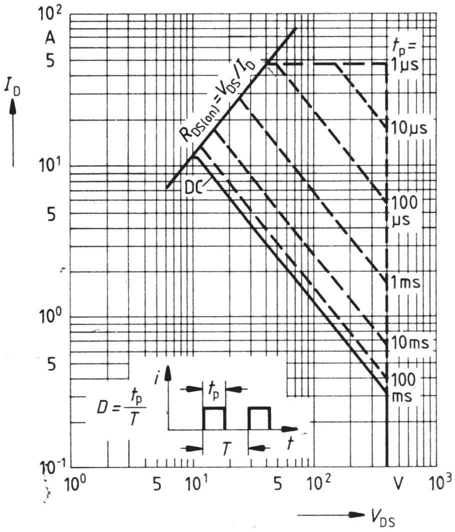


*Fig.4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; $T_{mb} = 25\,°C$.*

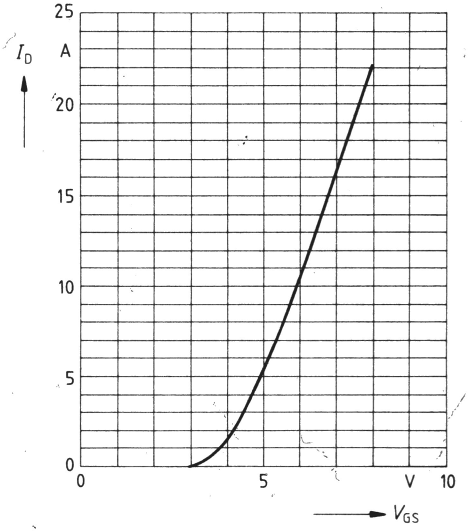


*Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25\,°C$.*

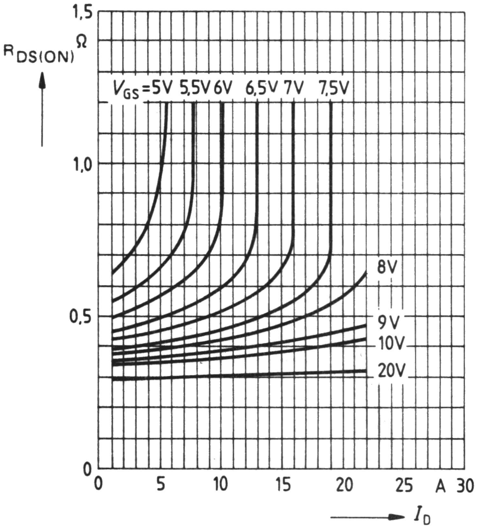


Fig.6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

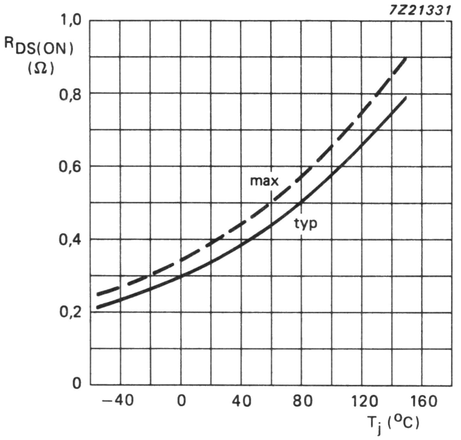


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 5{,}5\ A$; $V_{GS} = 10\ V$.

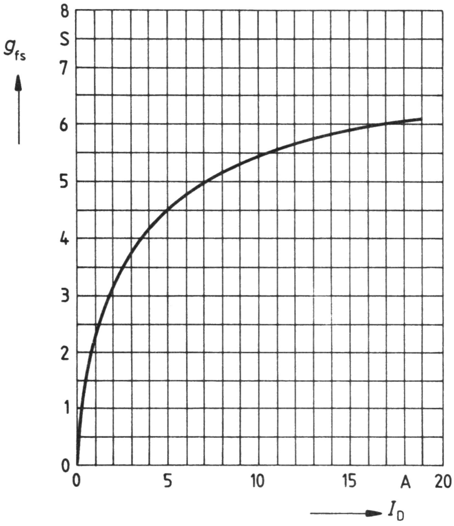


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\,°C$.

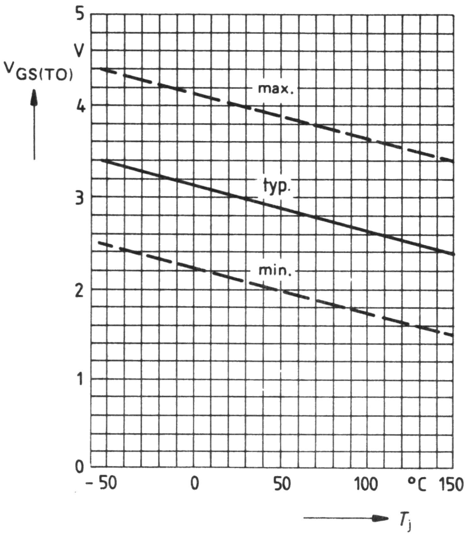


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

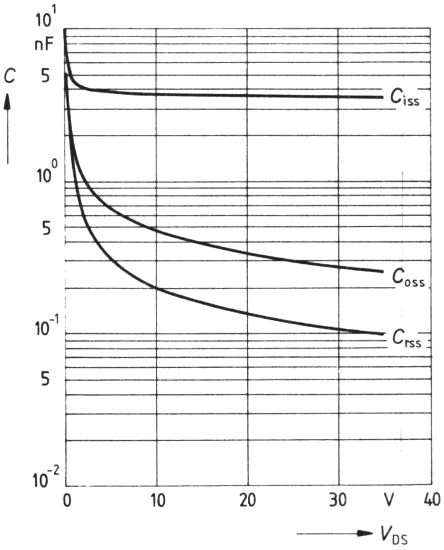


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

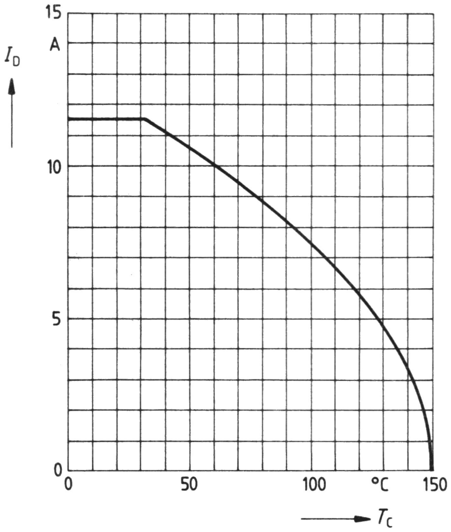


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geq 10$ V.

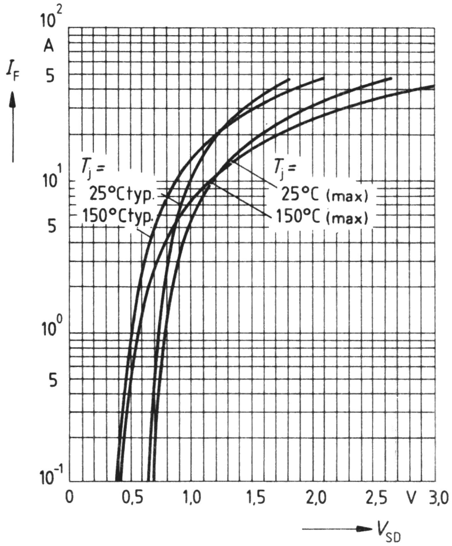


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

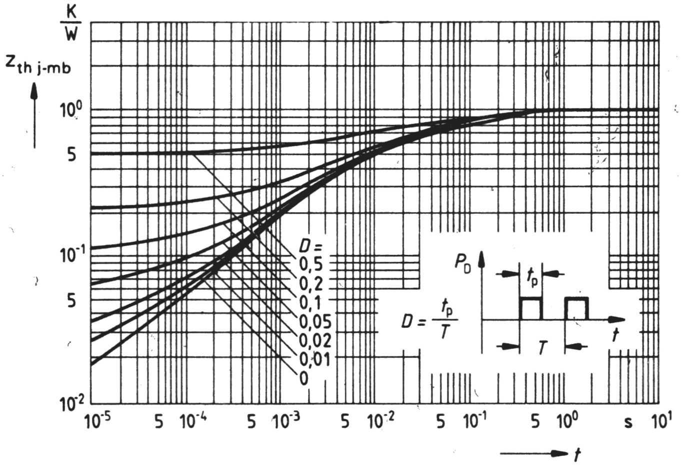


*Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.*

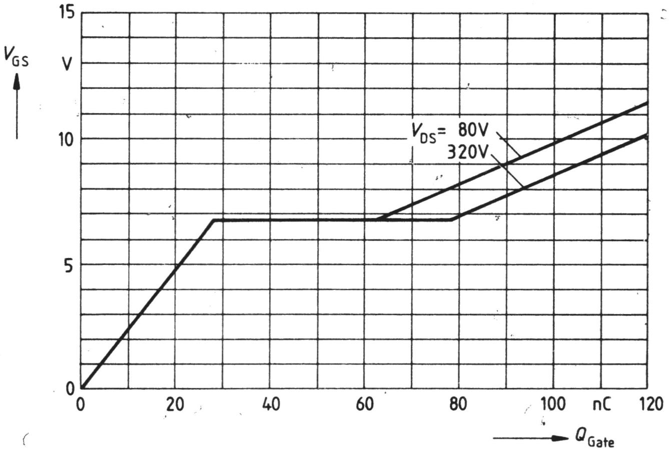


*Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 17{,}3$ A.*

PowerMOS transistor

BUZ45

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

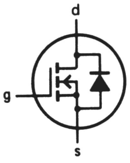
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	9,6	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,6	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



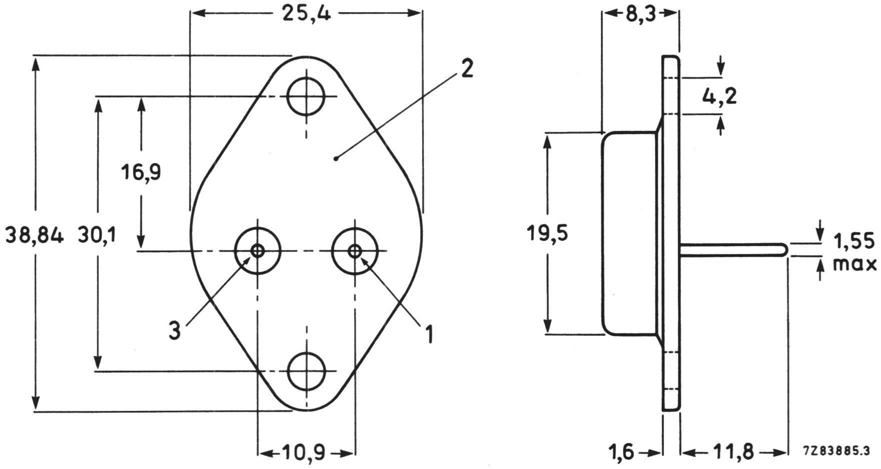


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	9,6	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	38	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,55	0,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	5,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	9,6	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	38	A
V_{SD}	Diode forward on-voltage	I_F = 19,2 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 9,6 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	1200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 100 V	–	12	–	μC

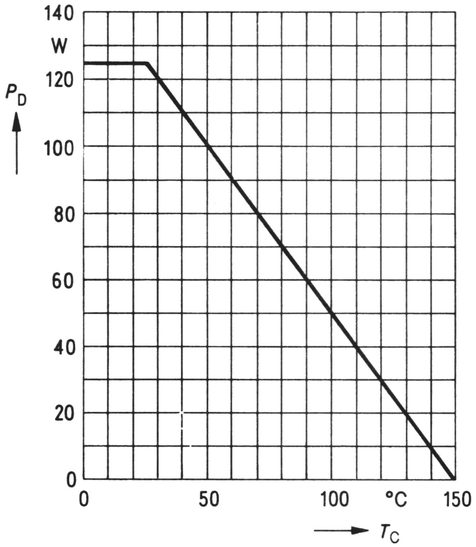


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

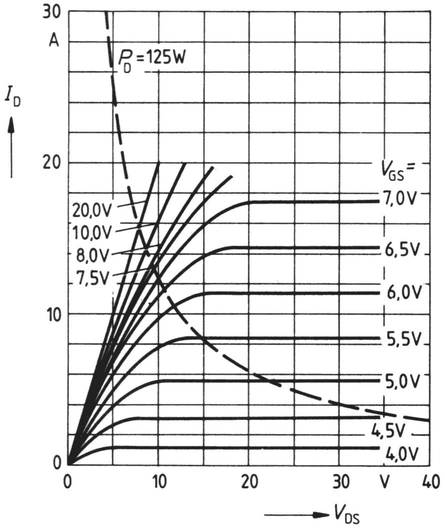


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 µs pulse test; T_{mb} = 25 °C.*

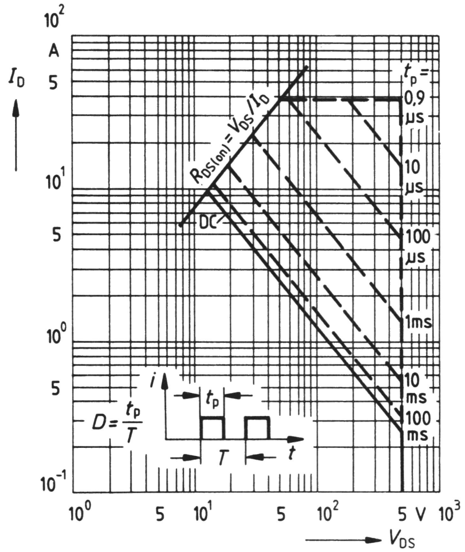


Fig.4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

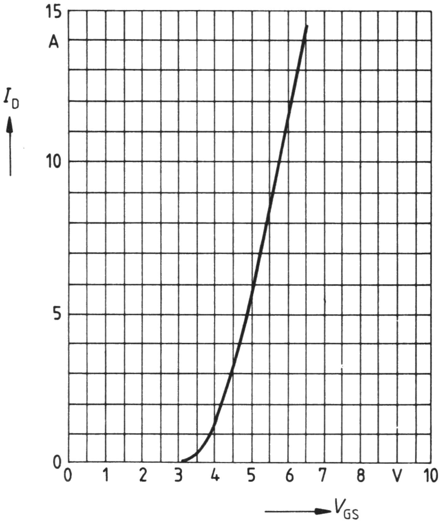


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 µs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

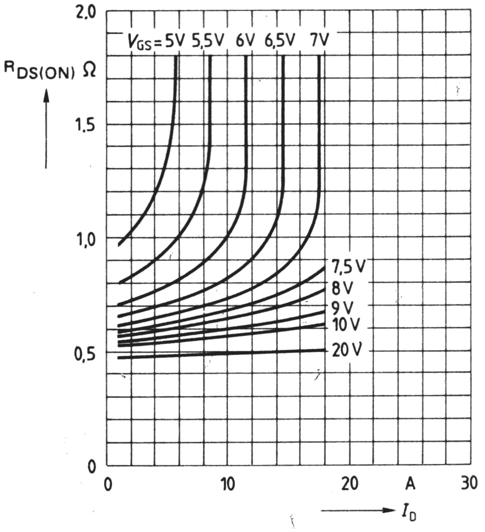


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\ °C$.

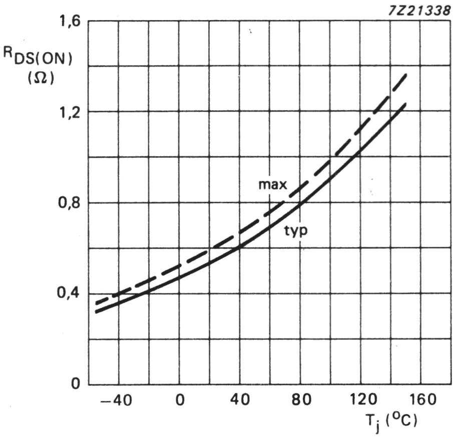


Fig.7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 5\ A$; $V_{GS} = 10\ V$.

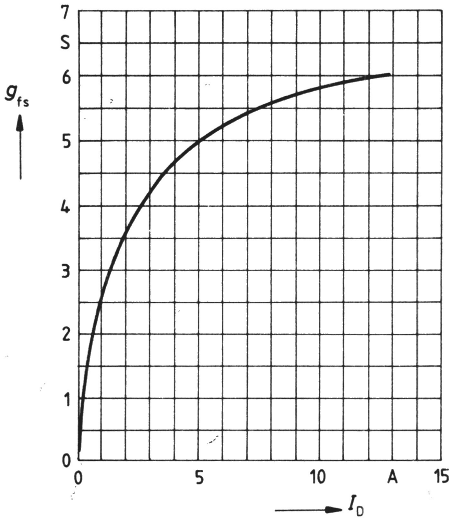


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\ °C$.

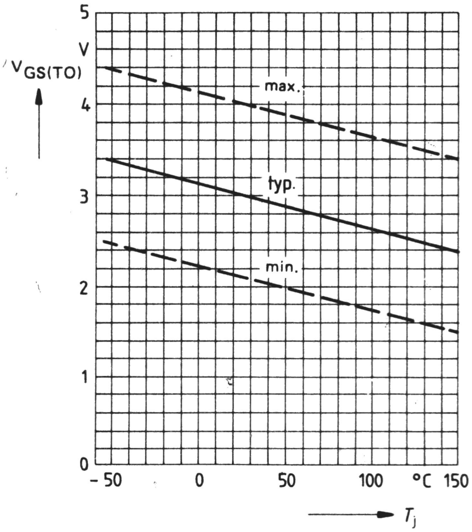


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

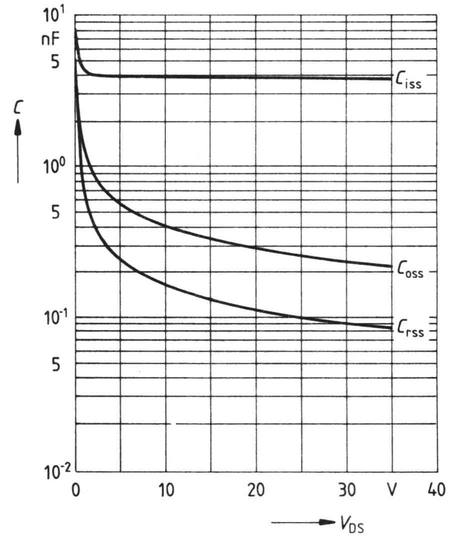


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

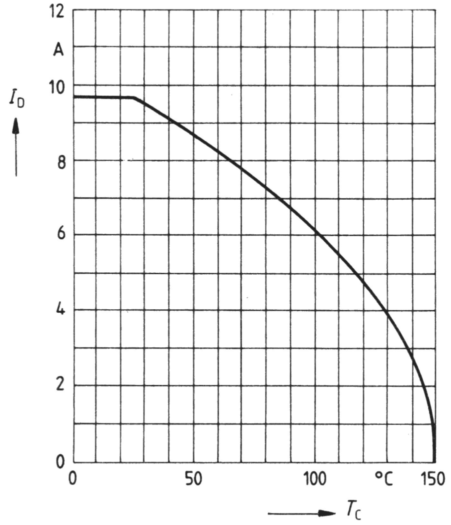


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

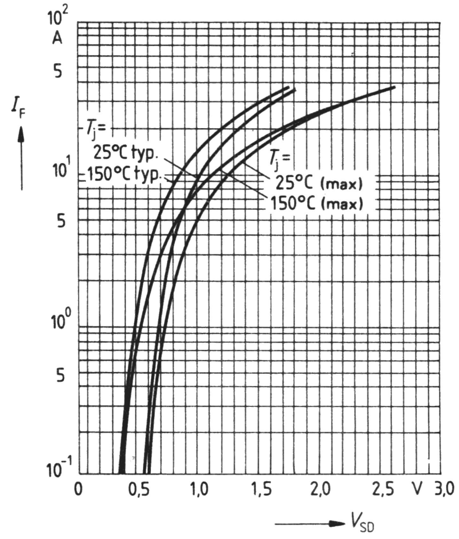


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80\ \mu s$.

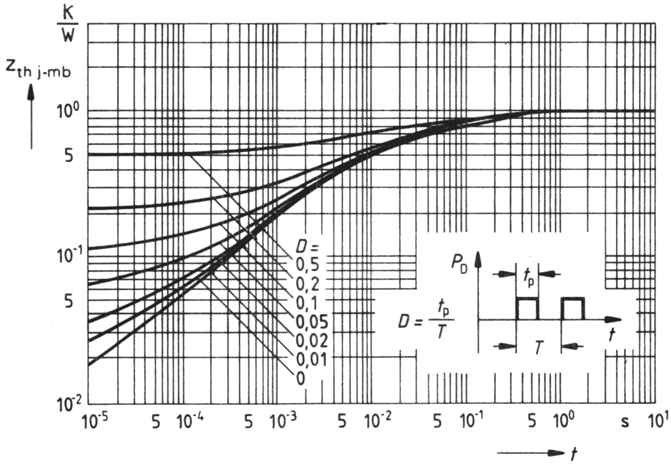


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

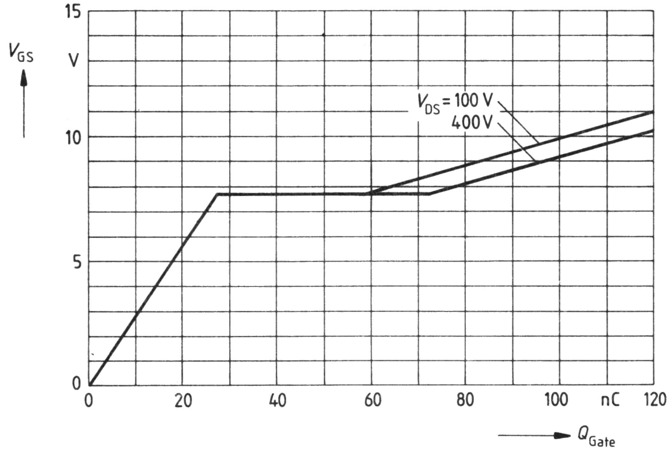


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 14{,}4$ A.

PowerMOS transistor BUZ45A

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

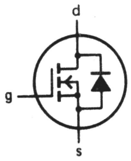
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	8,3	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,8	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



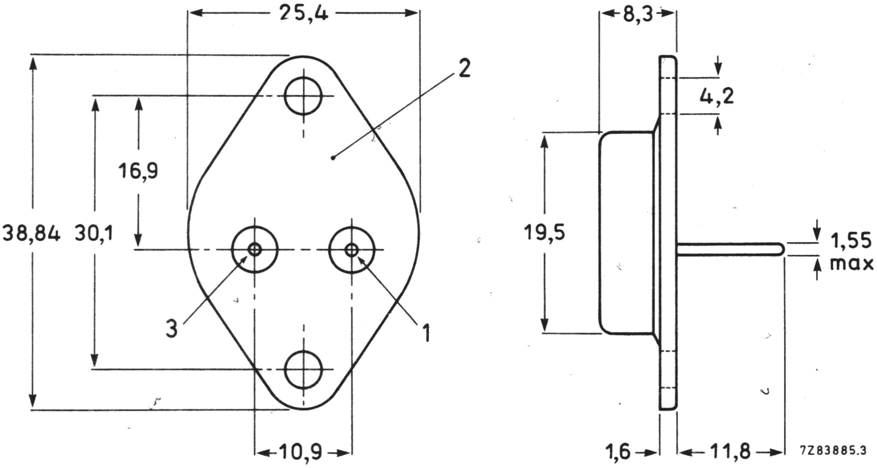


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	8,3	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	5,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	33	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,7	0,8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	5,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A ; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	8,3	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	33	A
V_{SD}	Diode forward on-voltage	I_F = 19,2 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,6	V
t_{rr}	Reverse recovery time	I_F = 9,6 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	1200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 100 V	–	12	–	μC

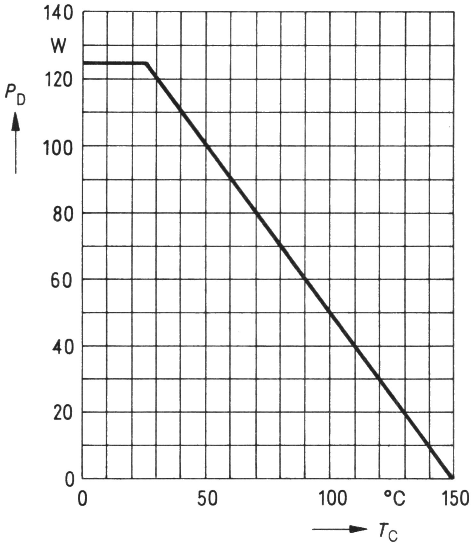


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

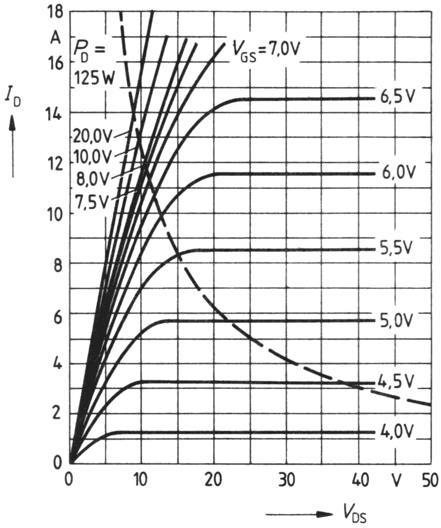


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

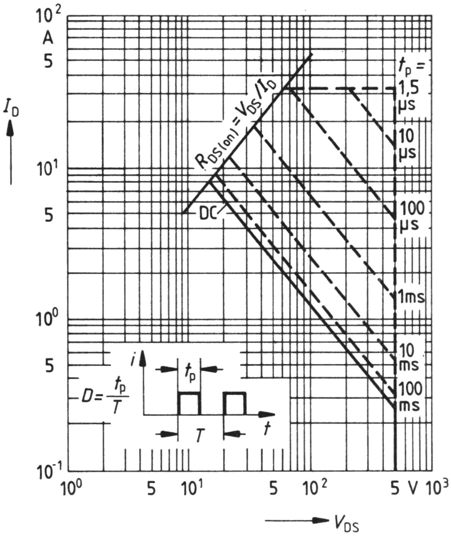


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

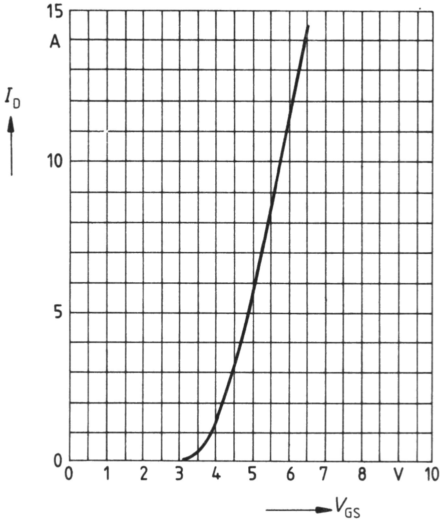


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

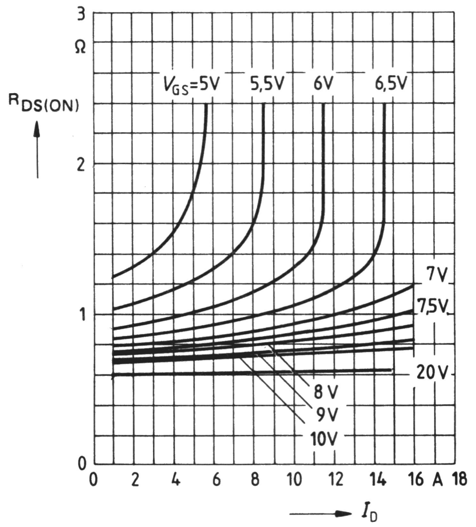


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}*;* $T_j = 25\,°C$.

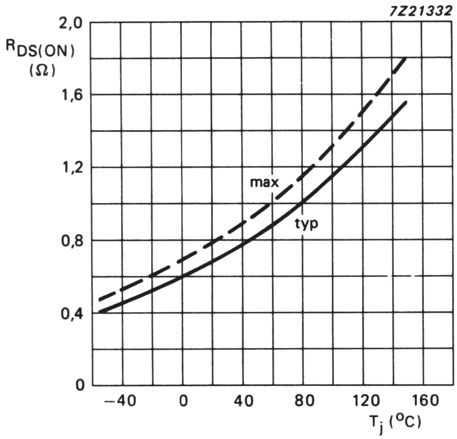


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 5\,A$; $V_{GS} = 10\,V$.

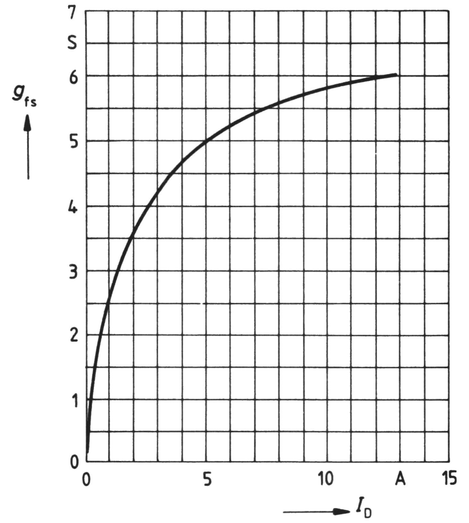


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\,V$; $T_j = 25\,°C$.

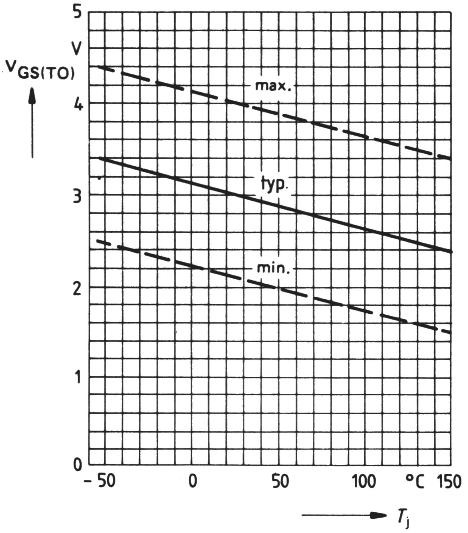


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

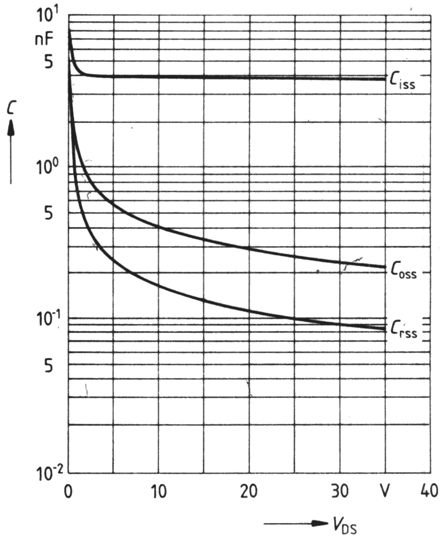


Fig.10 *Typical capacitances* $C = f(V_{DS})$.
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

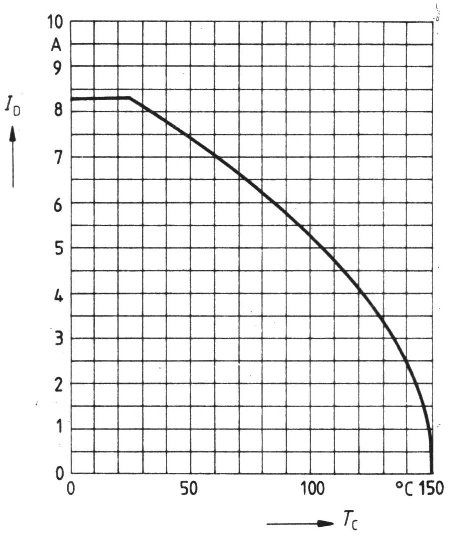


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geq 10$ *V.*

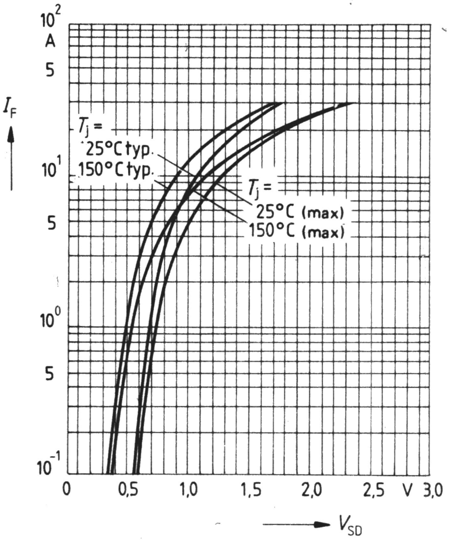


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

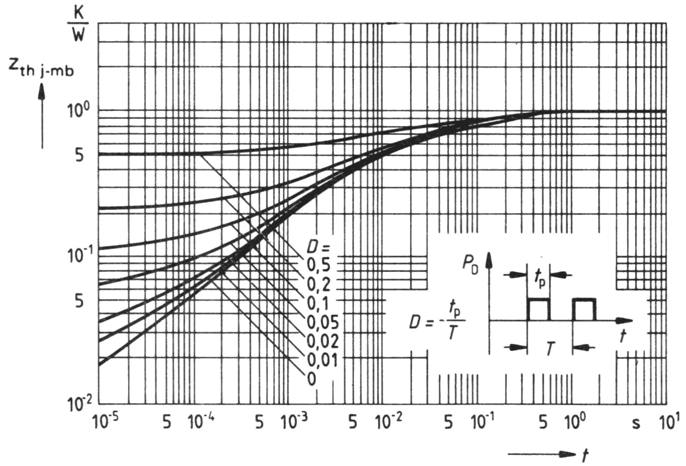


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

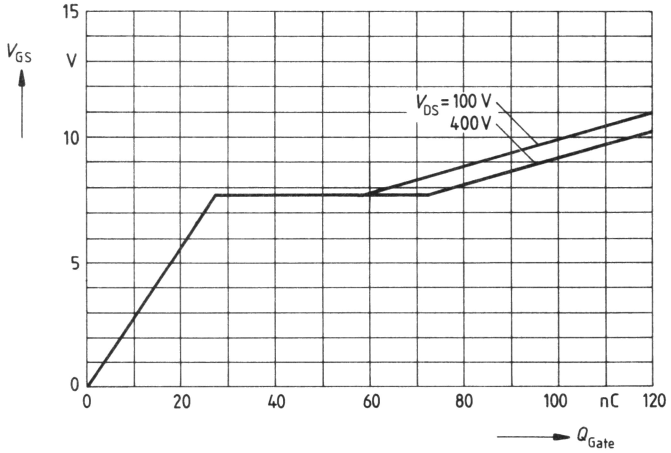


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 14,4 A.

PowerMOS transistor

BUZ45B

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

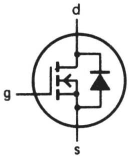
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	10	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



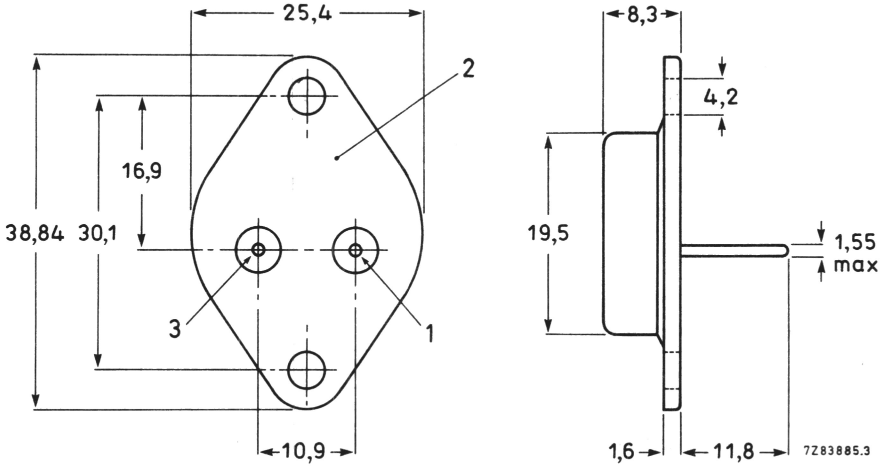


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	10	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,6	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	40	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,49	0,50	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	5,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	10	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	40	A
V_{SD}	Diode forward on-voltage	I_F = 20 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 10 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V;	–	1200	–	ns
Q_{rr}	Reverse recovery charge	V_R = 100 V	–	12	–	μC

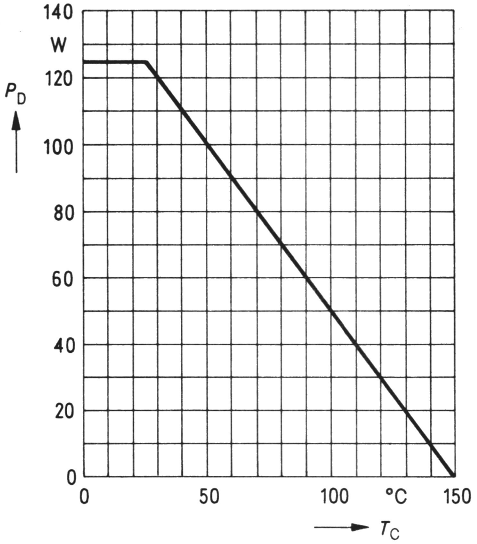


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

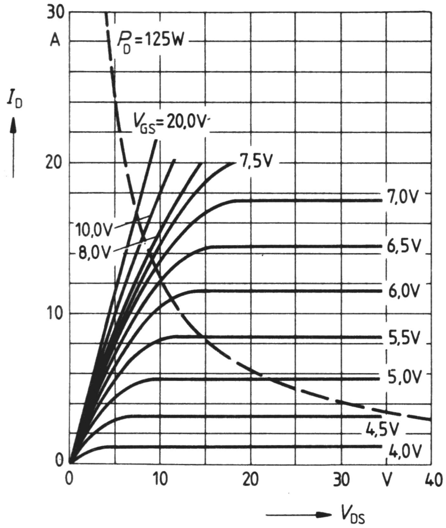


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$ *Parameter:* V_{GS}; *80 µs pulse test;* T_{mb} = *25 °C.*

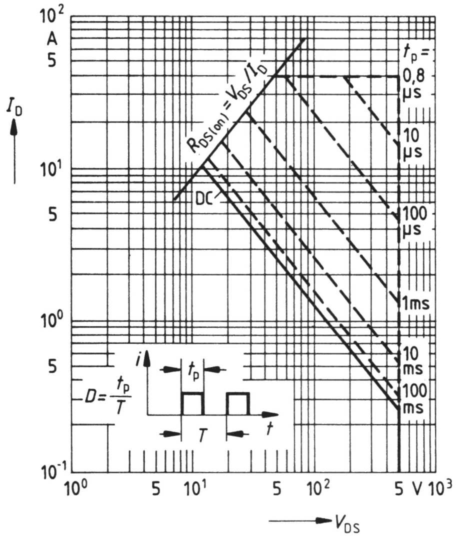


Fig.4 *Safe operating area* $I_D(DC)$ *and* $I_{DM} = f(V_{DS})$ *Parameter:* t_p; *D = 0,01;* T_{mb} = *25 °C.*

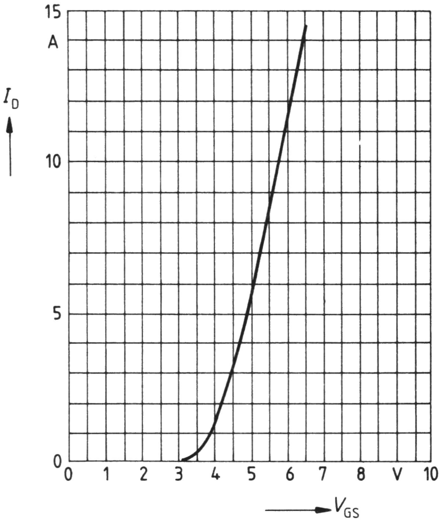


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$ *Conditions: 80 µs pulse test;* V_{DS} = *25 V,* T_{mb} = *25 °C.*

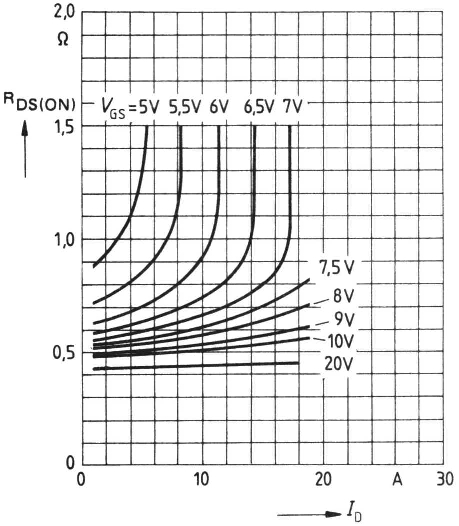


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$*
Parameter: V_{GS}; T_j = 25 °C.

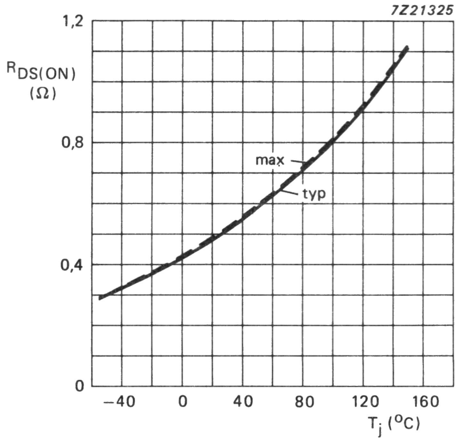


Fig. 7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$*
Conditions: I_D = 5 A; V_{GS} = 10 V.

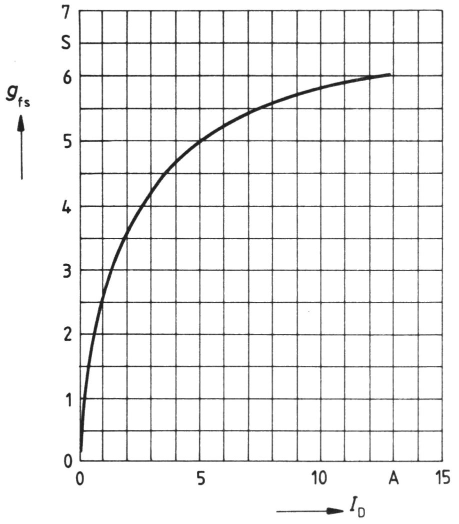


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

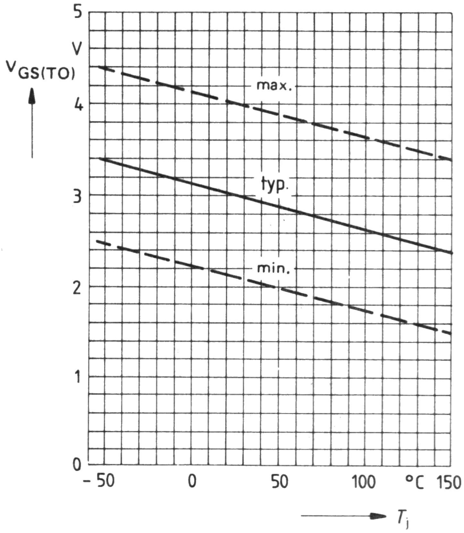


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

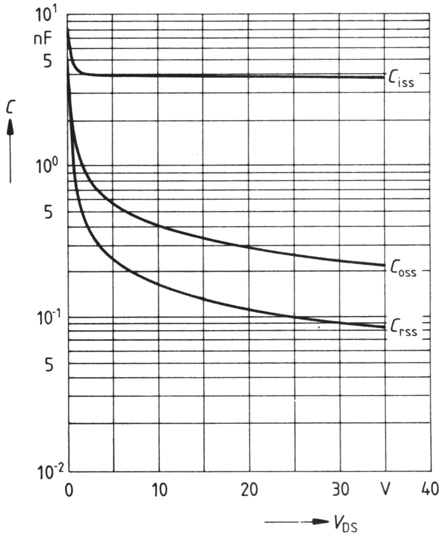


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

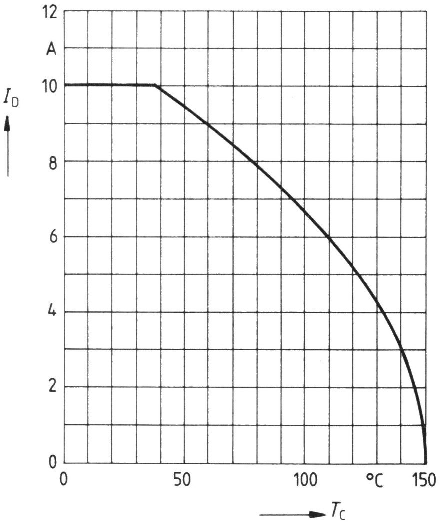


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

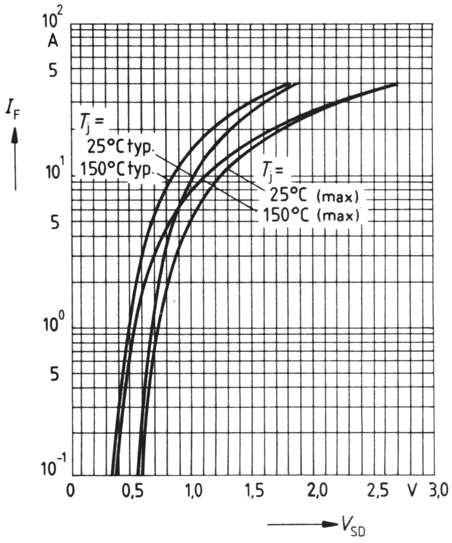


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

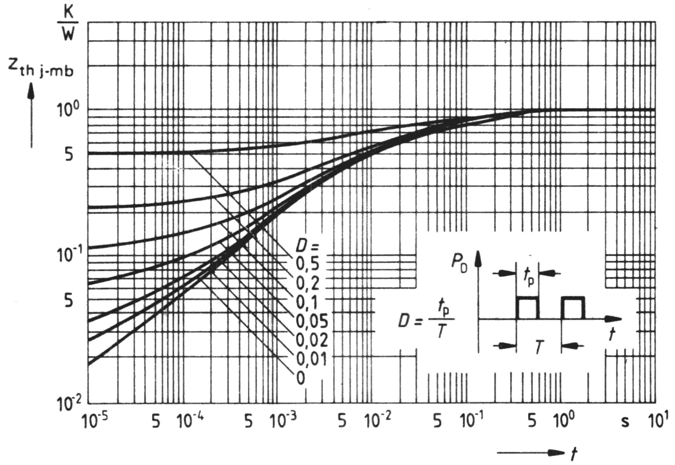


Fig.13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

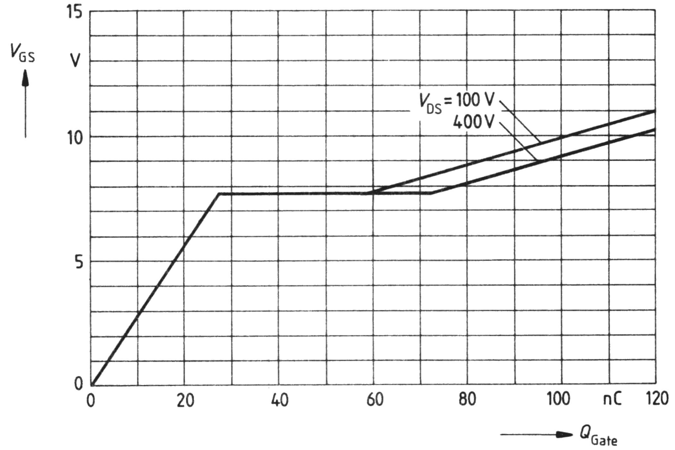


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 14{,}4$ A.

PowerMOS transistor

BUZ211

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

FREDFET* with fast-recovery reverse diode.

This device is particularly suitable for motor control applications, eg. in full-bridge configurations for which faster recovery characteristics simplify design for inductive loads.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	9,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,8	Ω

* Fast Recovery Epitaxial Diode FET.

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source

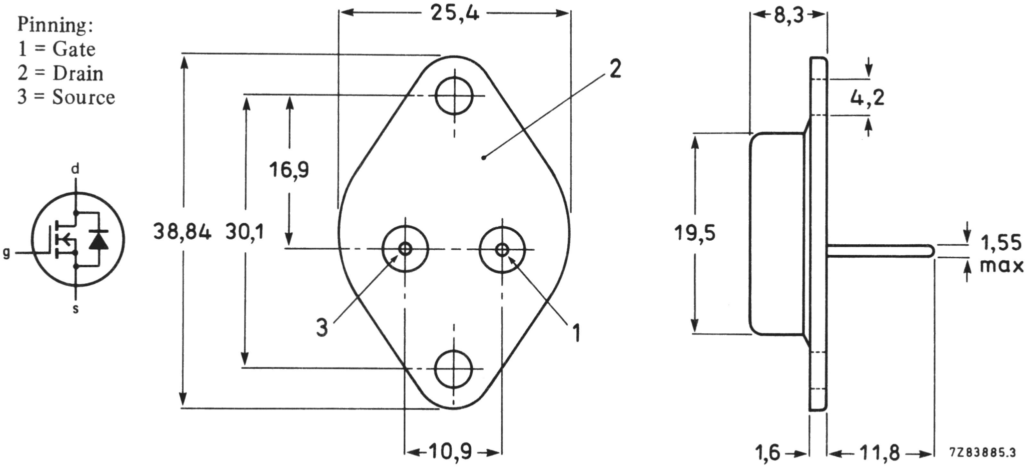


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	9,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	5,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\,j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\,j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6,5 V	–	0,7	0,8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6,5 A	2,7	5,3	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\,off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	9,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	36	A
V_{SD}	Diode forward on-voltage	I_F = 18 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,6	V
t_{rr}	Reverse recovery time	I_F = 9,0 A; T_j = 25 °C	–	180	250	ns
		$-dI_F/dt$ = T_j = 150 °C	–	220	300	ns
Q_{rr}	Reverse recovery charge	100 A/μs; T_j = 25 °C	–	0,65	1,2	μC
		V_{GS} = 0 V; T_j = 150 °C	–	2,6	5,0	μC
I_{rrm}	Reverse recovery current	V_R = 100 V T_j = 150 °C	–	15	–	A

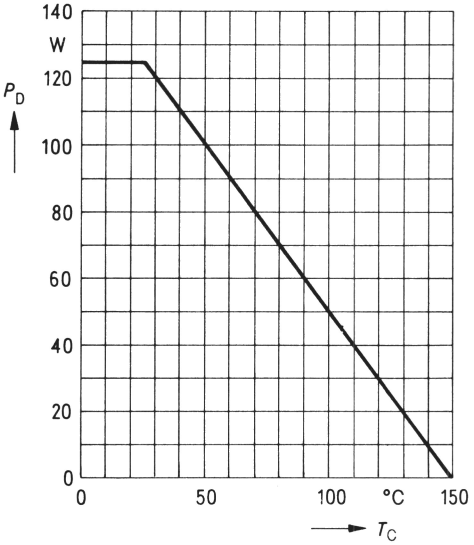


Fig.2 Power dissipation $P_D = f(T_{mb})$.

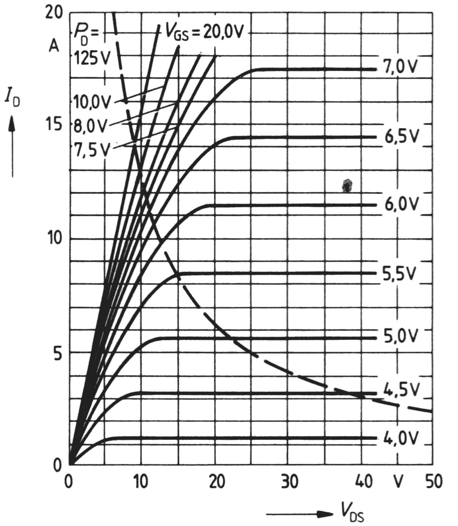


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 μs pulse test;
$T_{mb} = 25°C$.

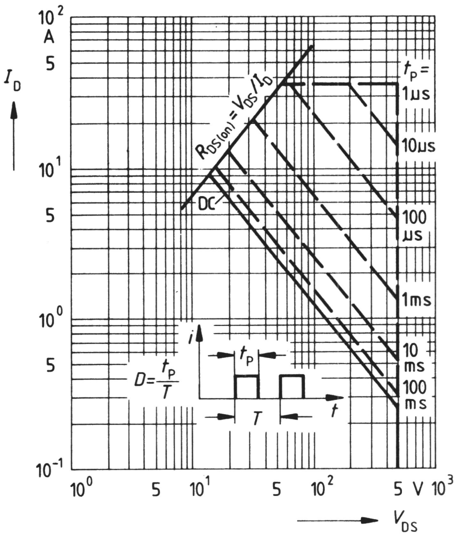


Fig.4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25°C$.

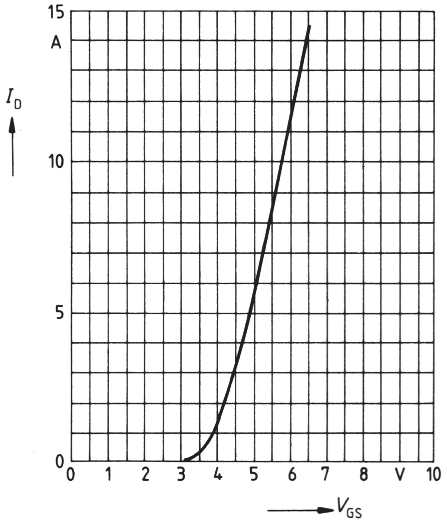


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 μs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25°C$.

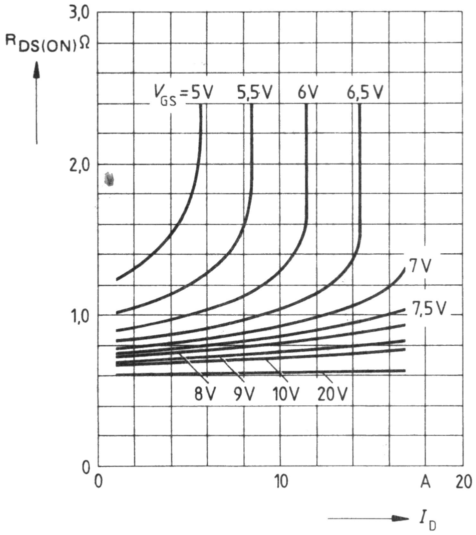


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

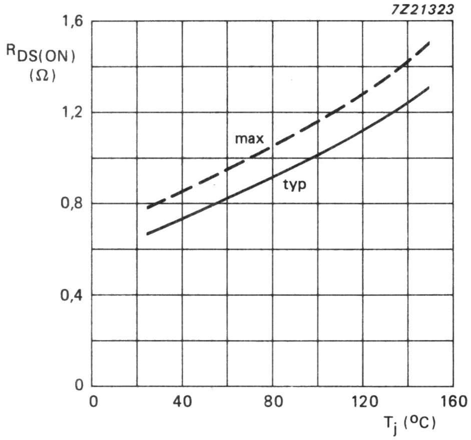


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 6{,}5$ A; $V_{GS} = 10$ V.

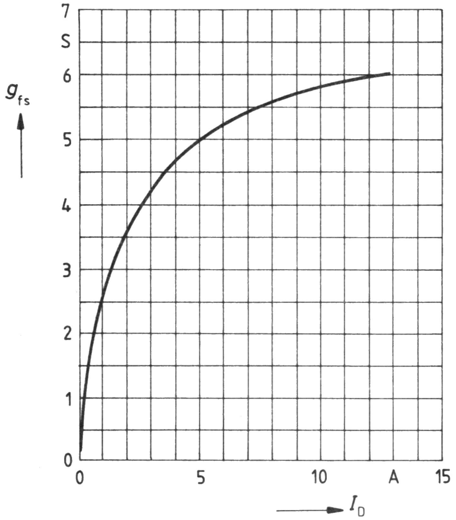


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

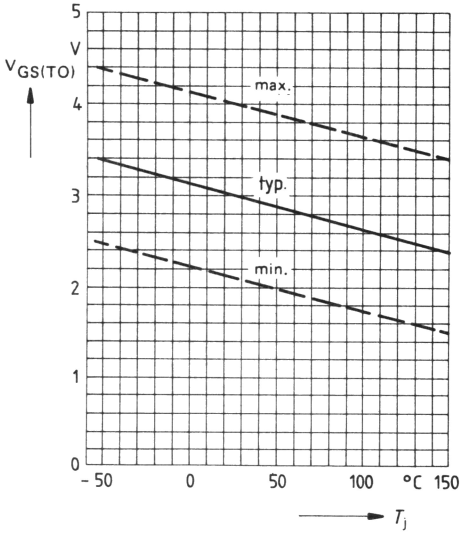


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

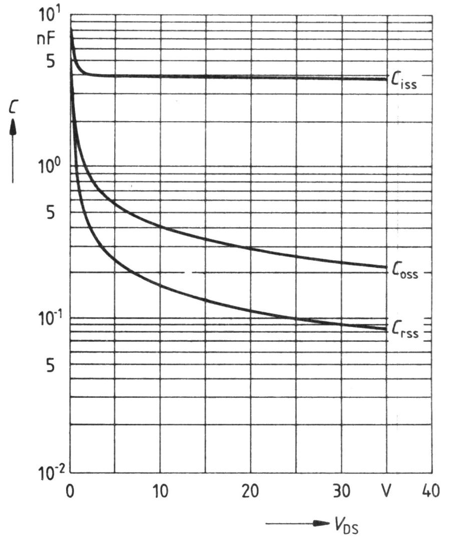


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

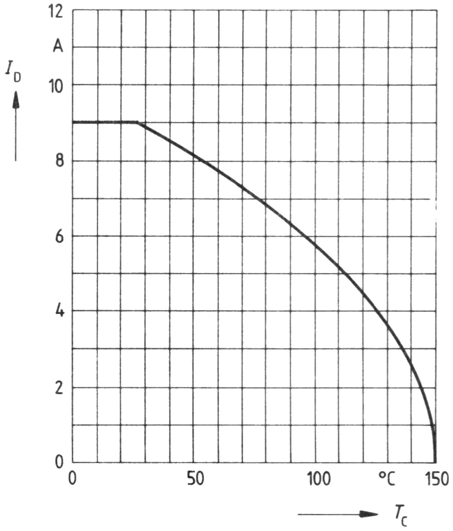


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

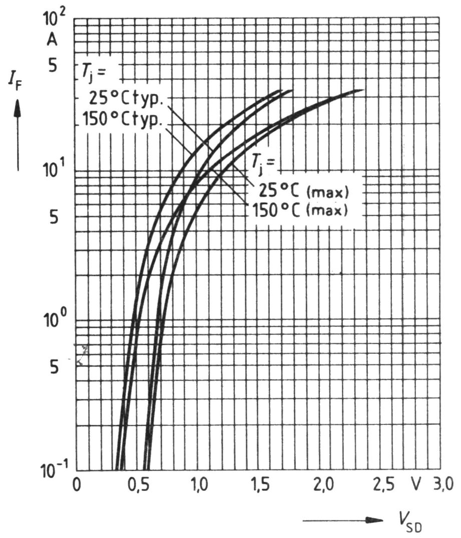


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

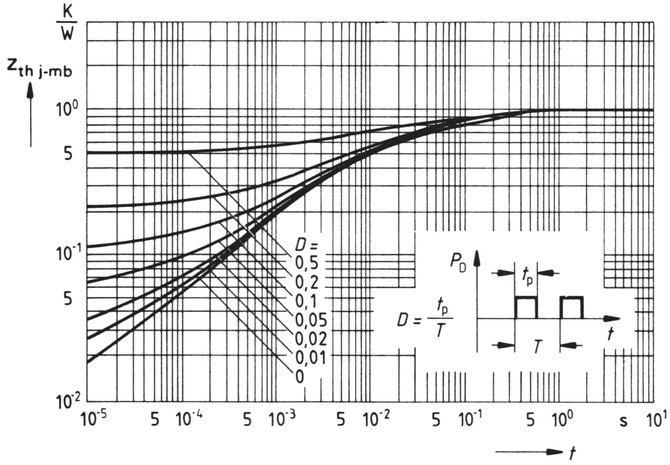


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

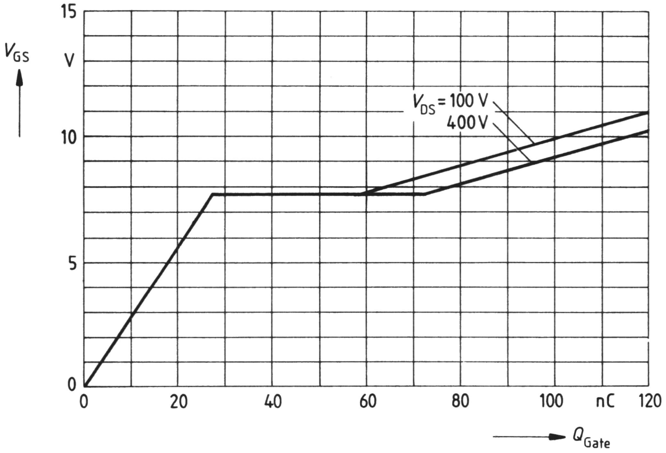


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 14{,}4$ A.

PowerMOS transistor BUZ94

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

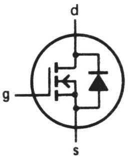
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	600	V
I_D	Drain current (d.c.)	7,8	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,9	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



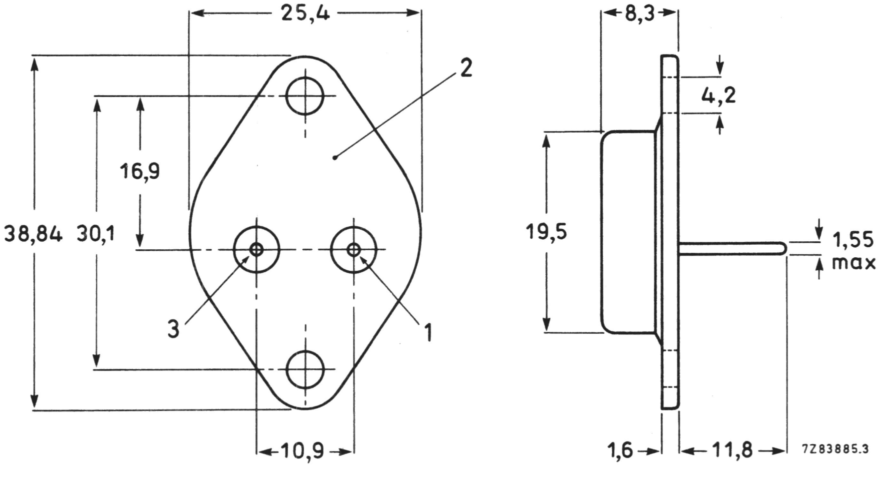


Fig. 1 *TO3; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	600	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	600	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	7,8	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	4,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	31	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	600	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 600 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5 A	–	0,8	0,9	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5 A	2,7	4,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	7,8	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	31	A
V_{SD}	Diode forward on-voltage	I_F = 15,6 A; V_{GS} = 0 V; T_j = 25 °C	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 7,8 A; T_j = 25 °C	–	1,2	–	µs
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/µs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	12	–	µC

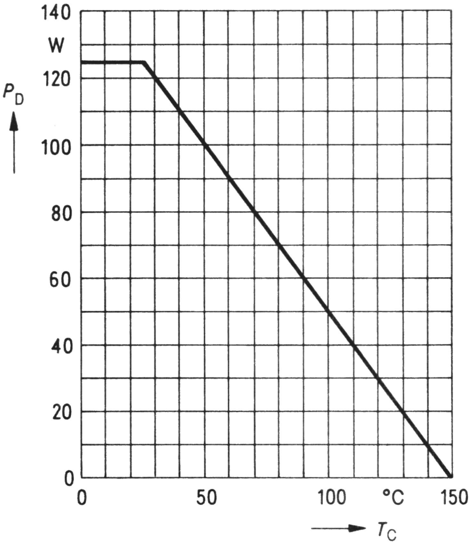


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

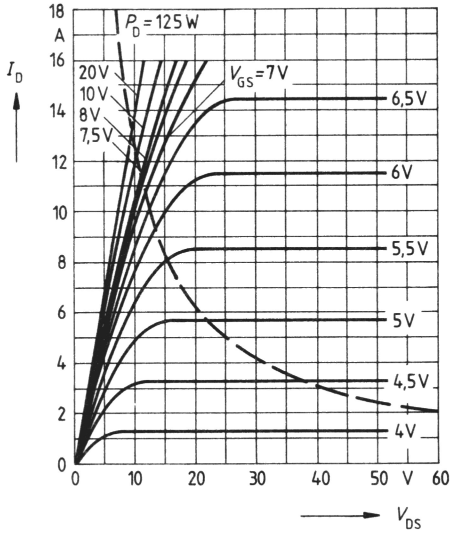


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

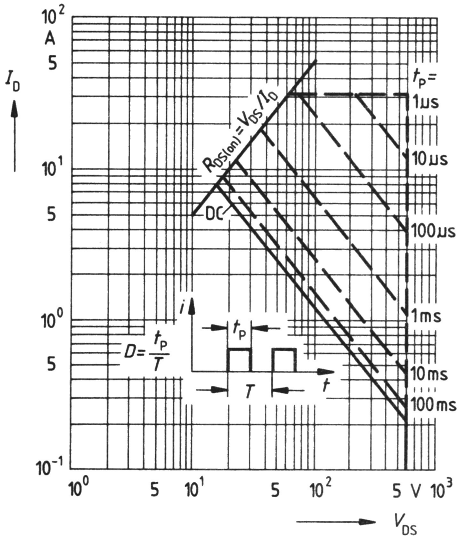


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

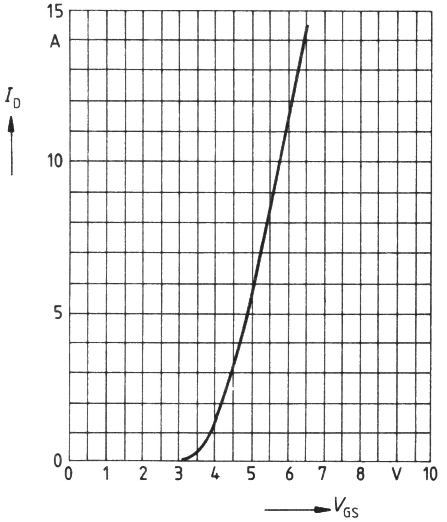


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

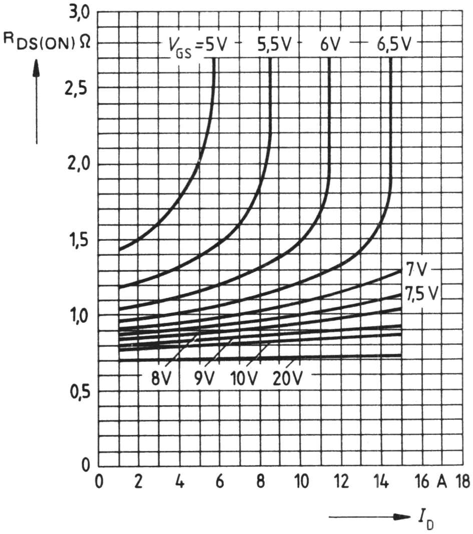


Fig. 6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

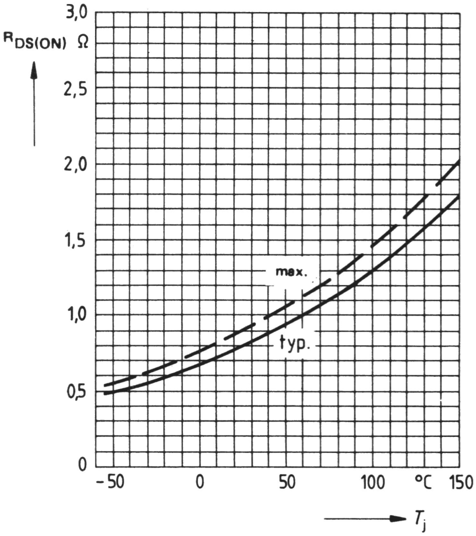


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 5\ A$; $V_{GS} = 10\ V$.

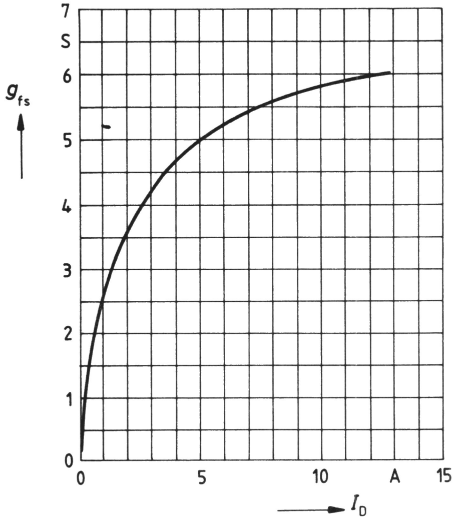


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\,°C$.

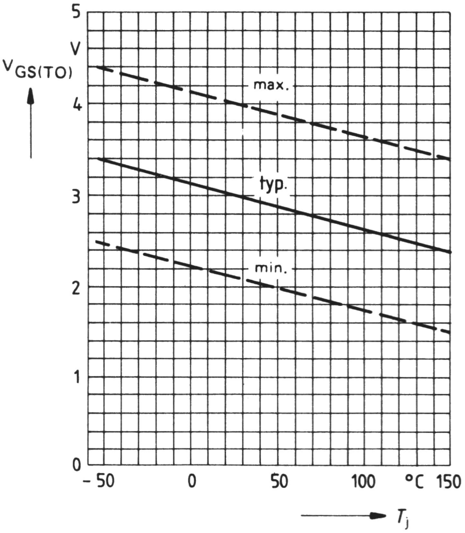


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

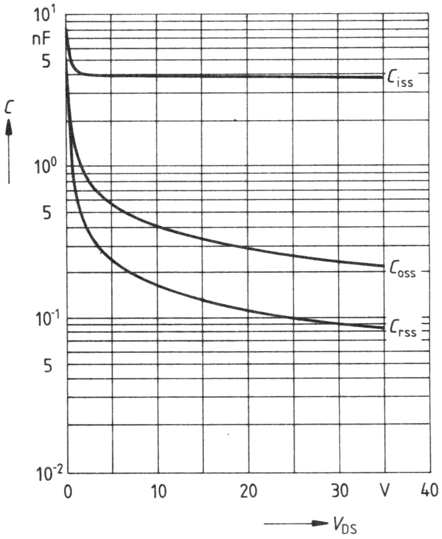


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

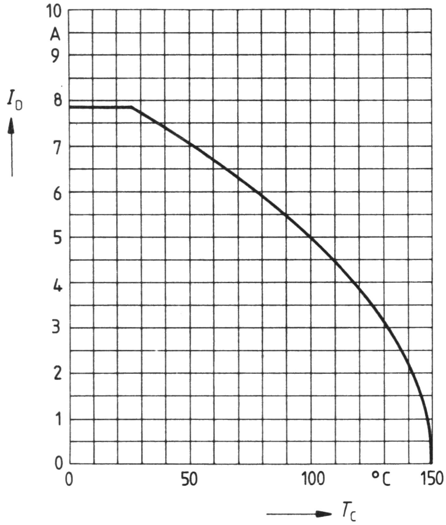


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

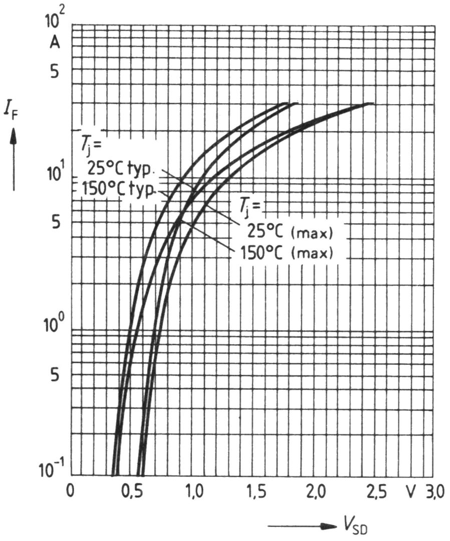


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

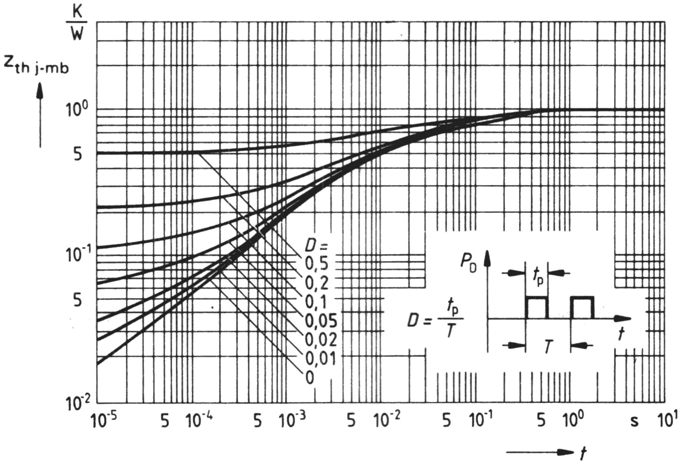


*Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.*

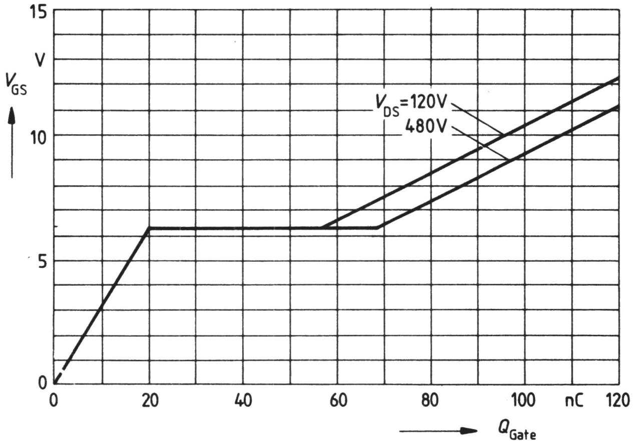


*Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 11{,}7\ A$.*

PowerMOS transistor BUZ83

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

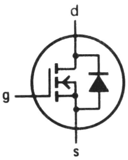
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	2,9	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	4,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



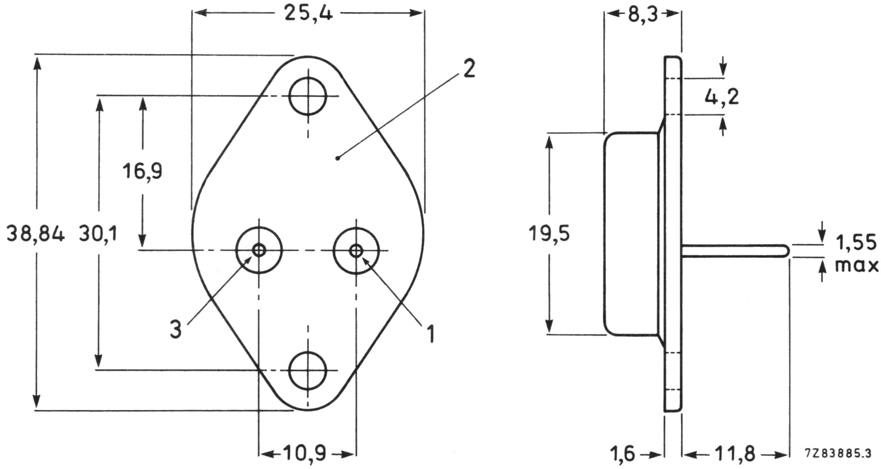


Fig. 1 *TO3; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,9	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	11	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,7 A	–	3,5	4,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,7 A	1,0	1,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,1 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	$T_{mb} = 25$ °C	–	–	2,9	A
I_{DRM}	Pulsed reverse drain current	$T_{mb} = 25$ °C	–	–	11	A
V_{SD}	Diode forward on-voltage	$I_F = 5{,}8$ A; $V_{GS} = 0$ V; $T_j = 25$ °C	–	1,05	1,3	V
t_{rr}	Reverse recovery time	$I_F = 2{,}9$ A; $T_j = 25$ °C	–	1800	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt = 100$ A/μs; $T_j = 25$ °C; $V_{GS} = 0$ V; $V_R = 100$ V	–	12	–	μC

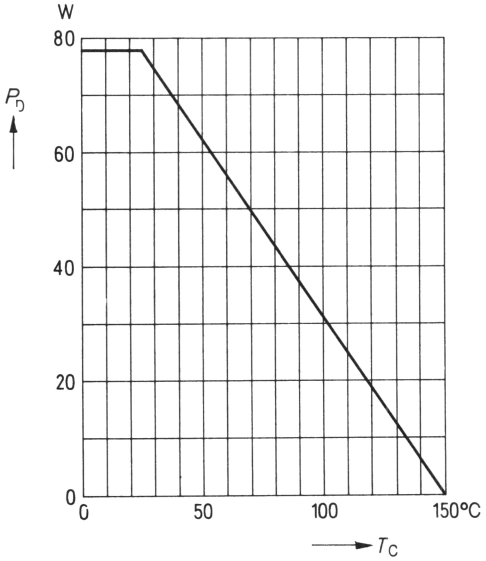


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

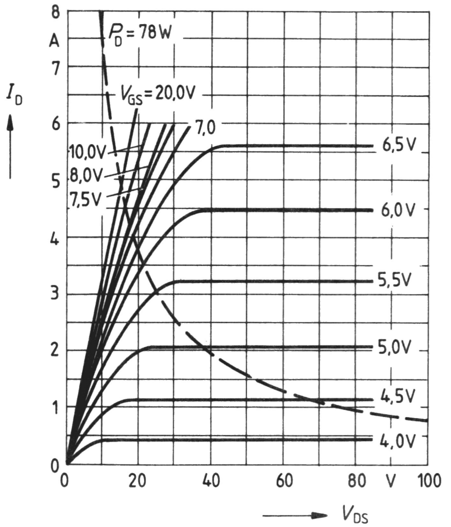


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

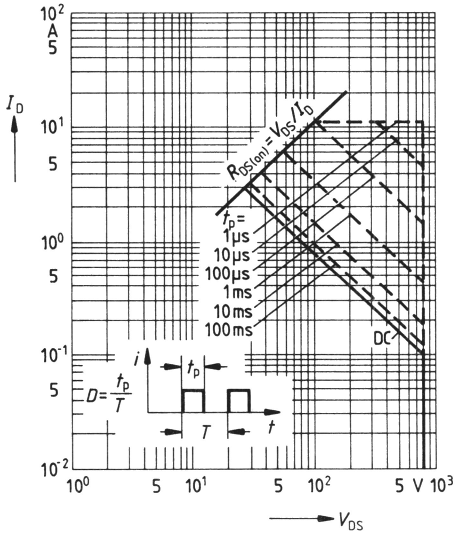


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

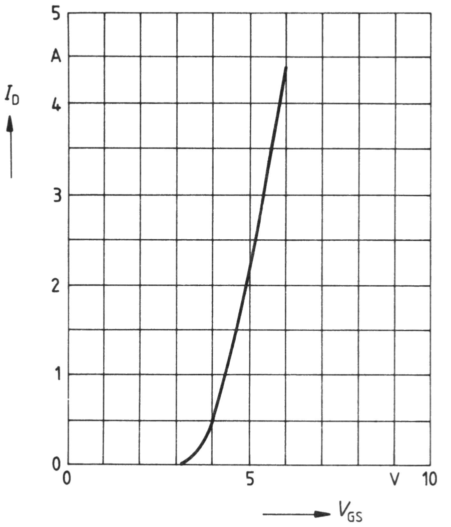


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

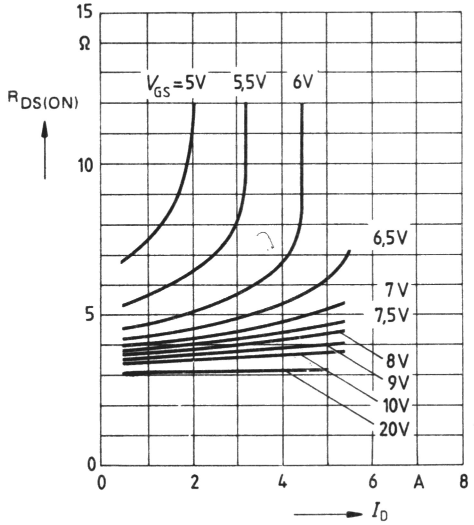


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

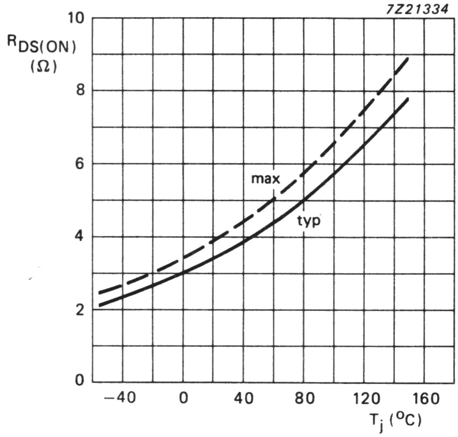


Fig.7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}7$ A; $V_{GS} = 10$ V.

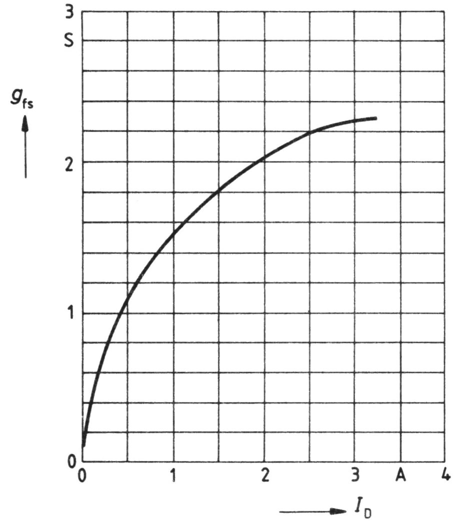


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

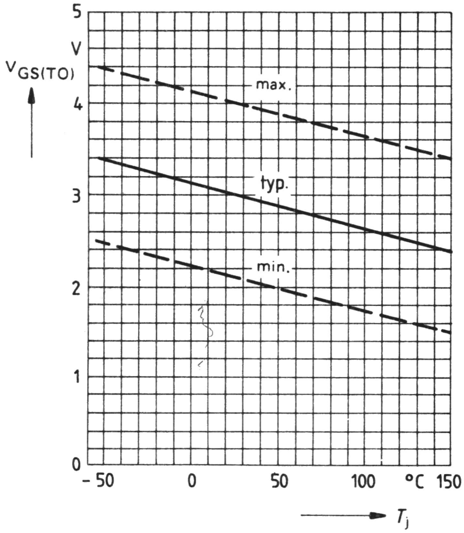


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

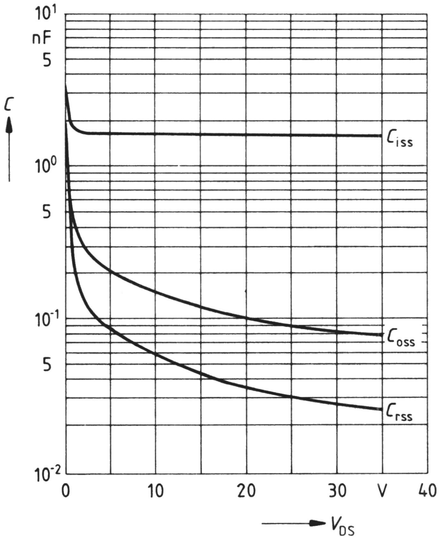


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

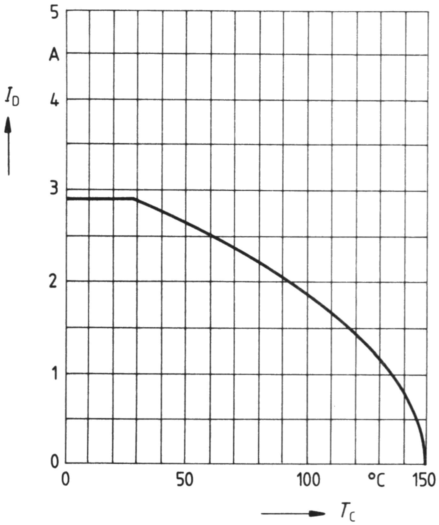


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

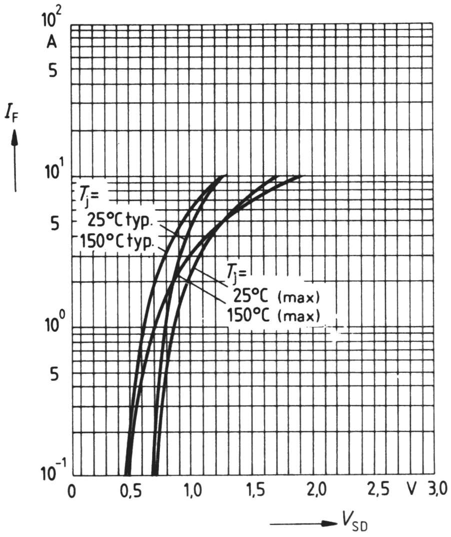


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *μs.*

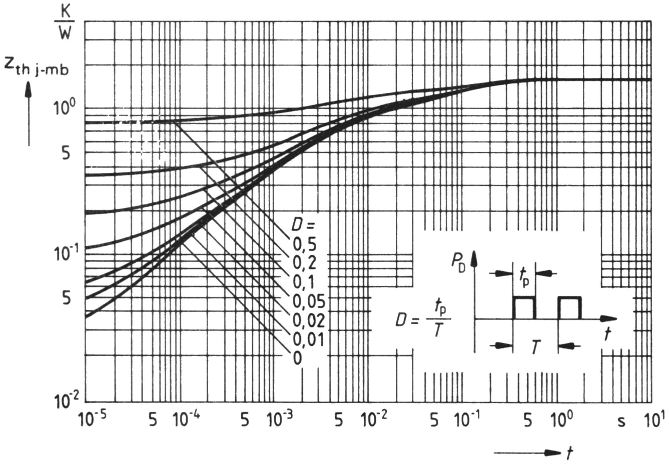


Fig.13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

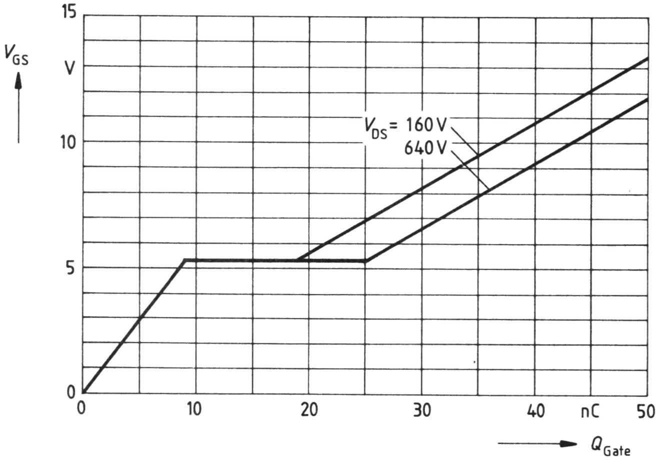


Fig.14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5$ A.

PowerMOS transistor

BUZ83A

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

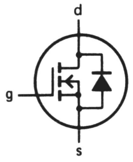
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	3,4	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	3,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



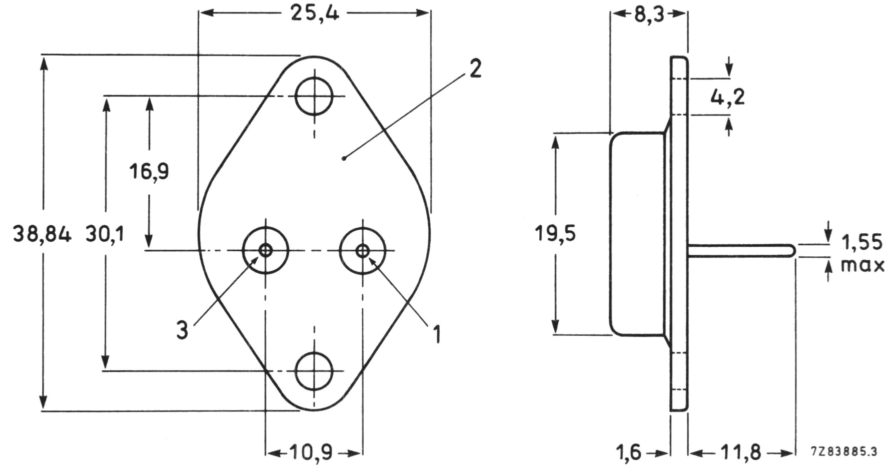


Fig. 1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	3,4	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	11	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,7 A	–	2,7	3,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,7 A	1,0	1,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	3,4	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	13	A
V_{SD}	Diode forward on-voltage	I_F = 6,8 A; V_{GS} = 0 V; T_j = 25 °C	–	1,1	1,35	V
t_{rr}	Reverse recovery time	I_F = 3,4 A; T_j = 25 °C	–	1800	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	12	–	μC

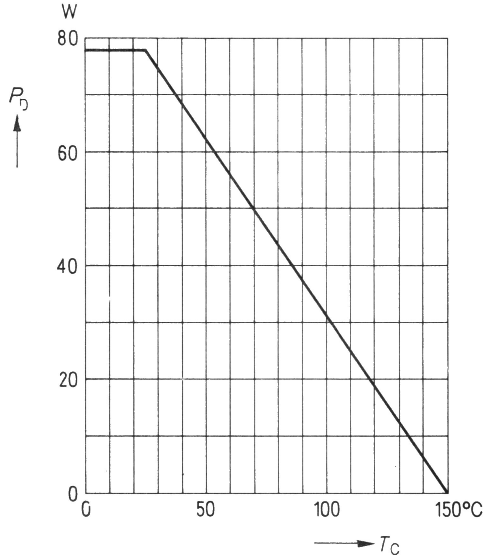


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

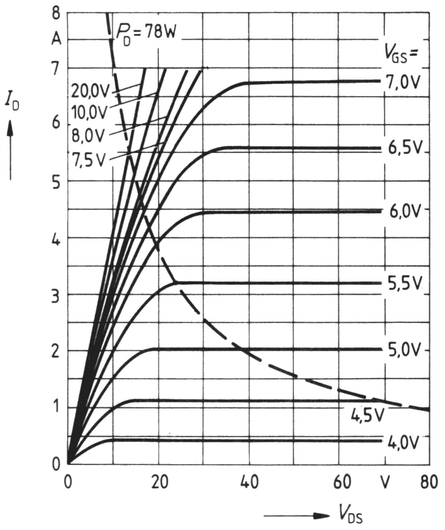


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25°C$.

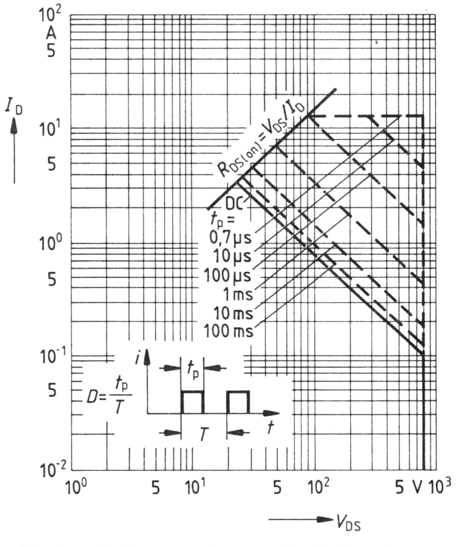


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0,01$; $T_{mb} = 25°C$.

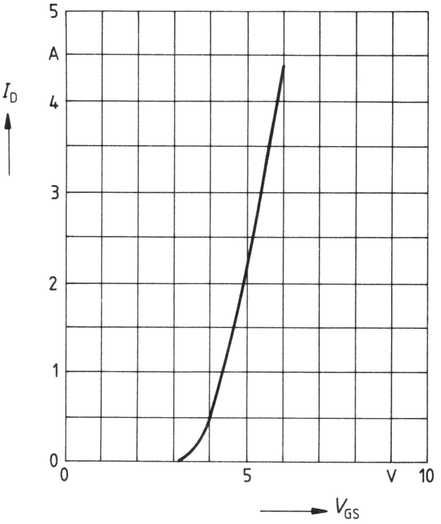


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25°C$.

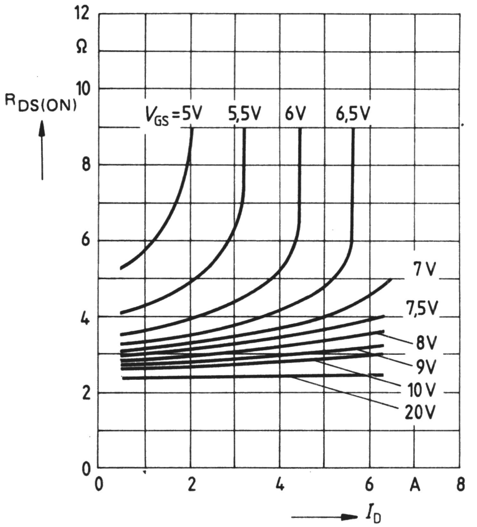


Fig. 6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

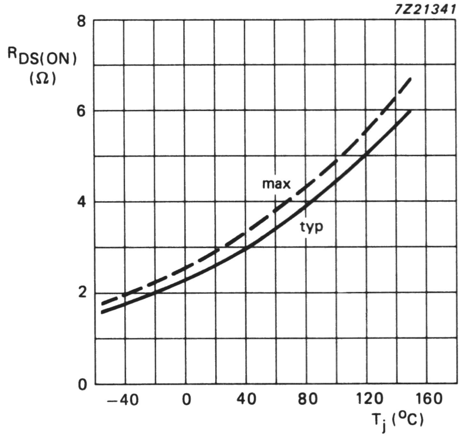


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}7\,A$; $V_{GS} = 10\,V$.

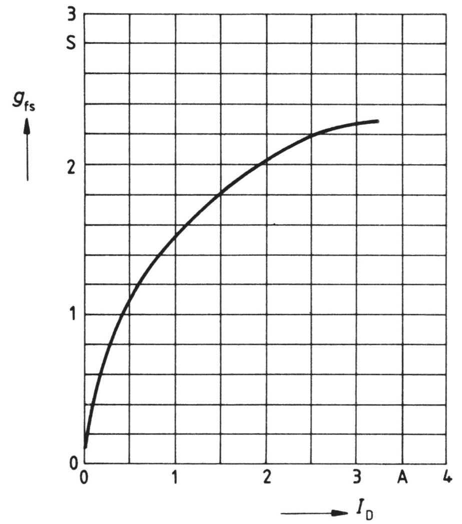


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25\,V$; $T_j = 25\,°C$.

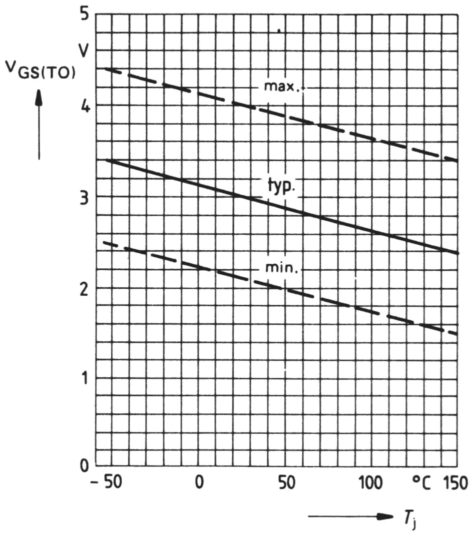


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.

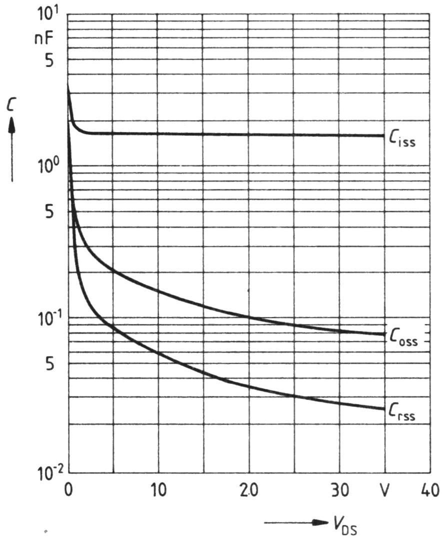


Fig. 10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

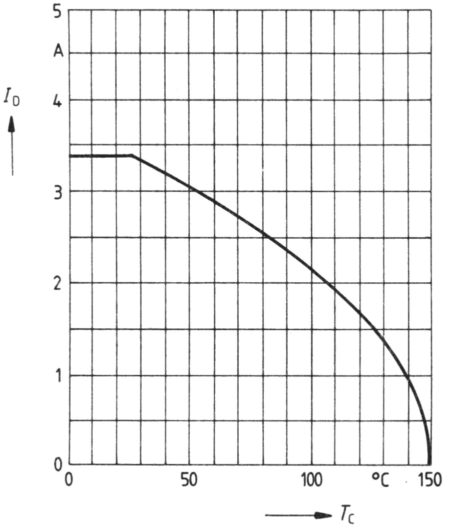


Fig. 11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

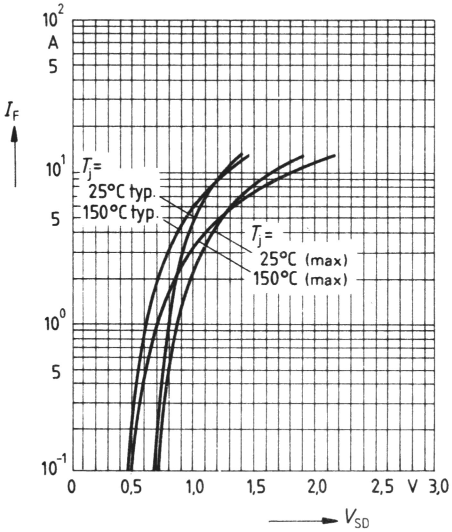


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

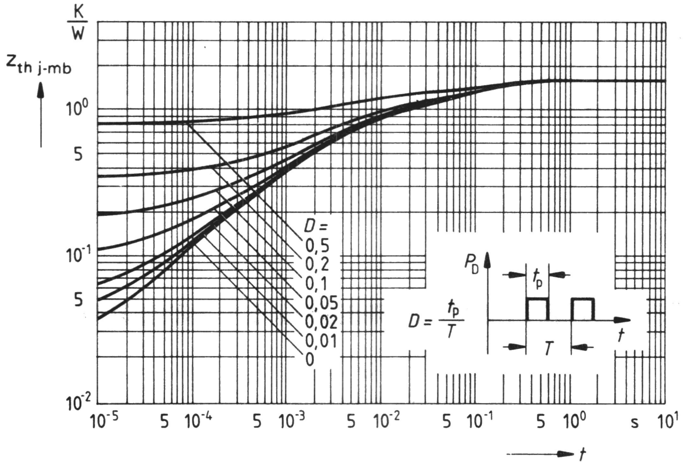


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

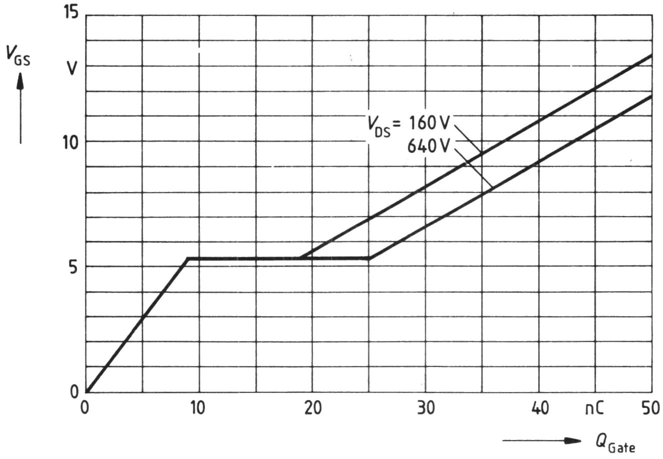


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5$ A.

PowerMOS transistor

BUZ84

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

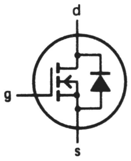
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	5,3	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



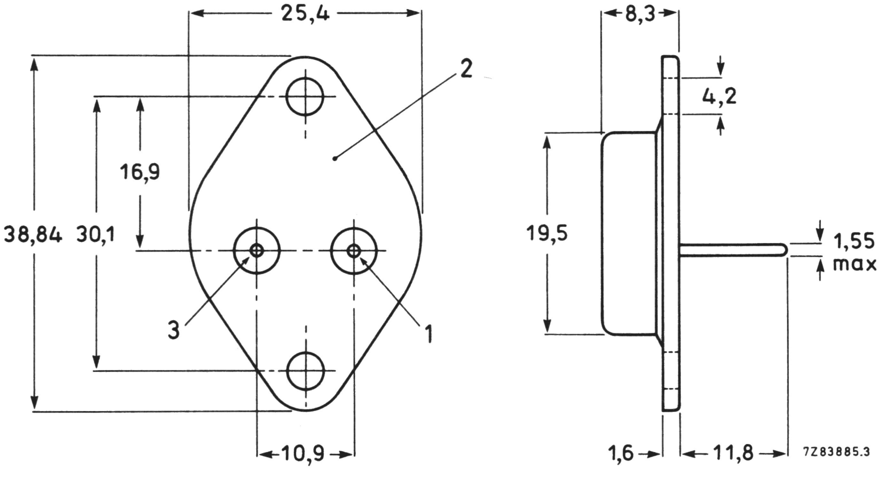


Fig. 1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	5,3	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,4	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	21	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3 A	–	1,6	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3 A	1,8	3,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	200	350	pF
C_{rss}	Feedback capacitance		–	80	140	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,3	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	21	A
V_{SD}	Diode forward on-voltage	I_F = 10,6 A; V_{GS} = 0 V; T_j = 25 °C	–	1,0	1,45	V
t_{rr}	Reverse recovery time	I_F = 5,3 A; T_j = 25 °C	–	1800	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/µs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	25	–	µC

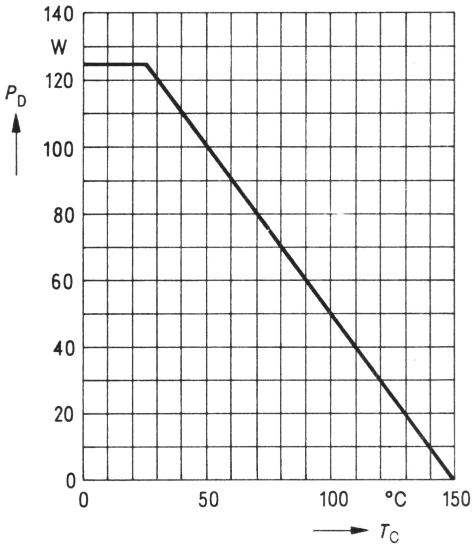


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

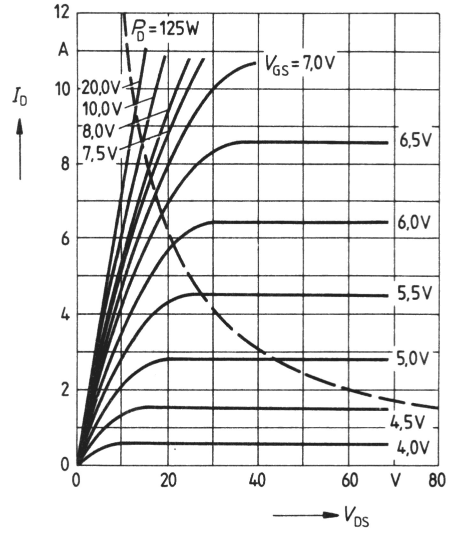


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

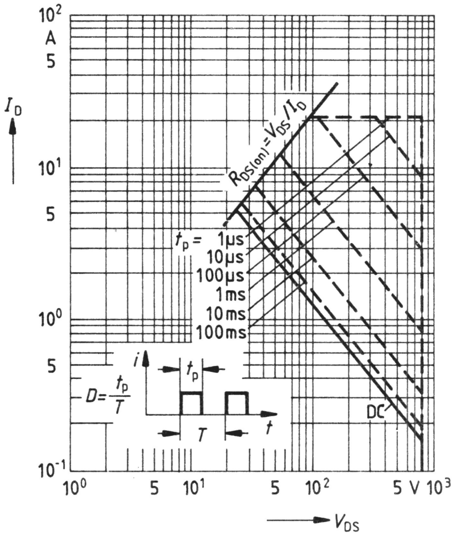


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0,01$; $T_{mb} = 25$ °C.

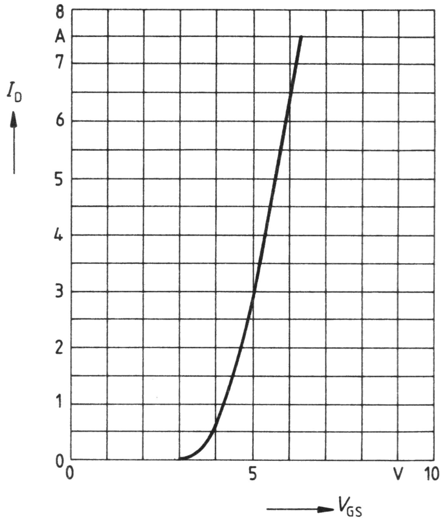


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

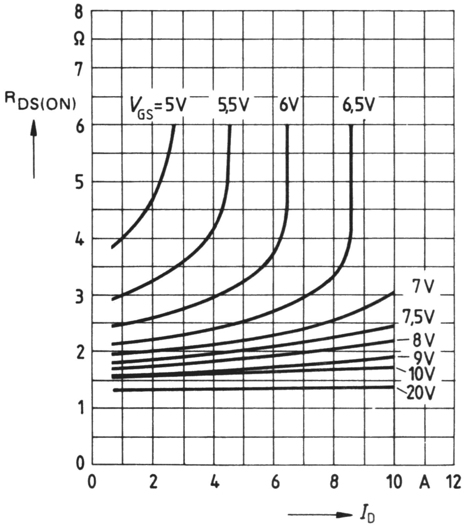


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; $T_j = 25\,°C$.*

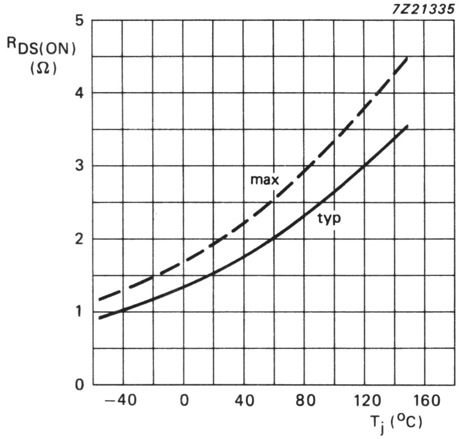


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: $I_D = 3\,A$; $V_{GS} = 10\,V$.*

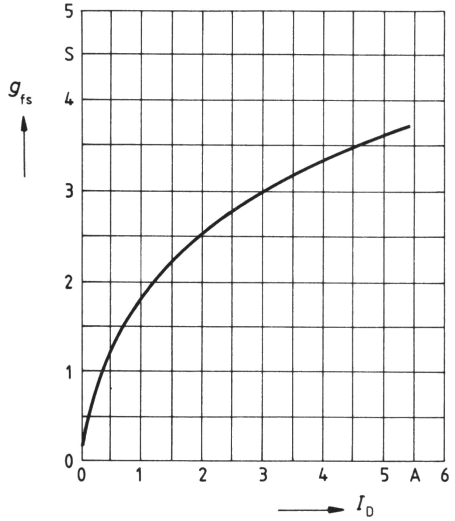


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 μs pulse test; $V_{DS} = 25\,V$; $T_j = 25\,°C$.*

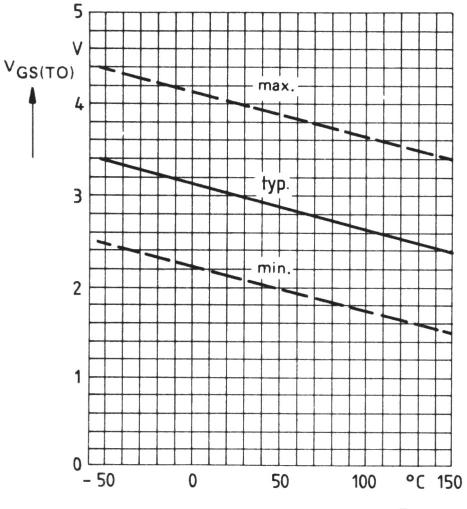


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; $I_D = 1\,mA$.*

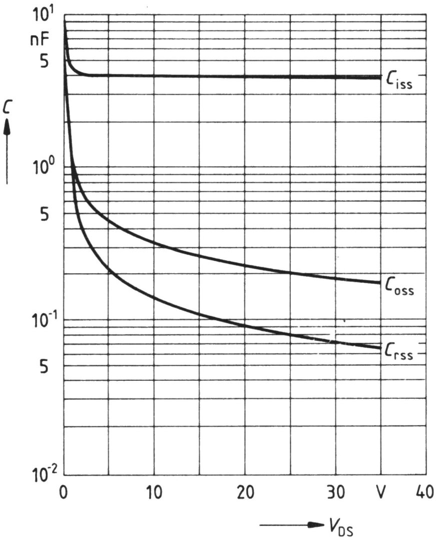


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

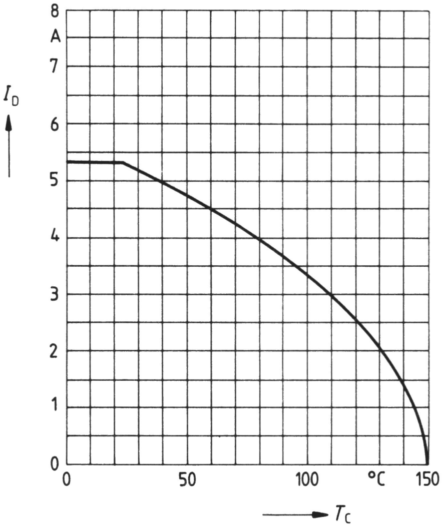


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

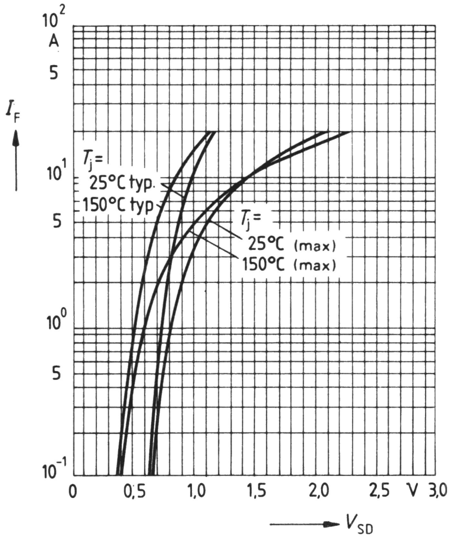


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

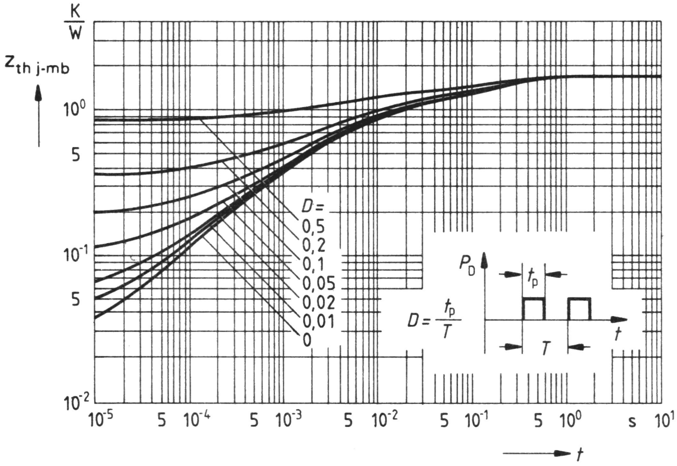


*Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.*

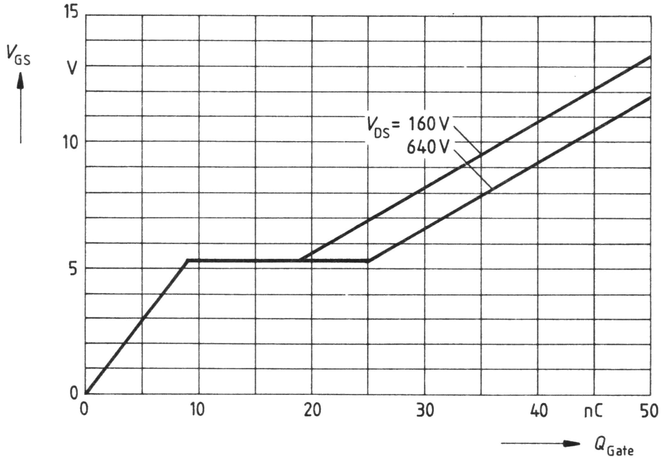


*Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 9$ A.*

PowerMOS transistor BUZ84A

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

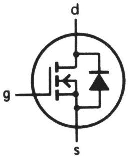
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	6,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



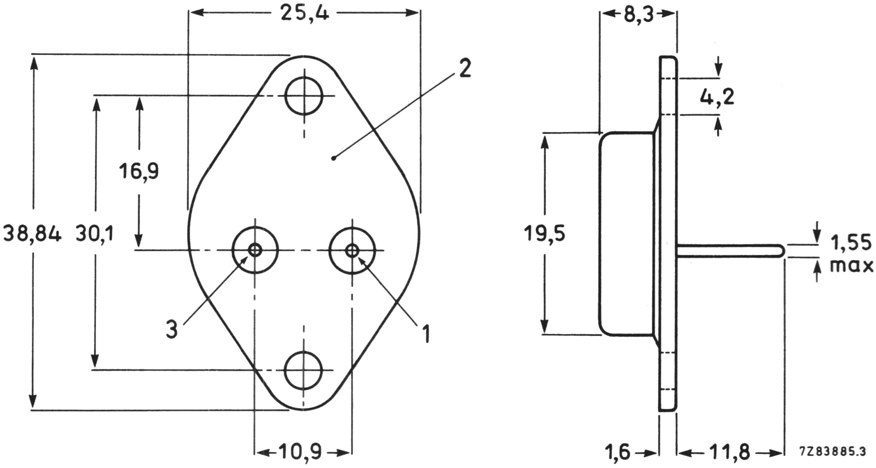


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	6,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	24	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3 A	–	1,3	1,5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3 A	1,8	3,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	200	350	pF
C_{rss}	Feedback capacitance		–	80	140	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,6 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	6,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	24	A
V_{SD}	Diode forward on-voltage	I_F = 12 A; V_{GS} = 0 V; T_j = 25 °C	–	1,1	1,5	V
t_{rr}	Reverse recovery time	I_F = 6 A; T_j = 25 °C	–	1800	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	25	–	μC

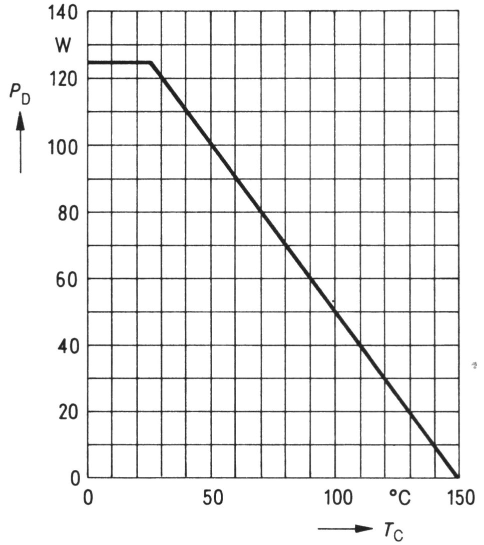


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

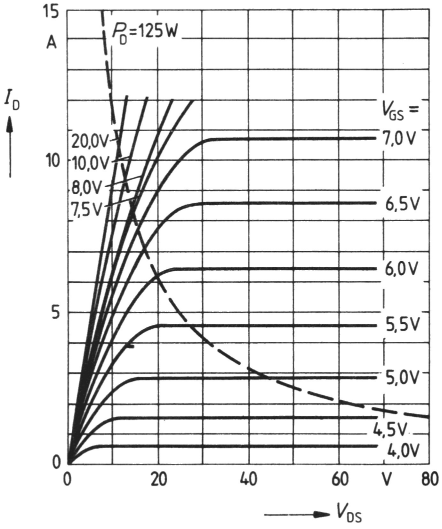


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$
Parameter: V_{GS}; *80 µs pulse test;*
$T_{mb} = 25°C$.

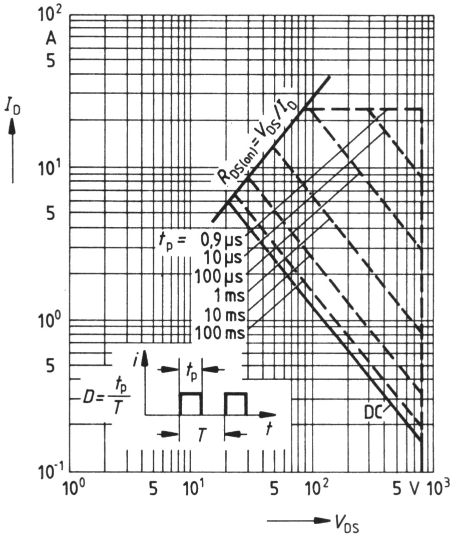


Fig.4 *Safe operating area* $I_D(DC)$ *and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25°C$.

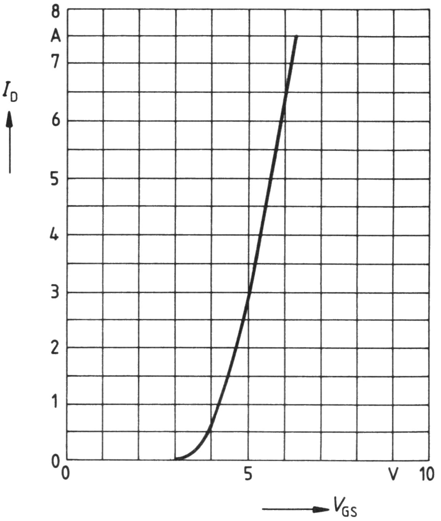


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25°C$.

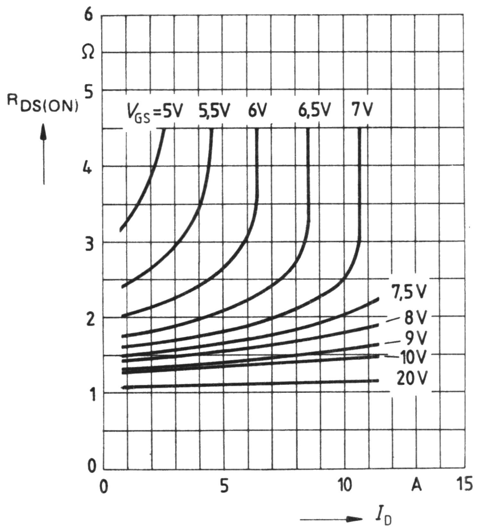


Fig. 6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

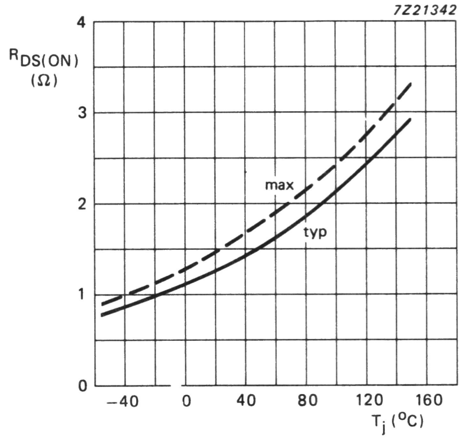


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 3$ A; $V_{GS} = 10$ V.

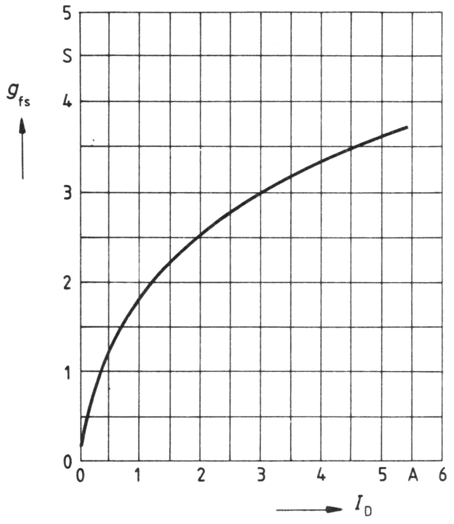


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

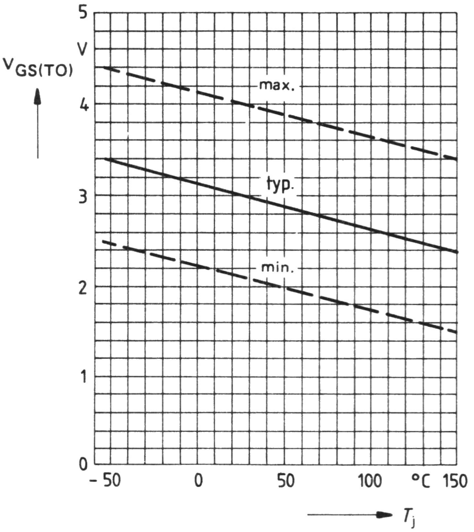


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

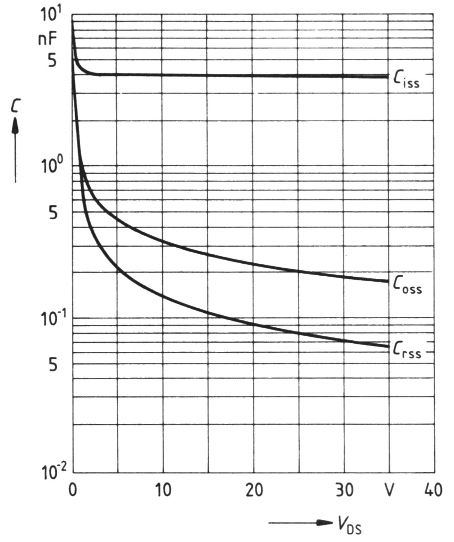


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

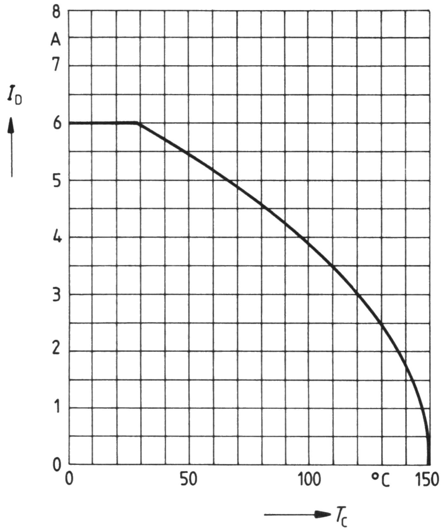


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

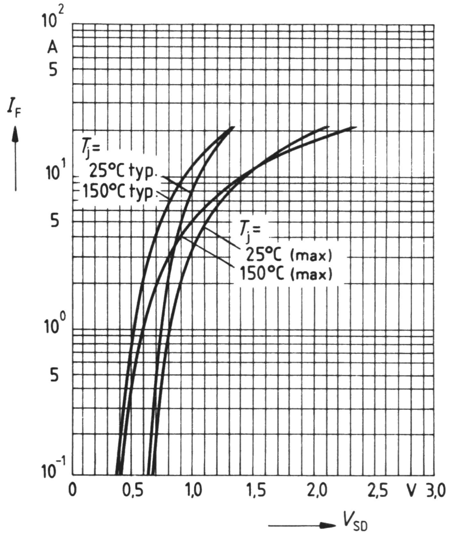


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

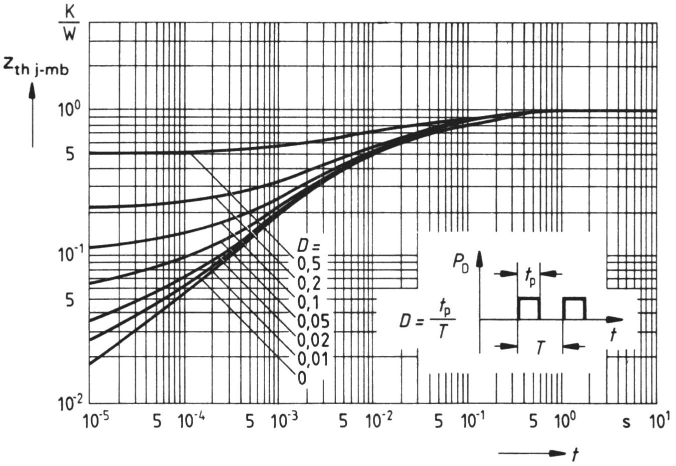


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

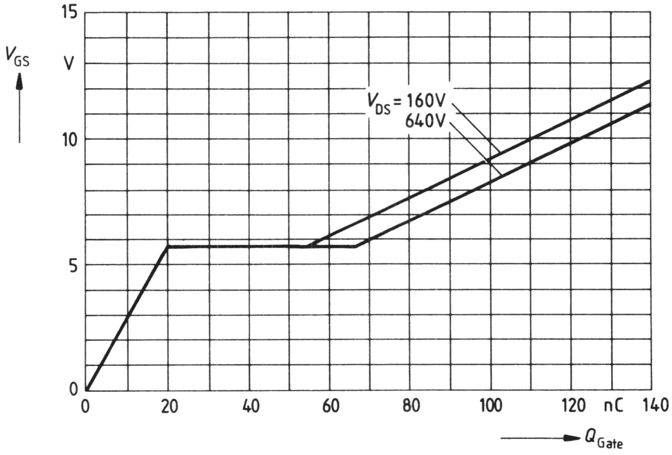


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 9\ A$.

PowerMOS transistor BUZ53A

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

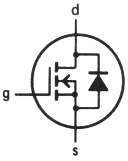
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,6	A
P_{tot}	Total power dissipation	78	W
$R_{DS(ON)}$	Drain-source on-state resistance	5,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



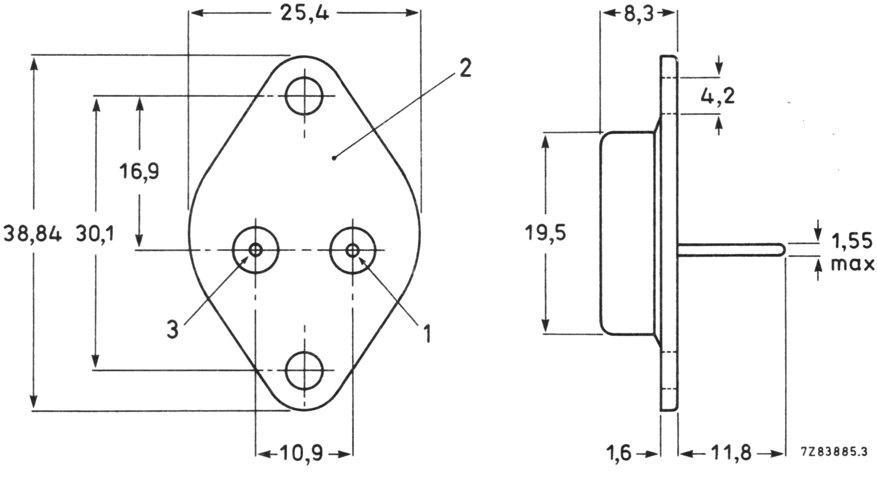


Fig. 1 *TO3; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	2,6	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	78	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,6 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	4,5	5,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	0,7	1,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,6	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5,2 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,6 A; T_j = 25 °C	–	2000	–	ns
Q_{rr}	Reverse recovery charge	$-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	15	–	μC

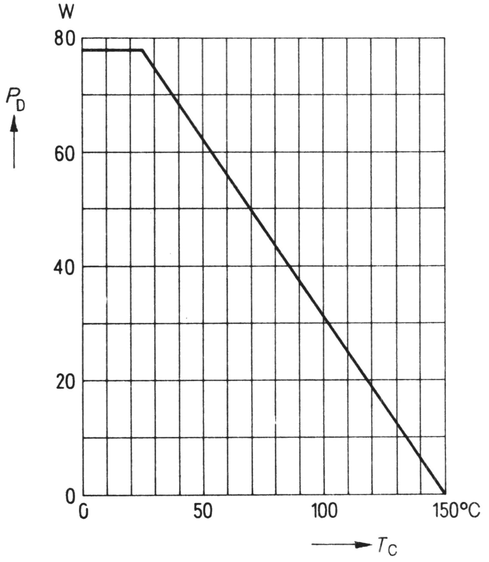


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

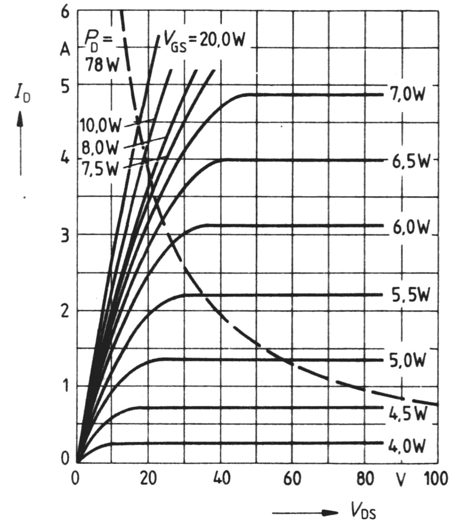


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

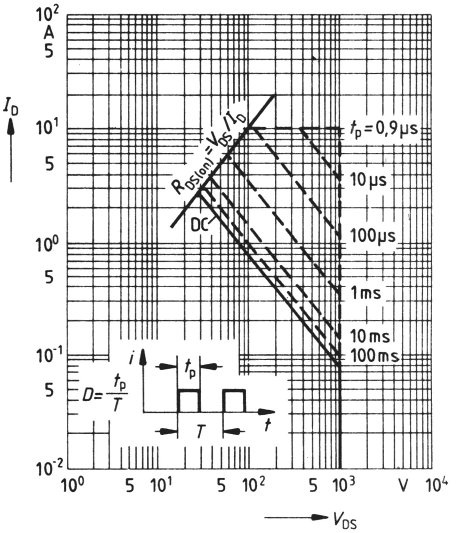


Fig. 4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

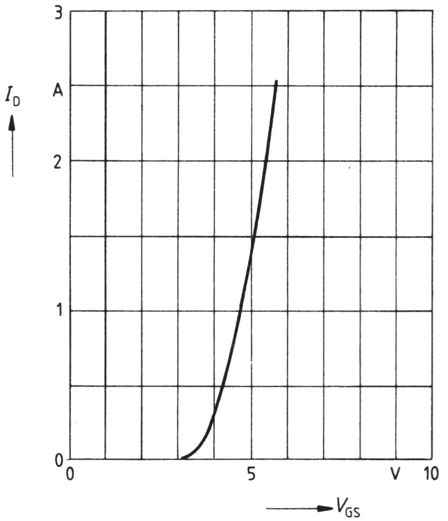


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

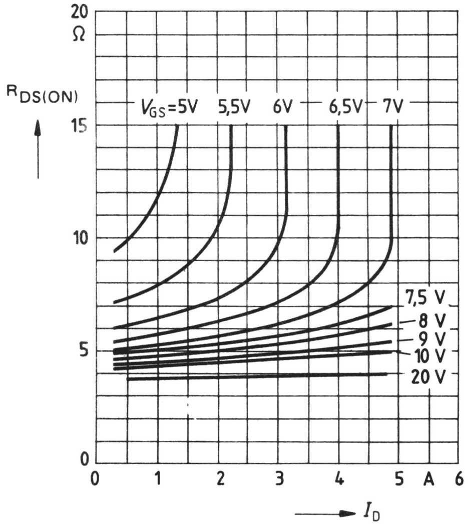


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

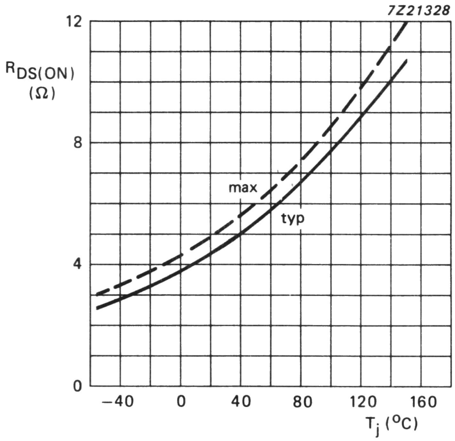


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

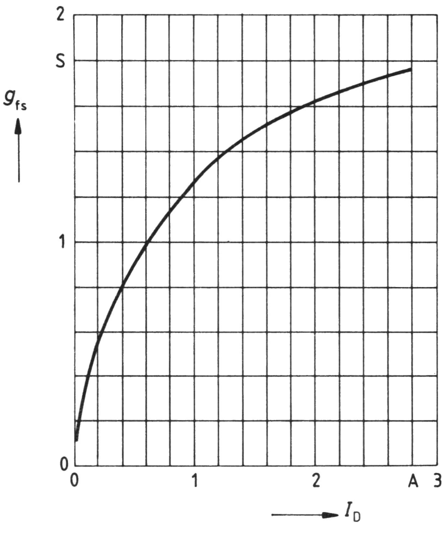


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

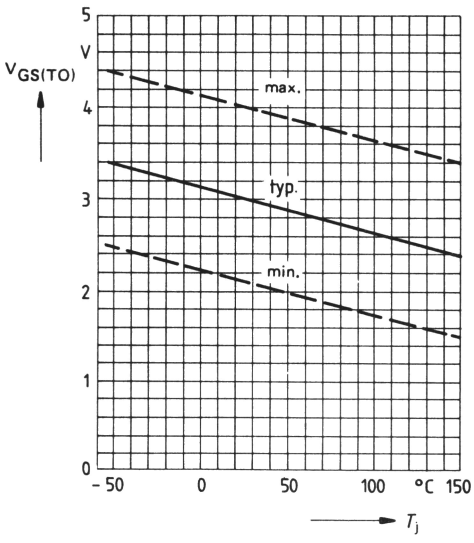


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

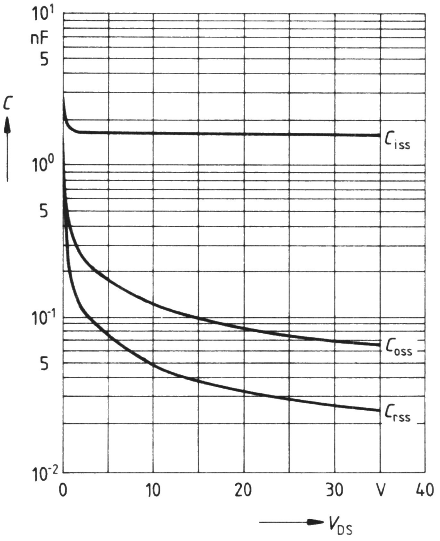


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

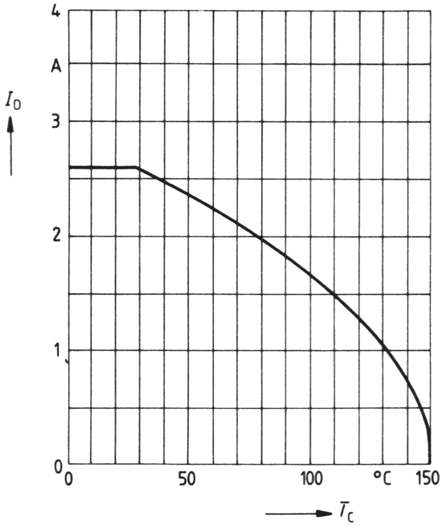


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

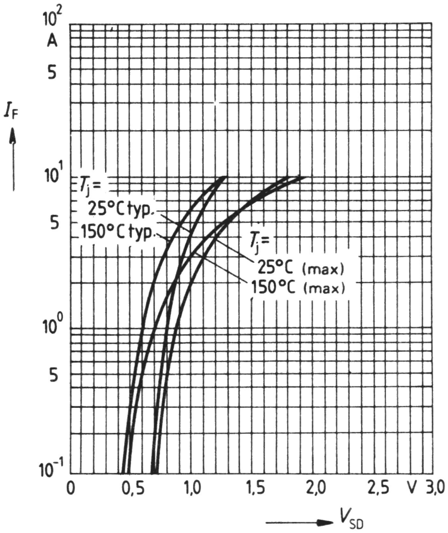


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

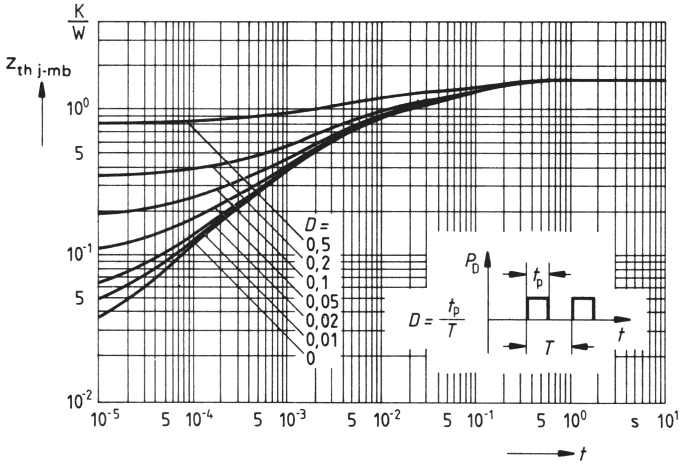


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

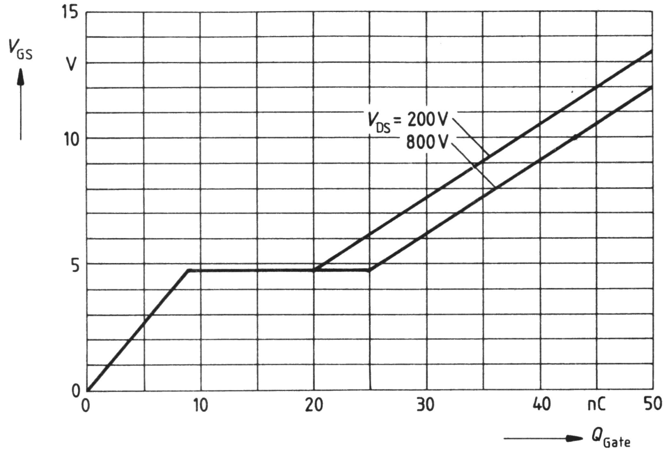


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 3{,}75$ *A.*

PowerMOS transistor BUZ54

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

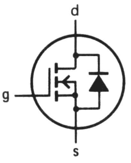
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	5,1	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source



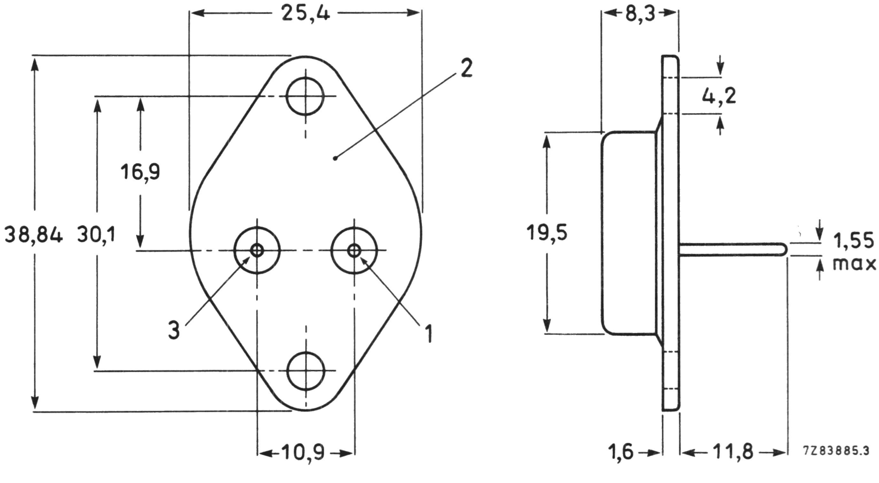


Fig.1 TO3; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	5,1	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	20	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,6 A	–	1,7	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,6 A	1,4	3,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	180	300	pF
C_{rss}	Feedback capacitance		–	70	120	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,1	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	20	A
V_{SD}	Diode forward on-voltage	I_F = 10,2 A; V_{GS} = 0 V; T_j = 25 °C	–	1,15	1,4	V
t_{rr}	Reverse recovery time	I_F = 5,1 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	2000	–	ns
Q_{rr}	Reverse recovery charge		–	30	–	μC

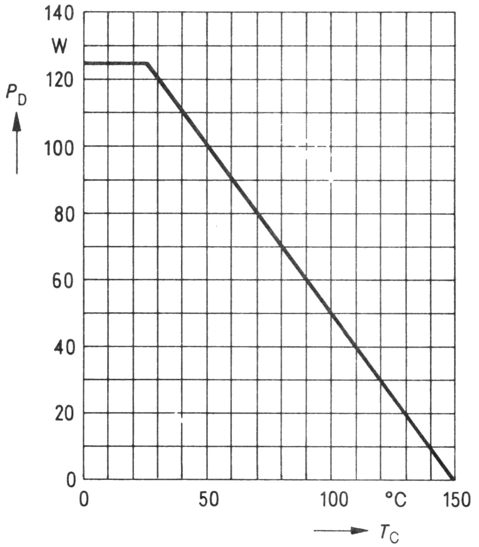


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

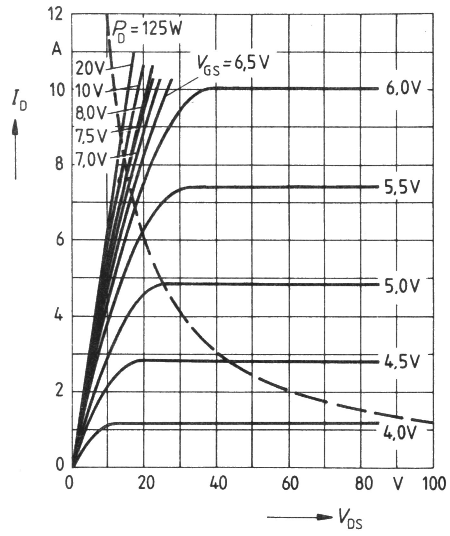


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

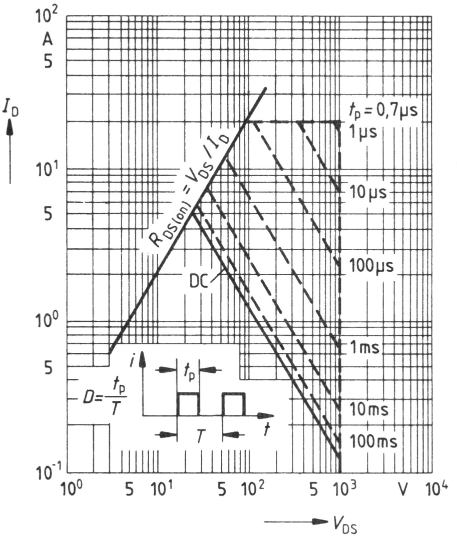


Fig. 4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

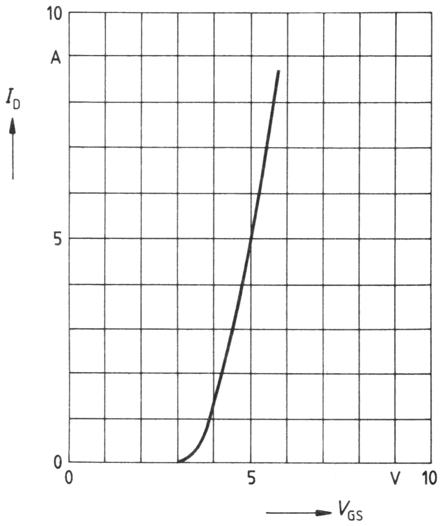


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

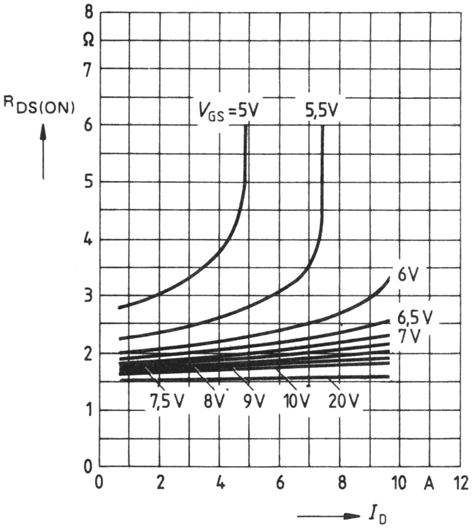


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

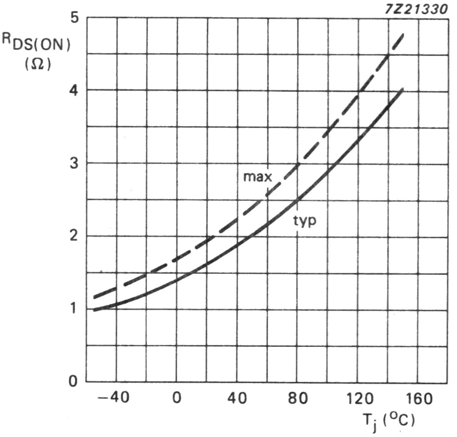


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 2,6 A; V_{GS} = 10 V.

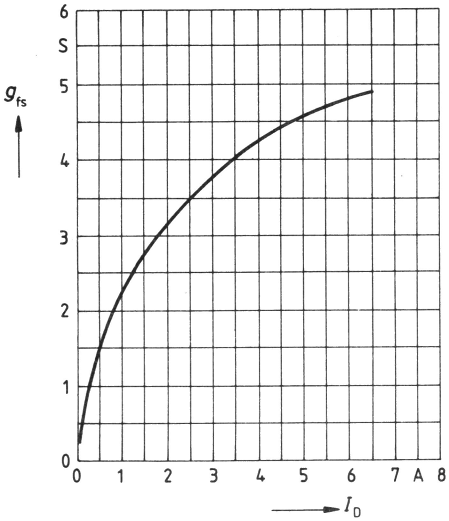


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

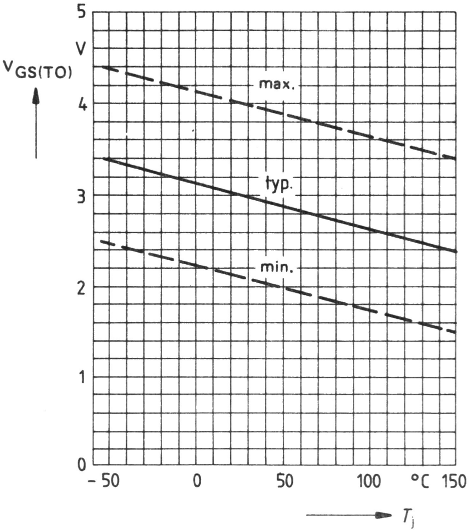


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

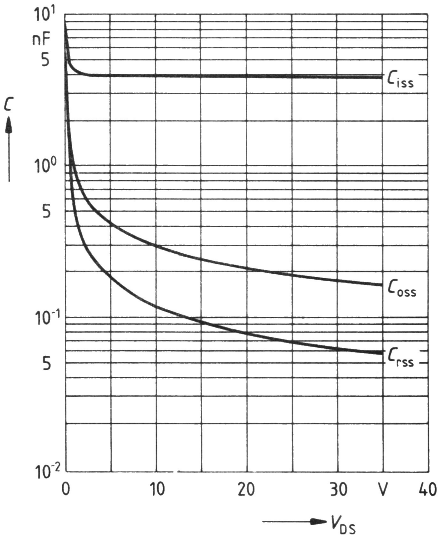


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

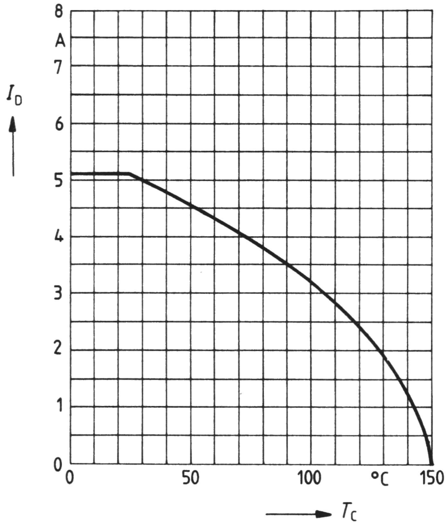


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

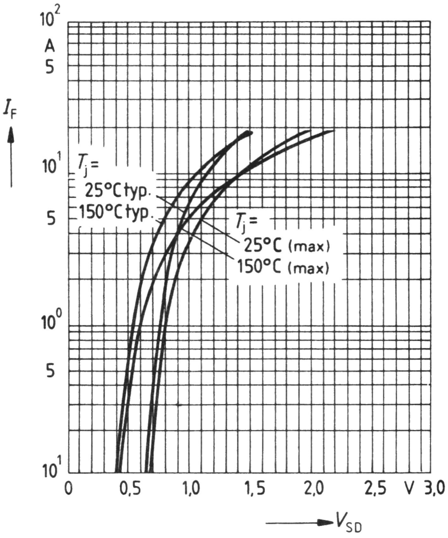


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

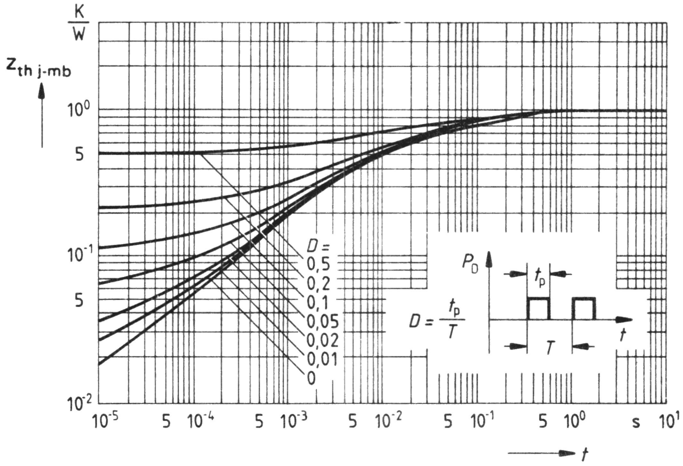


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

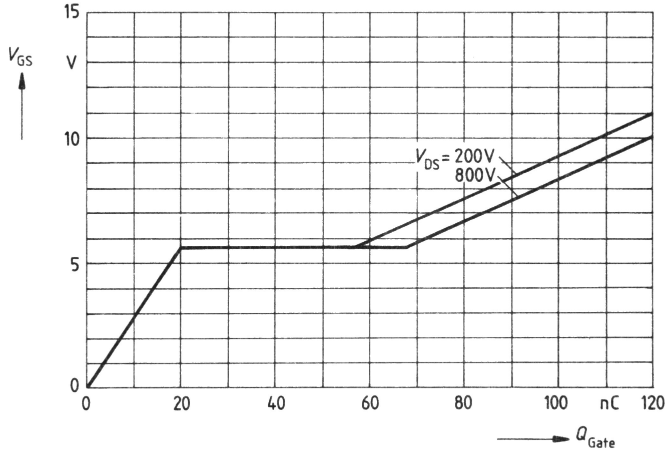


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 8{,}0$ A.

PowerMOS transistor

BUZ54A

July 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a metal envelope.

This device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	4,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,6	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 12 g

Pinning:
1 = Gate
2 = Drain
3 = Source

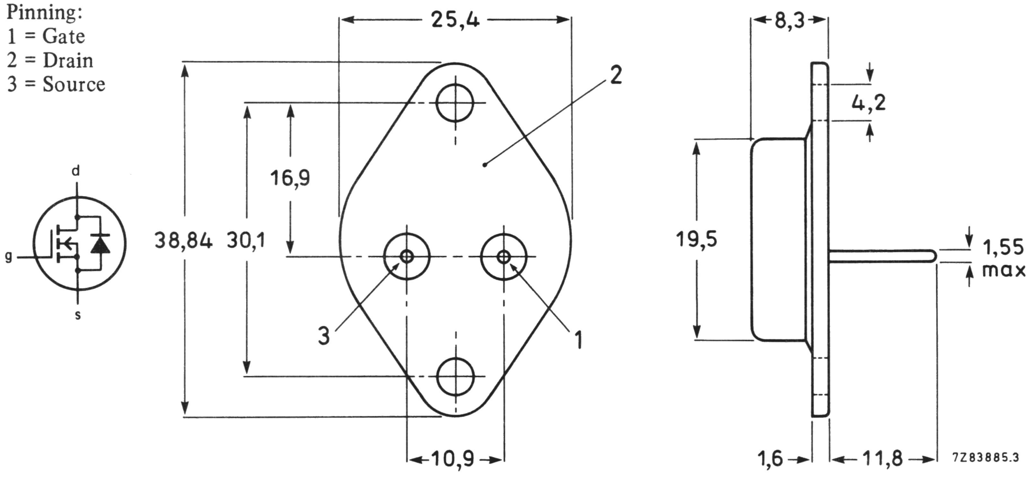


Fig. 1 *TO3; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO3 envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	4,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	18	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 35 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 2,6 A	–	2,3	2,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 2,6 A	1,4	3,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	180	300	pF
C_{rss}	Feedback capacitance		–	60	90	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,4 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on header closer to source pin and centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	4,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	18	A
V_{SD}	Diode forward on-voltage	I_F = 9 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	1,4	V
t_{rr}	Reverse recovery time	I_F = 4,5 A; T_j = 25 °C $-dI_F/dt$ = 100 A/μs; T_j = 25 °C; V_{GS} = 0 V; V_R = 100 V	–	2000	–	ns
Q_{rr}	Reverse recovery charge		–	30	–	μC

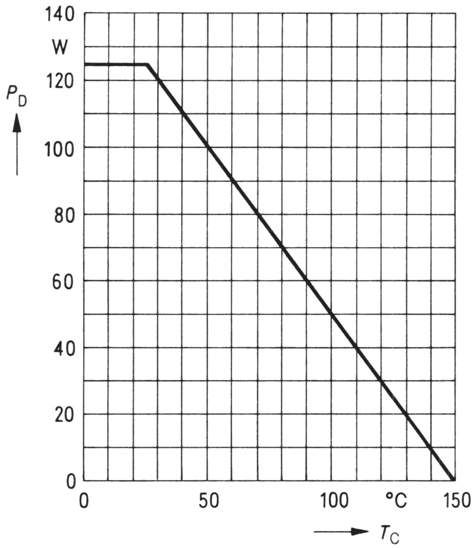


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

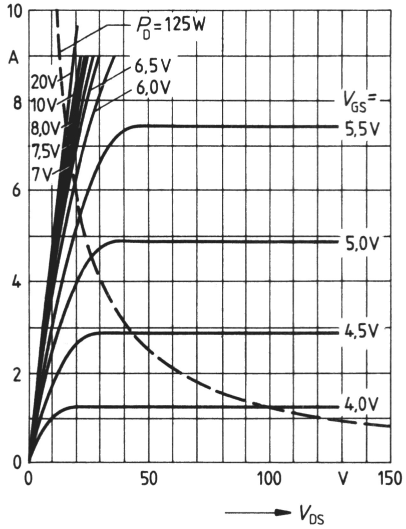


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

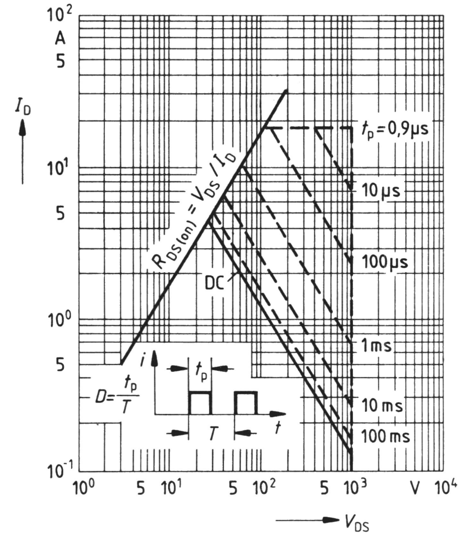


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

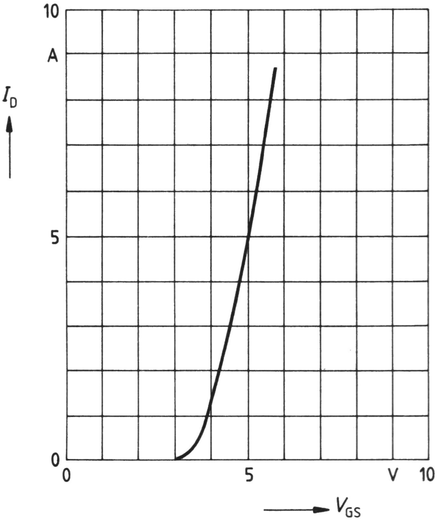


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

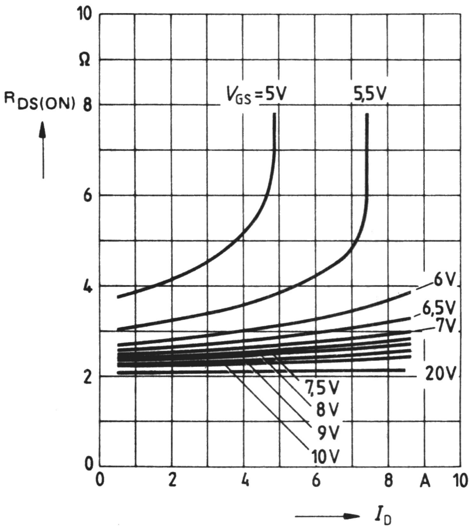


Fig. 6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\,°C$.

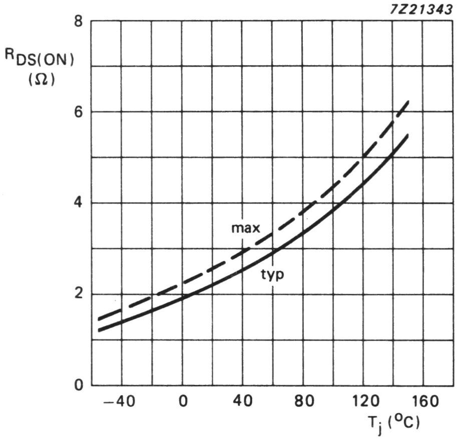


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 2{,}6$ A; $V_{GS} = 10$ V.

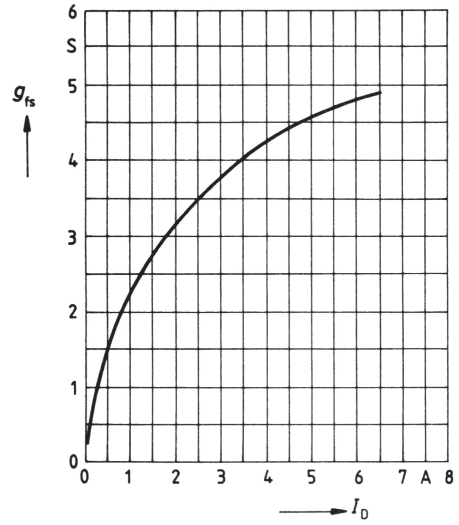


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25$ V; $T_j = 25\,°C$.

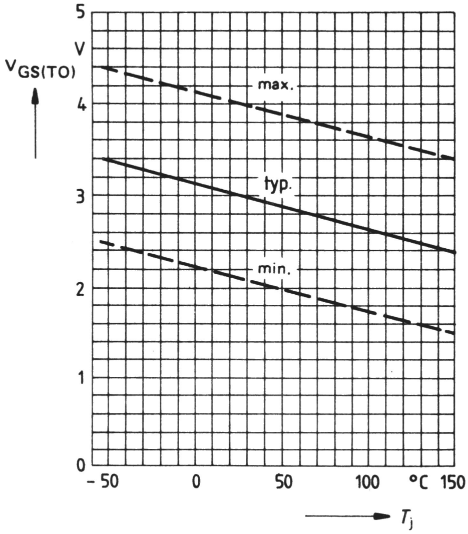


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

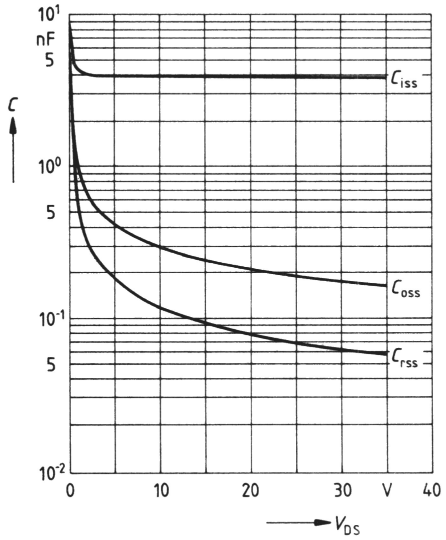


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

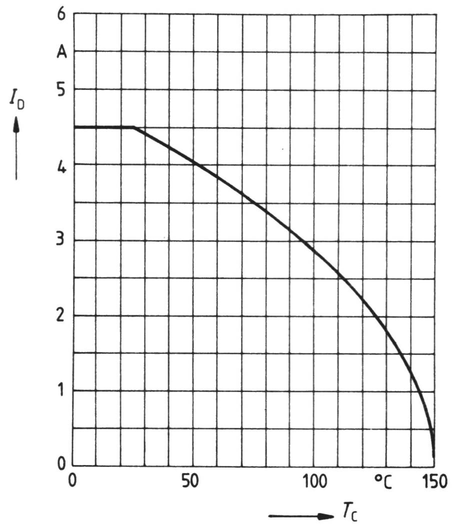


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

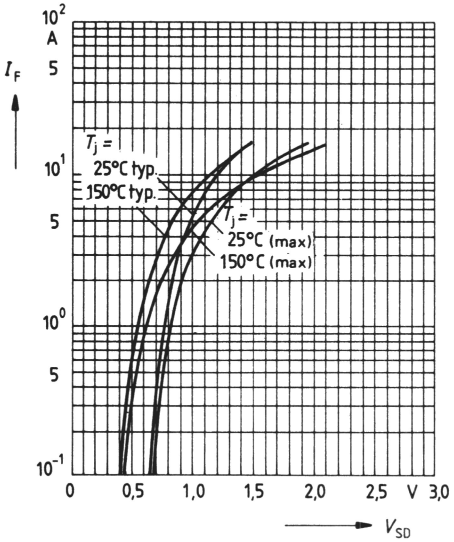


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

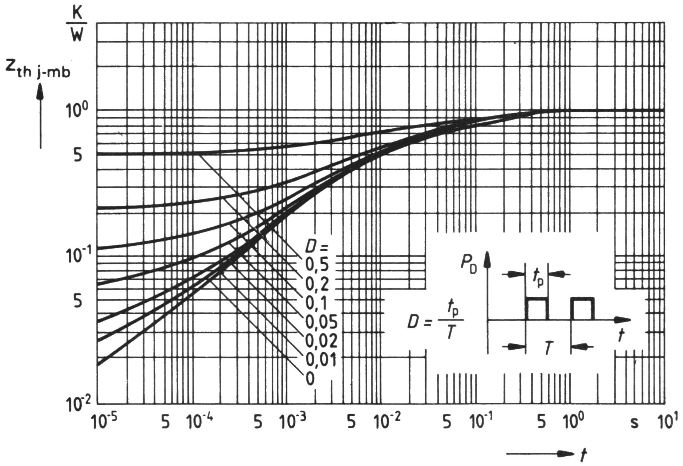


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

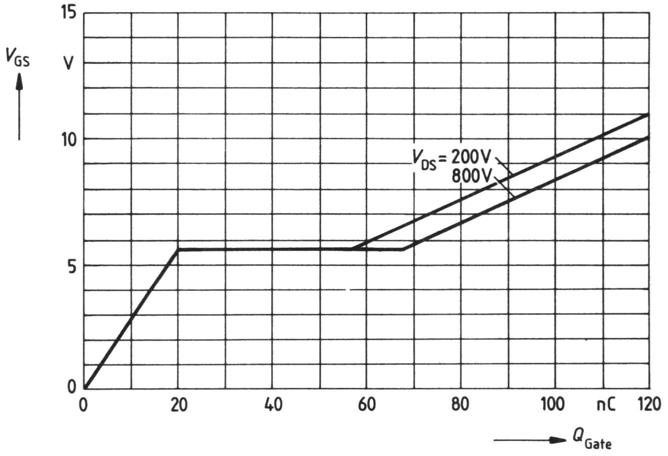


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 8{,}0$ A.

PowerMOS transistor BUZ347

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

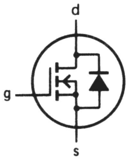
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	40	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,03	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



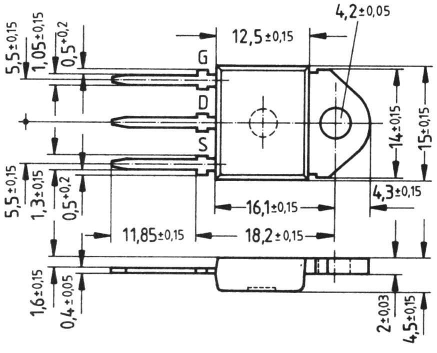

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for **TO218AA envelopes.**

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	40	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	160	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	65	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 28 A	–	0,025	0,03	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 28 A	7,0	18,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	1300	2000	pF
C_{rss}	Feedback capacitance		–	500	800	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	110	170	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	250	330	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	40	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	160	A
V_{SD}	Diode forward on-voltage	I_F = 80 A; V_{GS} = 0 V	–	1,6	1,95	V
t_{rr}	Reverse recovery time	I_F = 40 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 30 V	–	150	–	ns
Q_{rr}	Reverse recovery charge		–	1,0	–	μC

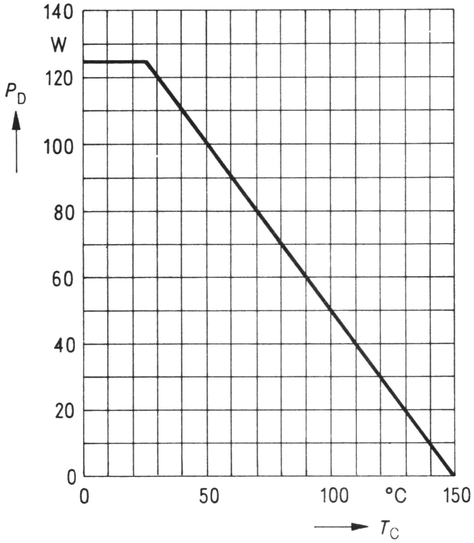


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

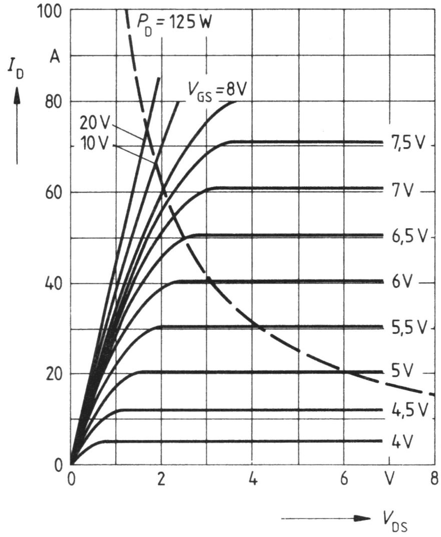


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 µs pulse test; T_{mb} = 25 °C.*

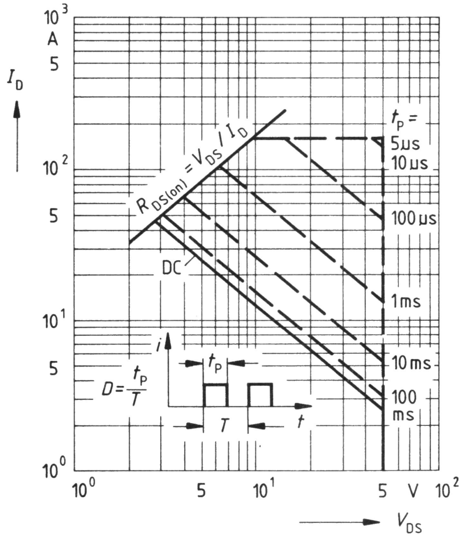


Fig.4 *Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

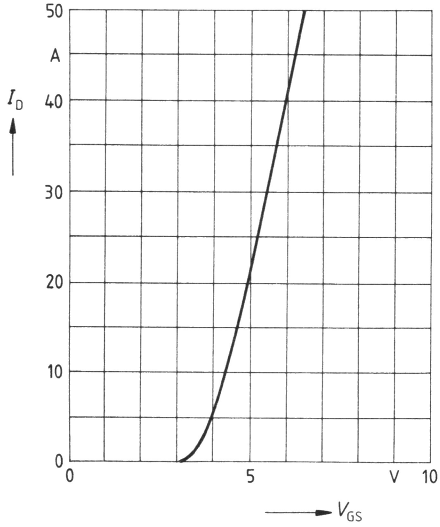


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 µs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

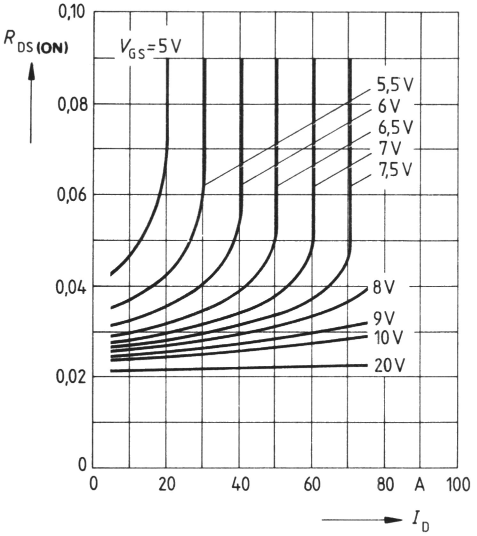


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25\ °C$.

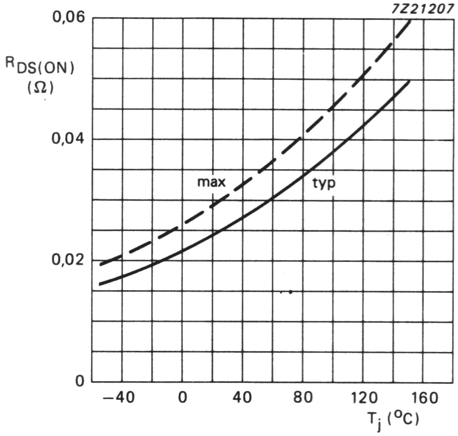


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 28\ A$; $V_{GS} = 10\ V$.

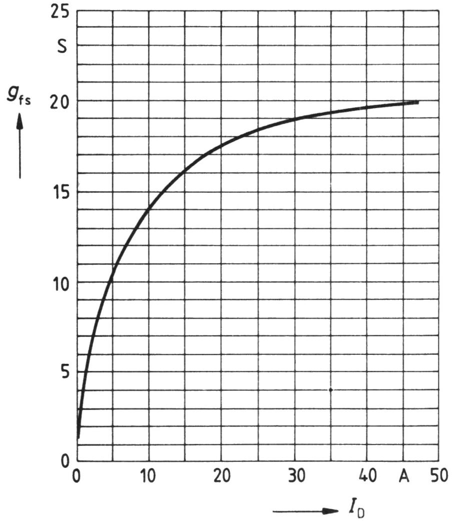


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
$V_{DS} = 25\ V$; $T_j = 25\ °C$.

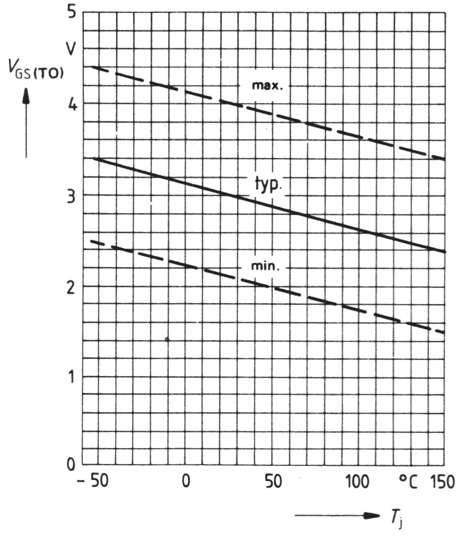


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1\ mA$.

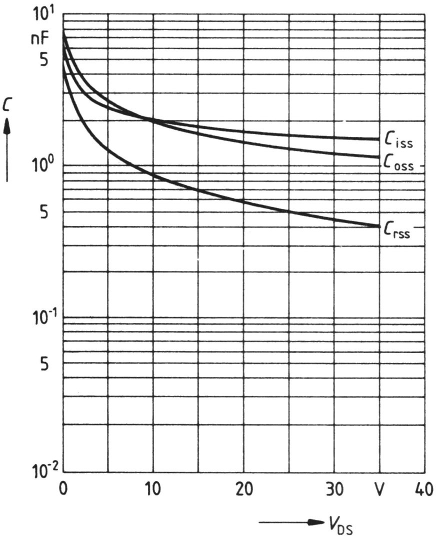


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

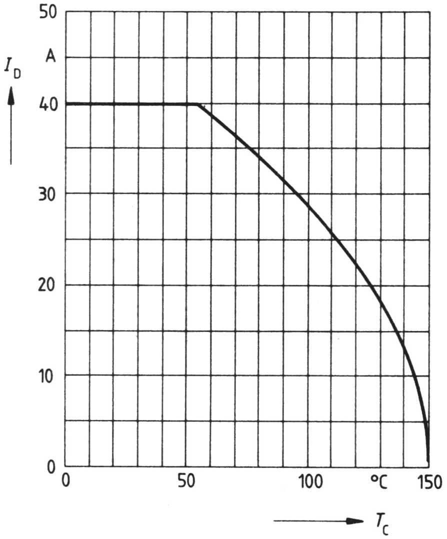


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

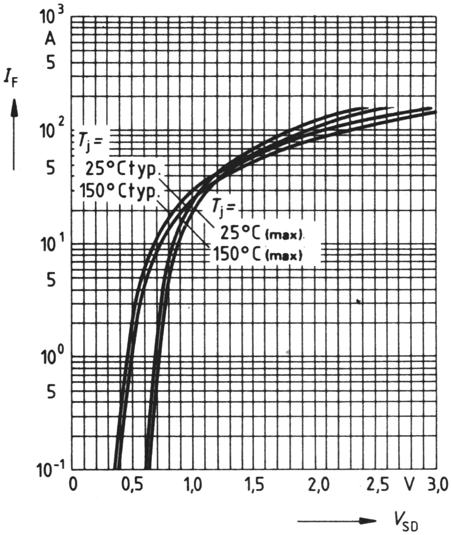


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

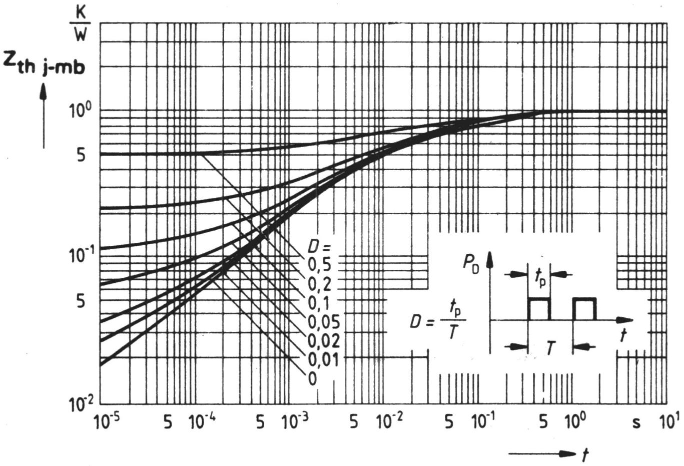


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

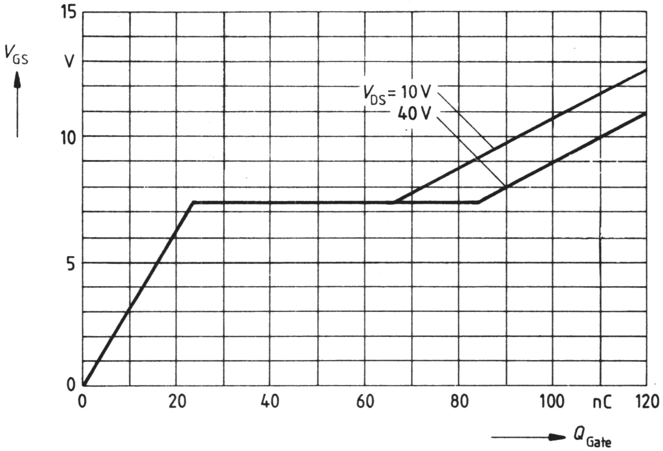


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; I_{DM} = 67,5 A.

PowerMOS transistor BUZ348

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

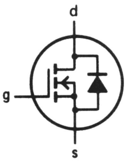
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	50	V
I_D	Drain current (d.c.)	39	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,04	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



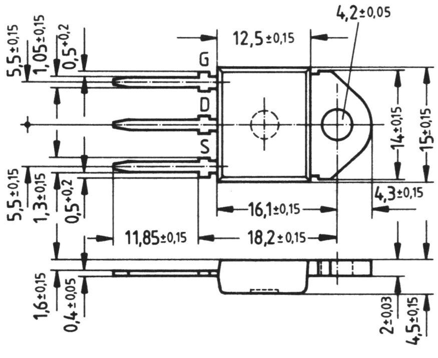

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
5,5±0,15
1,3±0,15
0,5+0,2
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for **TO218AA envelopes.**

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	50	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	50	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	39	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	?	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	155	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	50	65	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 50 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 28 A	–	0,035	0,04	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 28 A	7,0	18,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	1300	2000	pF
C_{rss}	Feedback capacitance		–	500	800	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	110	170	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	250	330	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	39	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	155	A
V_{SD}	Diode forward on-voltage	I_F = 78 A; V_{GS} = 0 V	–	1,6	1,95	V
t_{rr}	Reverse recovery time	I_F = 39 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 30 V	–	150	–	ns
Q_{rr}	Reverse recovery charge		–	1,0	–	μC

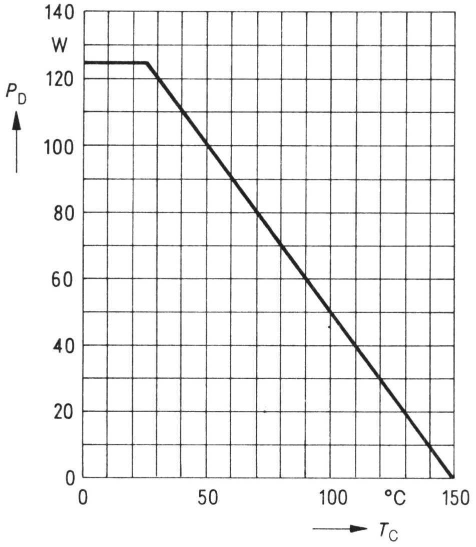


Fig.2 Power dissipation $P_D = f(T_{mb})$.

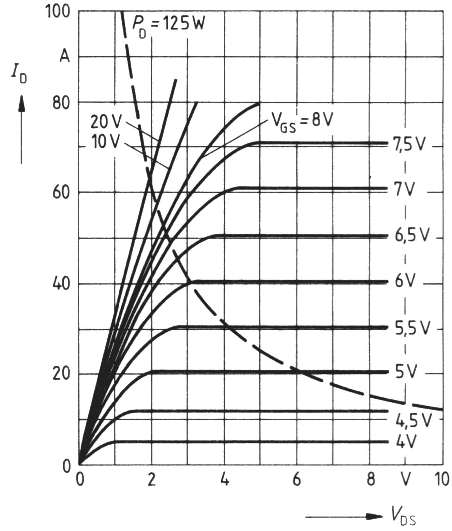


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

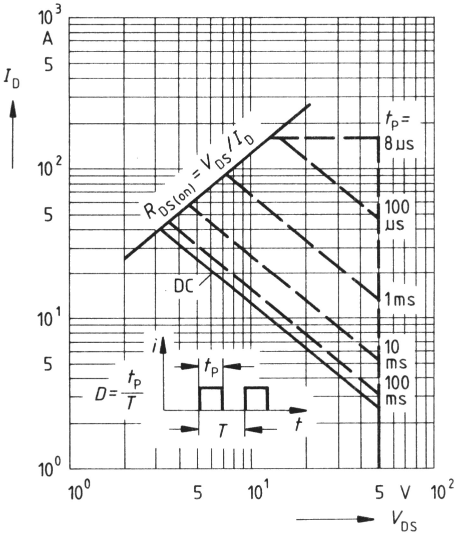


Fig.4 Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

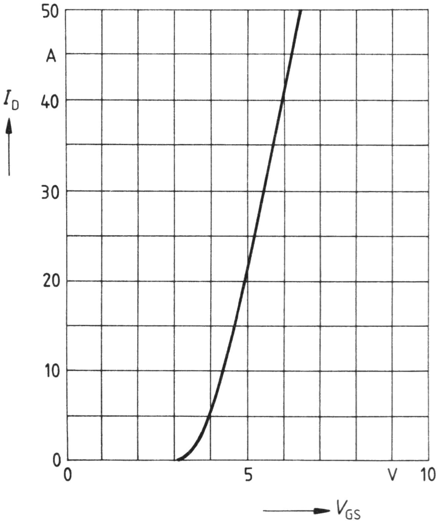


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

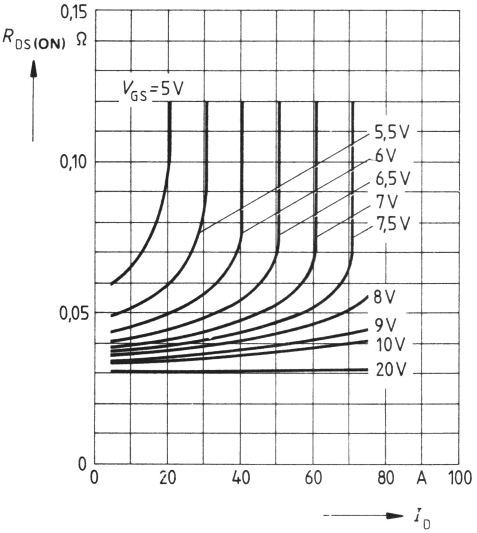


Fig. 6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; T_j = 25 °C.

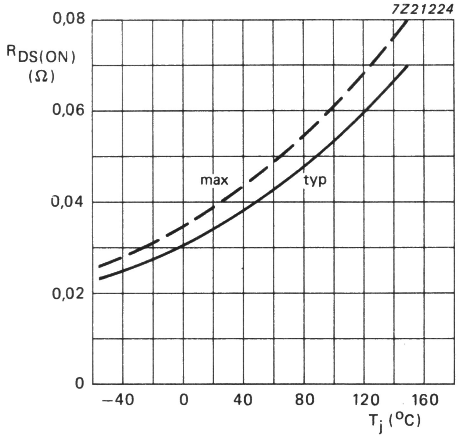


Fig. 7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* I_D = 28 A; V_{GS} = 10 V.

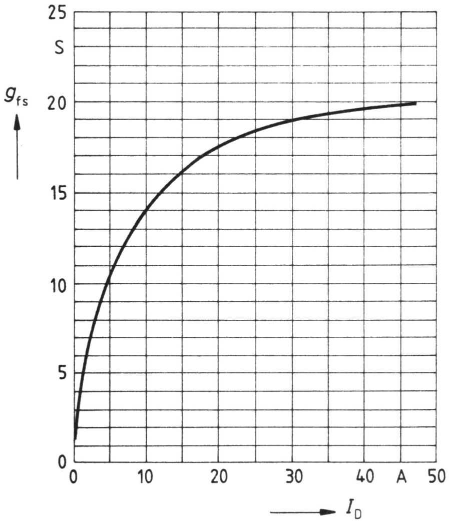


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 µs pulse test;* V_{DS} = 25 V; T_j = 25 °C.

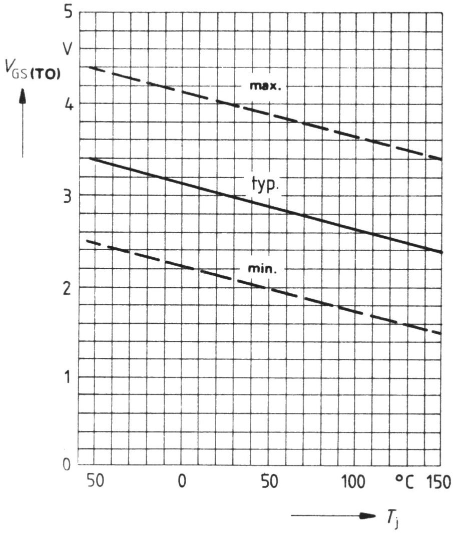


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; I_D = 1 mA.

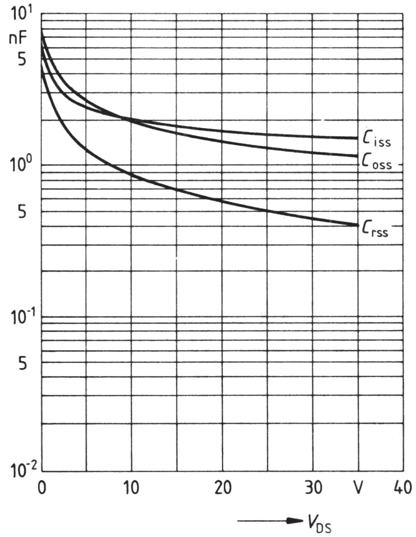


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

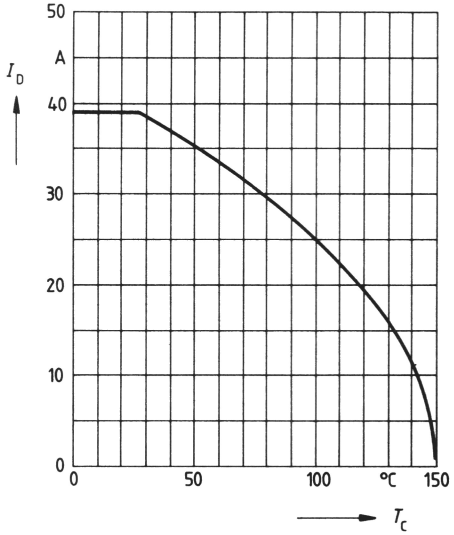


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

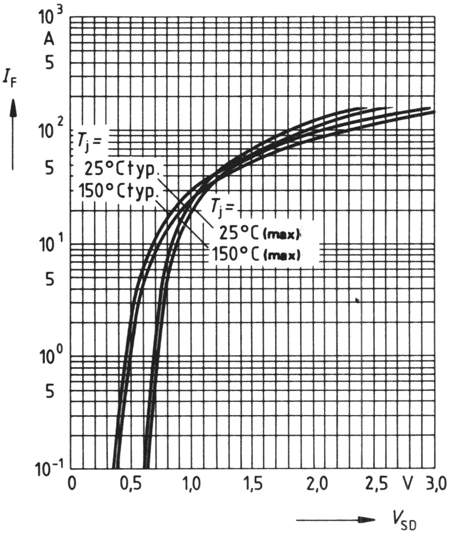


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

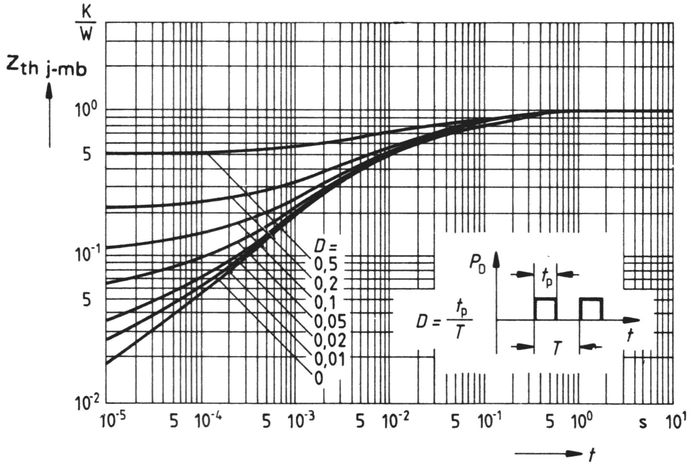


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

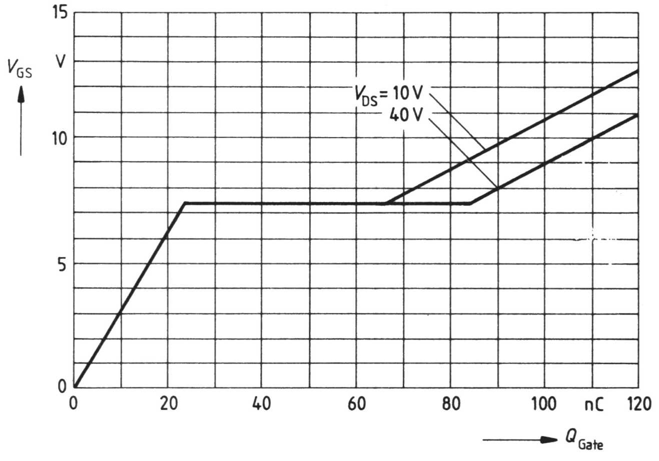


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 67{,}5$ A.

PowerMOS transistor BUZ349

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

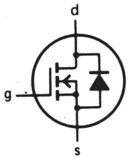
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	100	V
I_D	Drain current (d.c.)	32	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,06	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



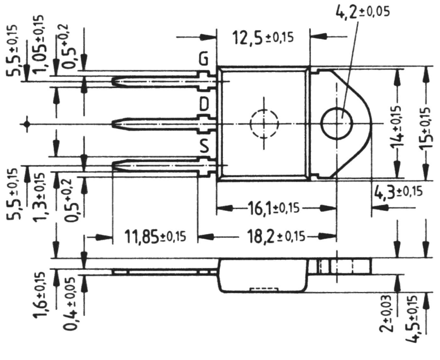

4,2±0,05
12,5±0,15
5,5±0,15
1,05±0,15
0,5+0,2
G
D
S
14±0,15
15±0,15
4,3±0,15
16,1±0,15
5,5±0,15
1,3±0,15
0,5+0,2
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	100	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	100	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	32	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	20	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	125	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	100	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 21 A	–	0,045	0,06	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 21 A	6,0	18,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1500	2000	pF
C_{oss}	Output capacitance		–	800	1200	pF
C_{rss}	Feedback capacitance		–	300	500	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	170	220	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	32	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	125	A
V_{SD}	Diode forward on-voltage	I_F = 64 A; V_{GS} = 0 V	–	1,5	2,0	V
t_{rr}	Reverse recovery time	I_F = 32 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 30 V	–	200	–	ns
Q_{rr}	Reverse recovery charge		–	1,6	–	μC

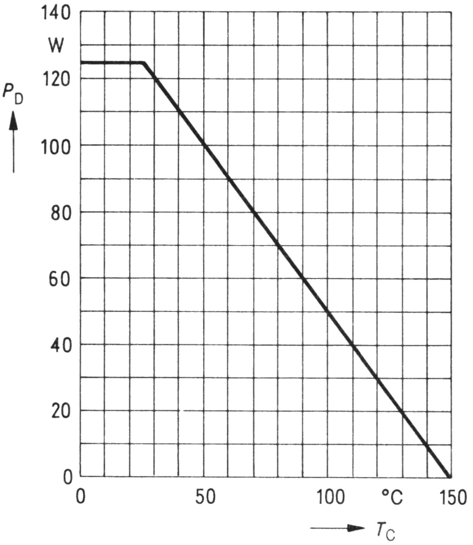


Fig.2 Power dissipation $P_D = f(T_{mb})$.

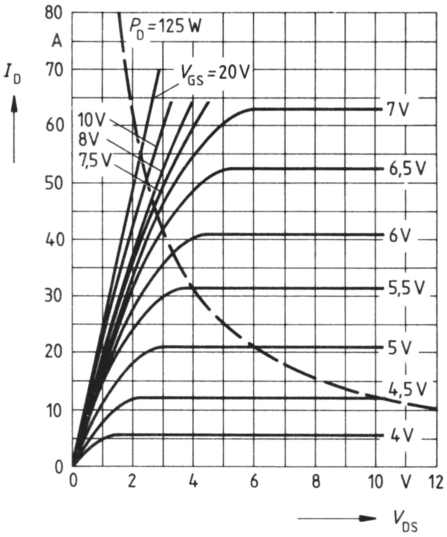


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

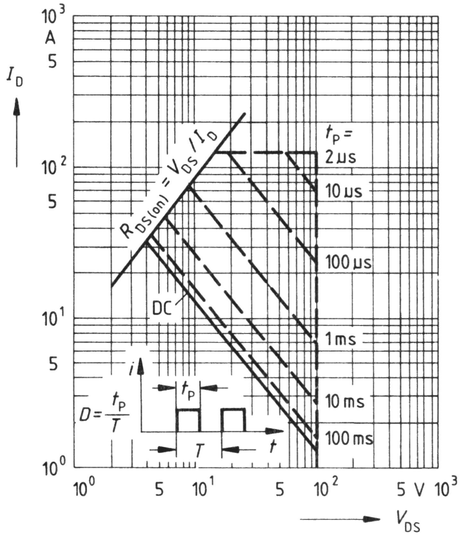


Fig.4 Safe operating area I_D(DC) and $I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

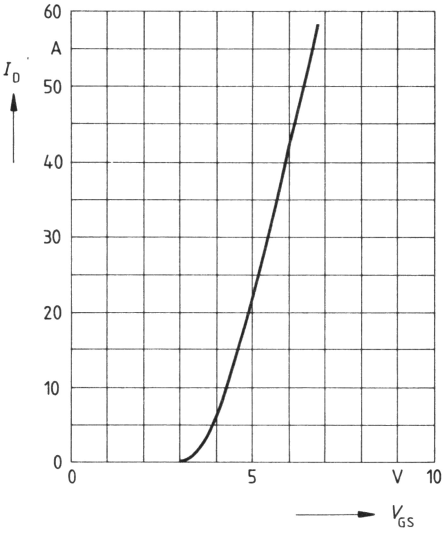


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

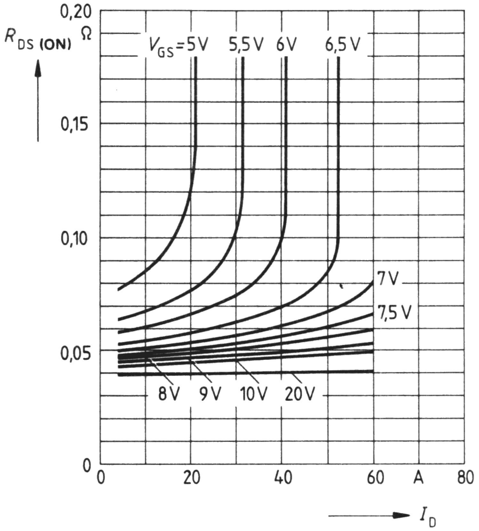


Fig. 6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

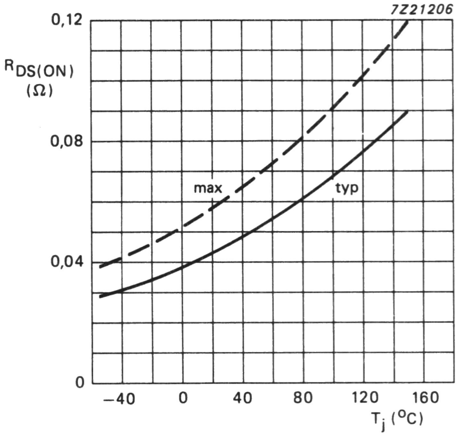


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 21 A; V_{GS} = 10 V.

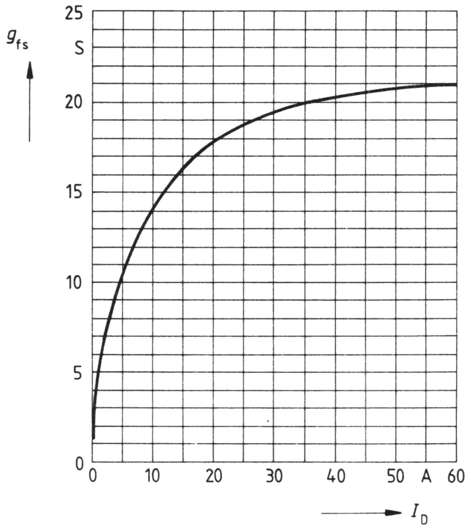


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

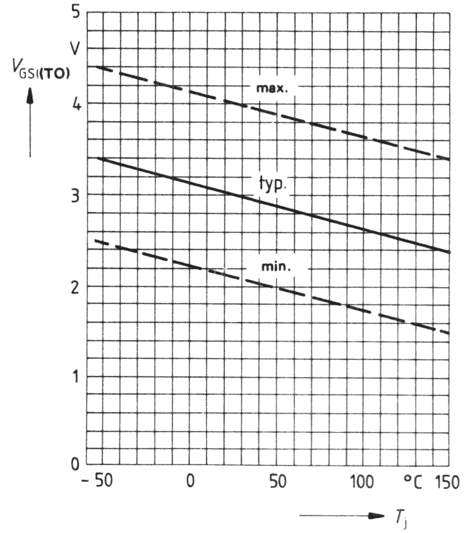


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$
Conditions: V_{DS} = V_{GS}; I_D = 1 mA.

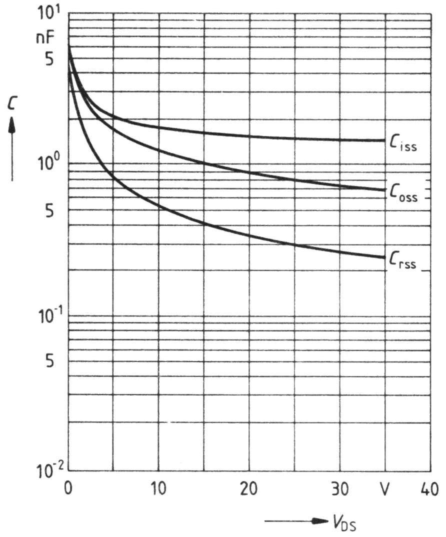


Fig.10 *Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.*

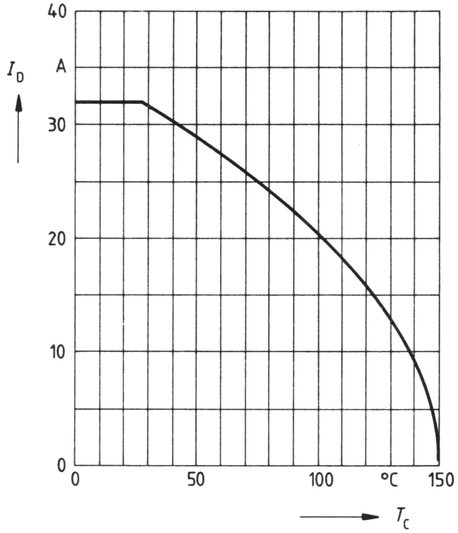


Fig.11 *Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geq 10$ V.*

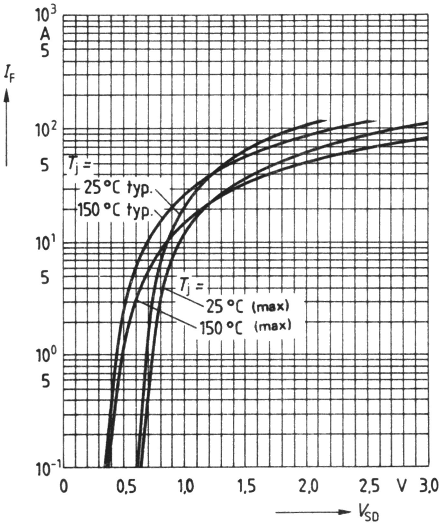


Fig.12 *Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.*

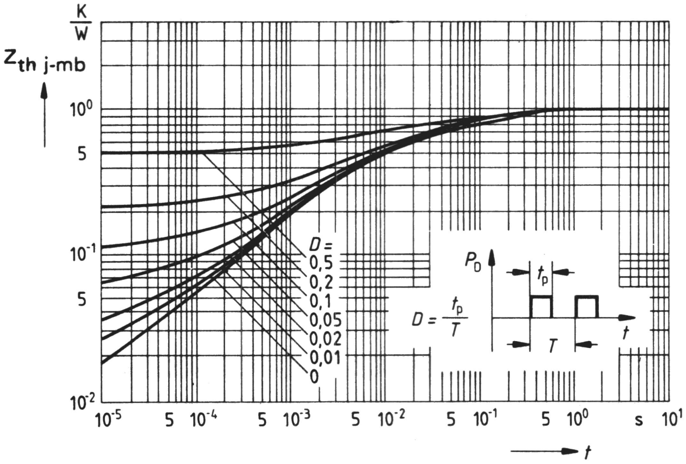


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

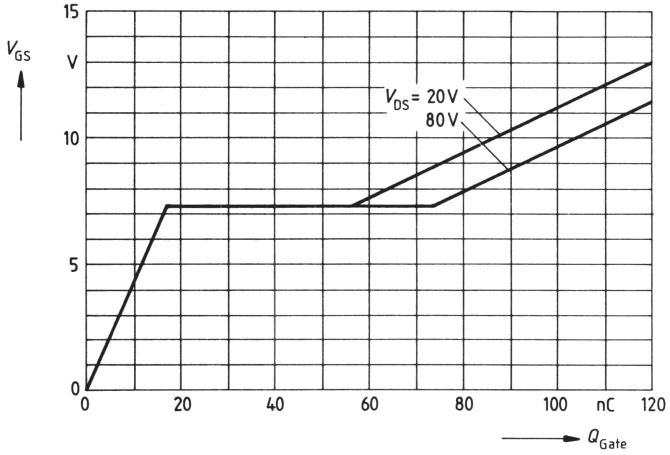


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 48$ A.

PowerMOS transistor BUZ350

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

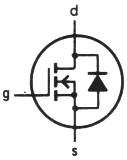
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	200	V
I_D	Drain current (d.c.)	22	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,12	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



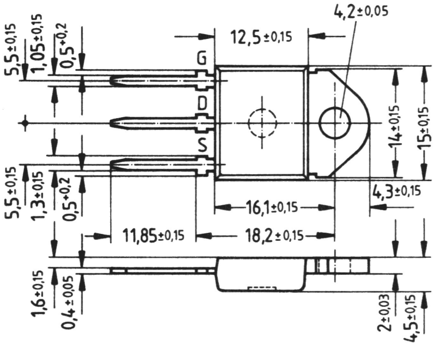

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	200	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\ k\Omega$	–	200	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 35\ °C$	–	22	A
I_D	Drain current (d.c.)	$T_{mb} = 100\ °C$	–	14,5	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\ °C$	–	85	A
P_{tot}	Total power dissipation	$T_{mb} = 25\ °C$	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1,0\ K/W$
From junction to ambient	$R_{th\ j\text{-}a} = 45\ K/W$

STATIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\ V;\ I_D = 0,25\ mA$	200	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS};\ I_D = 1\ mA$	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200\ V;\ V_{GS} = 0\ V;\ T_j = 25\ °C$	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 200\ V;\ V_{GS} = 0\ V;\ T_j = 125\ °C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\ V;\ V_{DS} = 0\ V$	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\ V;\ I_D = 11\ A$	–	0,09	0,12	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\ V;\ I_D = 11\ A$	9,0	13,0	–	S
C_{iss}	Input capacitance	$V_{GS} = 0\ V;\ V_{DS} = 25\ V;\ f = 1\ MHz$	–	1500	2000	pF
C_{oss}	Output capacitance		–	500	800	pF
C_{rss}	Feedback capacitance		–	200	250	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\ V;\ I_D = 3\ A;$ $V_{GS} = 10\ V;\ R_{GS} = 50\ \Omega;$ $R_{gen} = 50\ \Omega$	–	30	45	ns
t_r	Turn-on rise time		–	70	110	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	120	160	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	22	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	85	A
V_{SD}	Diode forward on-voltage	I_F = 44 A; V_{GS} = 0 V	–	1,2	1,7	V
t_{rr}	Reverse recovery time	I_F = 22 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	400	–	ns
Q_{rr}	Reverse recovery charge		–	6,0	–	μC

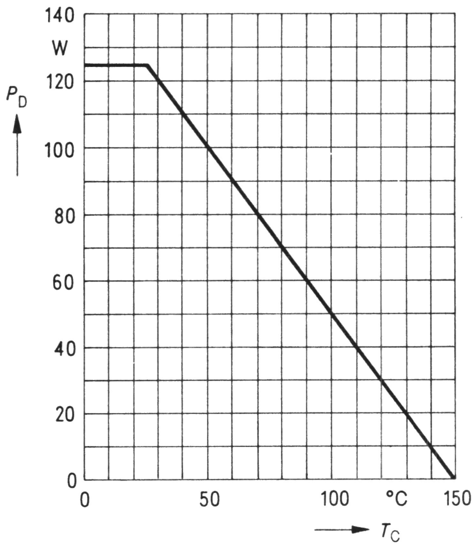


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

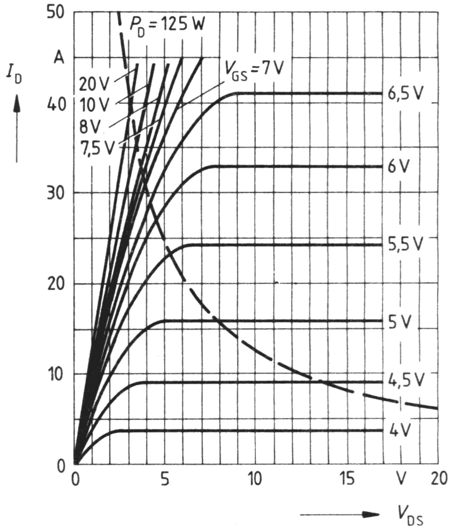


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

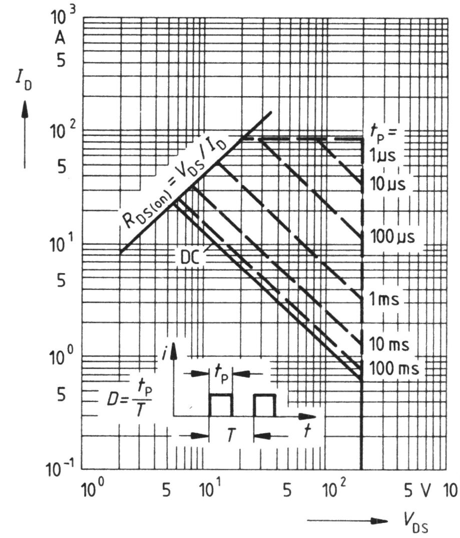


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

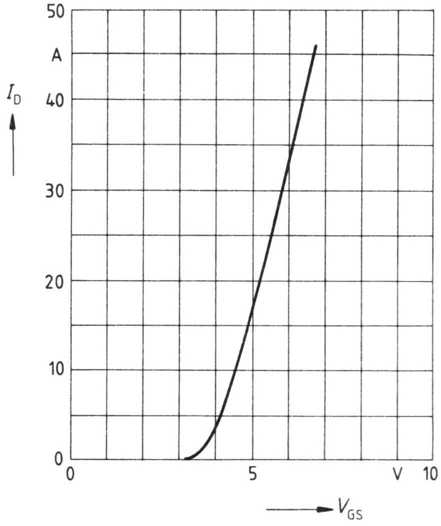


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

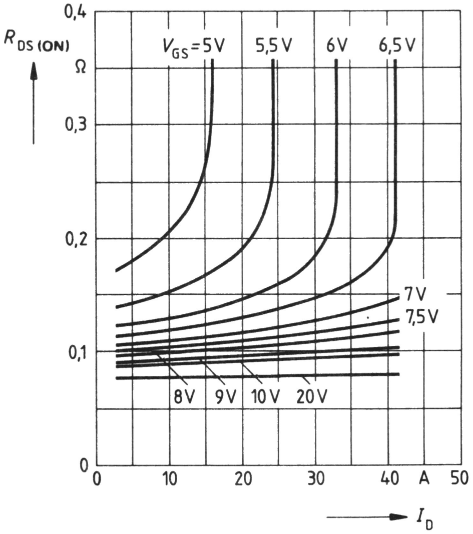


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

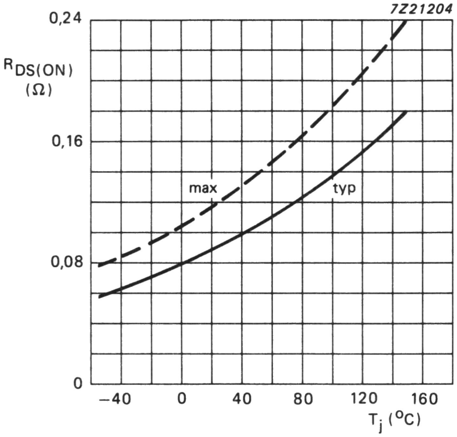


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 11 A; V_{GS} = 10 V.

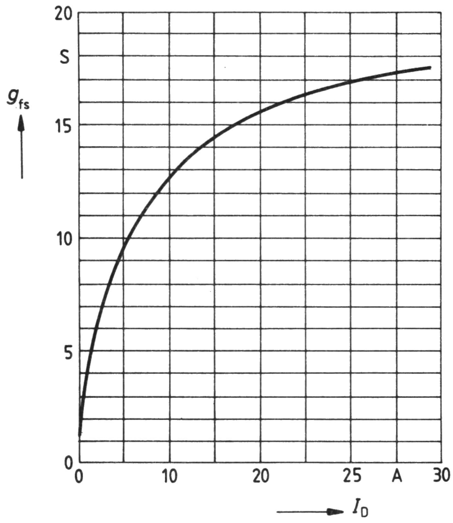


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

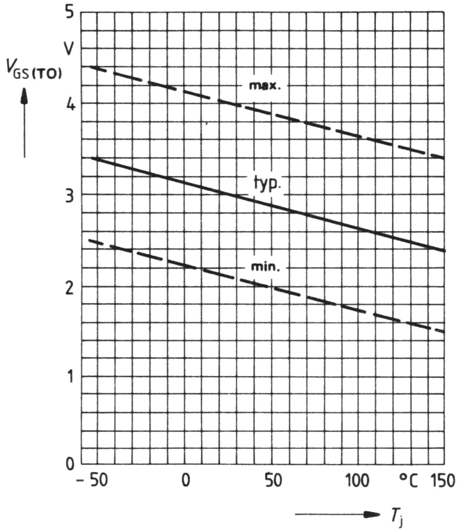


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

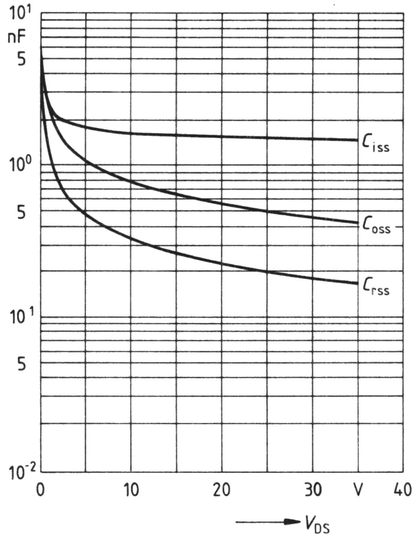


Fig.10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

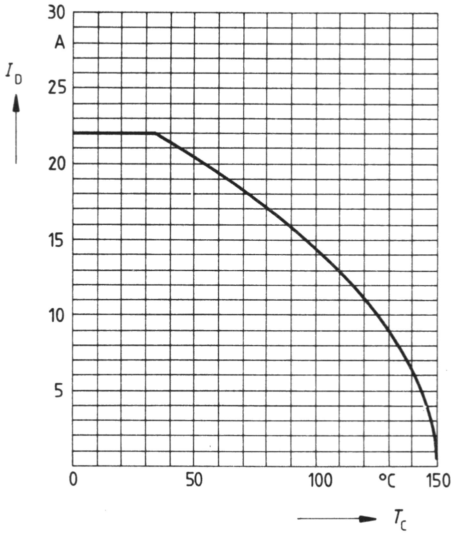


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

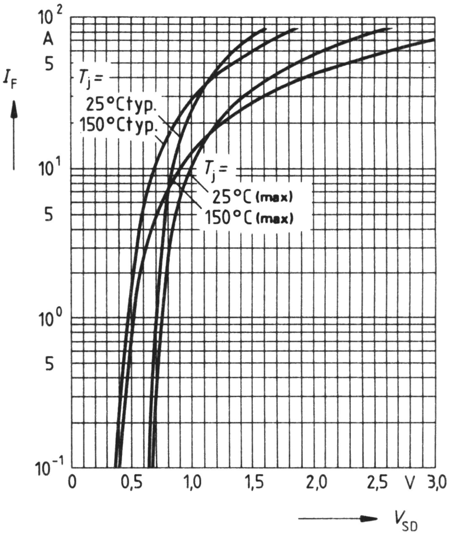


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ *µs.*

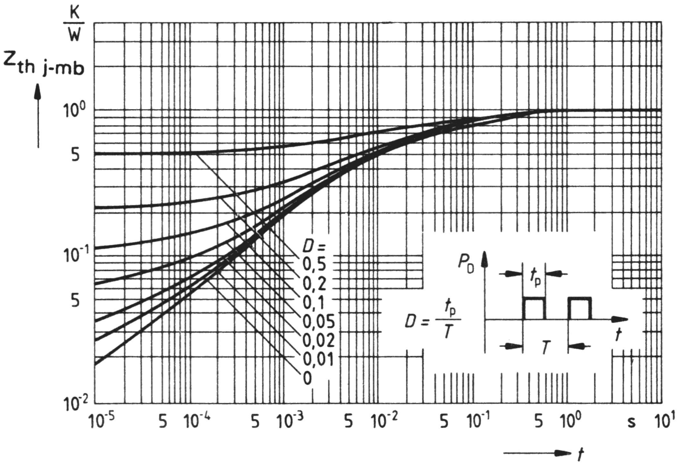


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

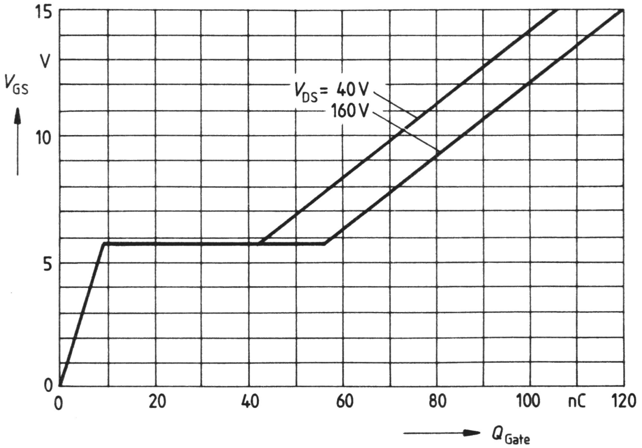


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 33$ A.

PowerMOS transistor BUZ326

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

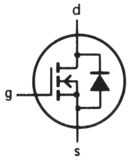
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	10,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



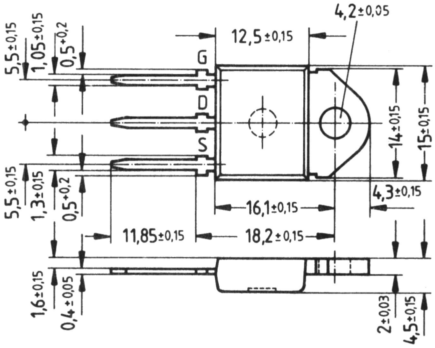

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\ k\Omega$	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 25\ °C$	–	10,5	A
I_D	Drain current (d.c.)	$T_{mb} = 100\ °C$	–	6,6	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\ °C$	–	42	A
P_{tot}	Total power dissipation	$T_{mb} = 25\ °C$	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1{,}0\ K/W$
From junction to ambient	$R_{th\ j\text{-}a} = 45\ K/W$

STATIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\ V$; $I_D = 0{,}25\ mA$	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\ mA$	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 400\ V$; $V_{GS} = 0\ V$; $T_j = 25\ °C$	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 400\ V$; $V_{GS} = 0\ V$; $T_j = 125\ °C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\ V$; $V_{DS} = 0\ V$	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 6\ A$	–	0,4	0,5	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\ V$; $I_D = 6\ A$	5,0	8,0	–	S
C_{iss}	Input capacitance	$V_{GS} = 0\ V$; $V_{DS} = 25\ V$; $f = 1\ MHz$	–	1350	1750	pF
C_{oss}	Output capacitance		–	200	320	pF
C_{rss}	Feedback capacitance		–	90	150	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\ V$; $I_D = 2{,}9\ A$; $V_{GS} = 10\ V$; $R_{GS} = 50\ \Omega$; $R_{gen} = 50\ \Omega$	–	25	40	ns
t_r	Turn-on rise time		–	45	70	ns
$t_{d\ off}$	Turn-off delay time		–	250	310	ns
t_f	Turn-off fall time		–	75	90	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	10,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	42	A
V_{SD}	Diode forward on-voltage	I_F = 21 A; V_{GS} = 0 V	–	1,0	1,5	V
t_{rr}	Reverse recovery time	I_F = 10,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	–	–	ns
Q_{rr}	Reverse recovery charge		–	–	–	µC

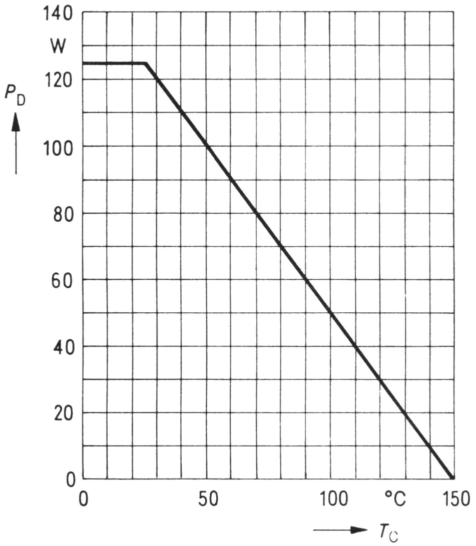


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

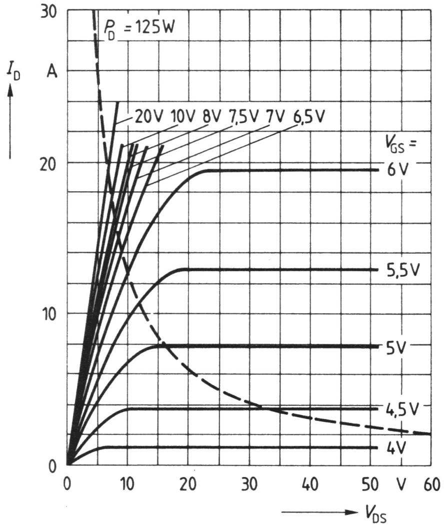


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

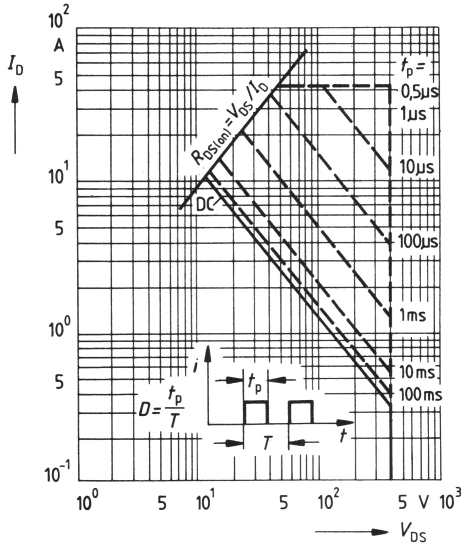


Fig. 4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

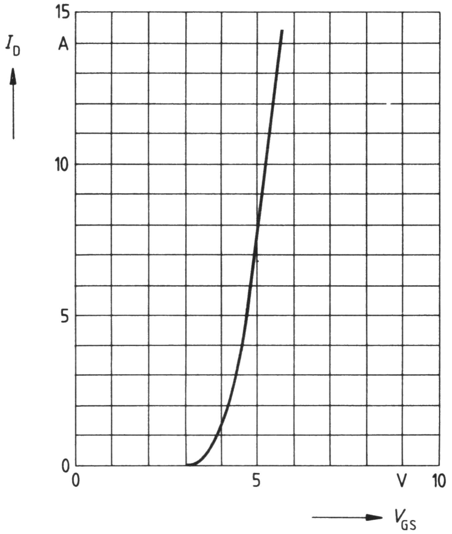


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

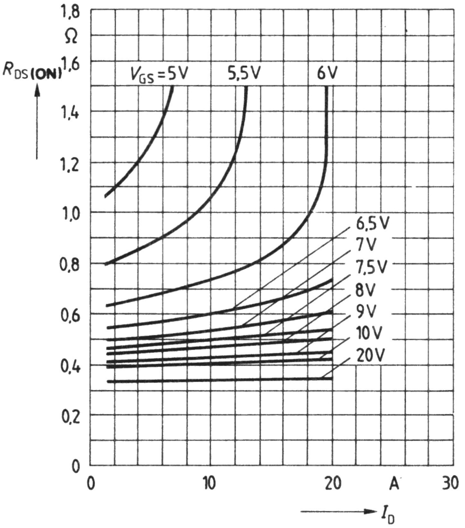


Fig. 6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; $T_j = 25$ °C.*

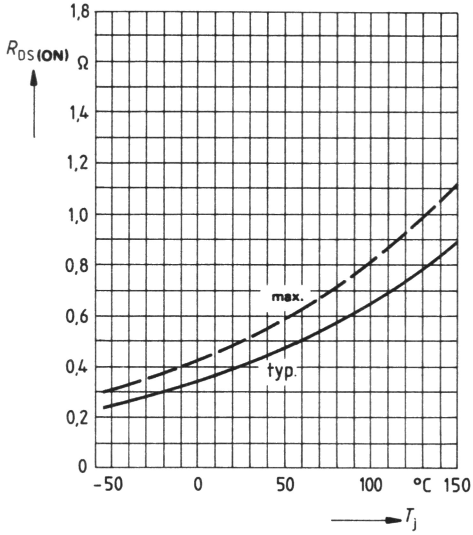


Fig. 7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: $I_D = 6$ A; $V_{GS} = 10$ V.*

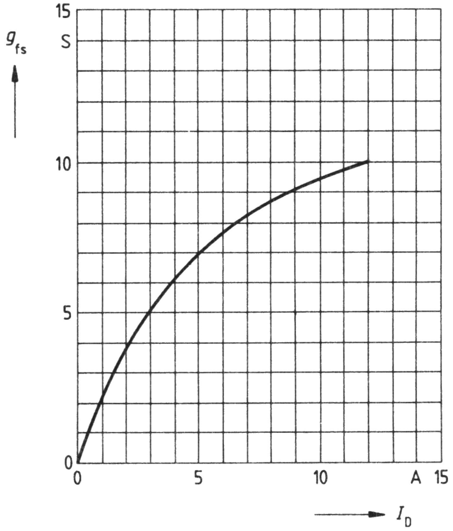


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 µs pulse test; $V_{DS} = 25$ V; $T_j = 25$ °C.*

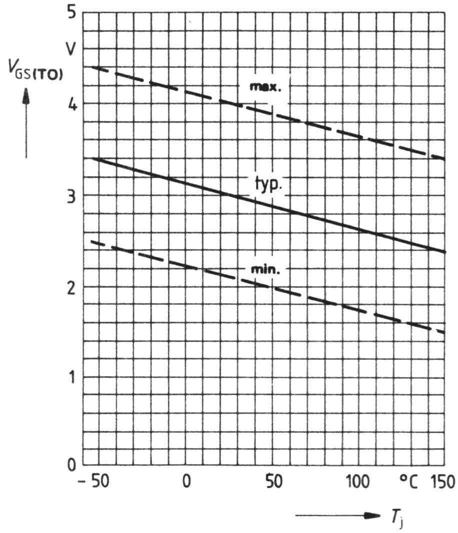


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.*

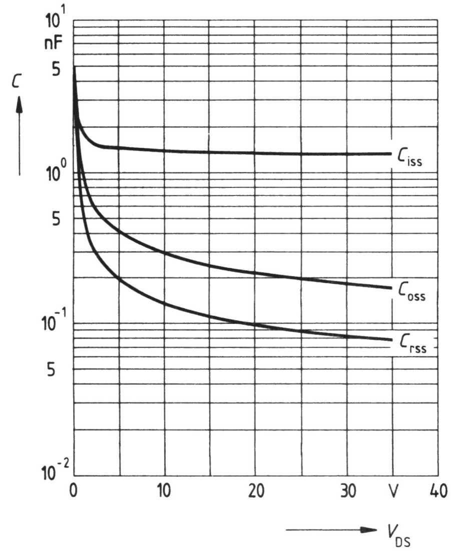


Fig.10 *Typical capacitances* $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ *MHz.*

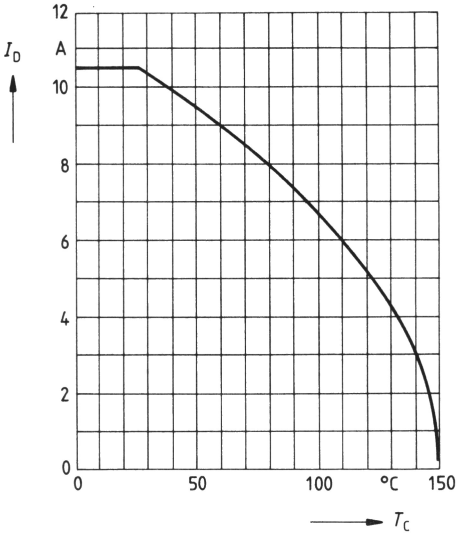


Fig.11 *Continuous drain current* $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ *V.*

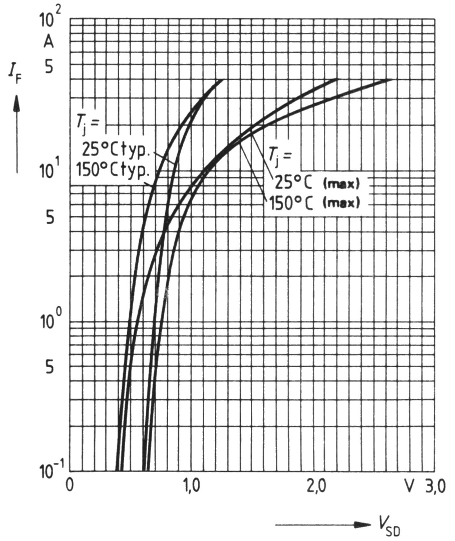


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80\ \mu s$.

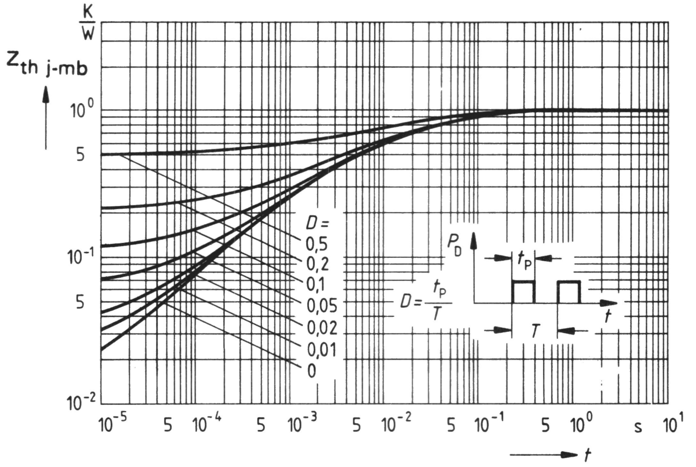


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

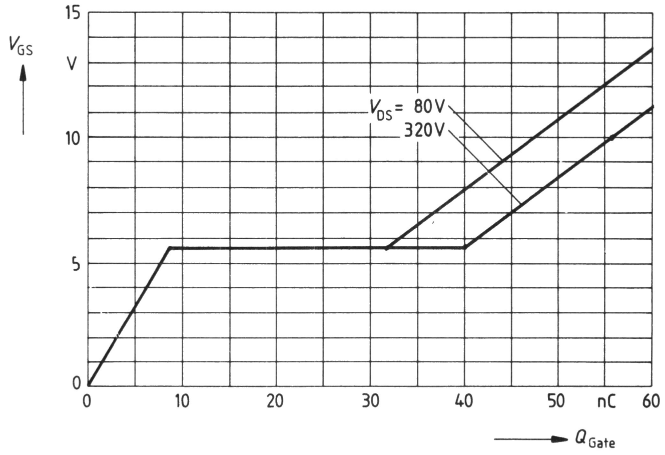


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 14{,}3$ A.

PowerMOS transistor BUZ351

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

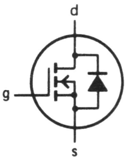
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	400	V
I_D	Drain current (d.c.)	11,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,4	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



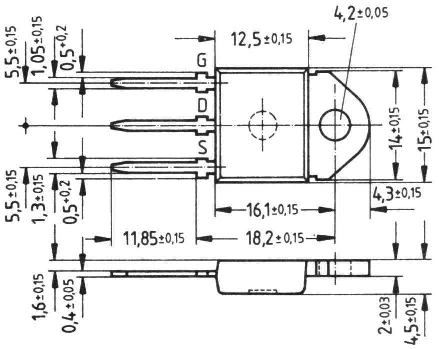

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
18,2±0,15
11,85±0,15
5,5±0,15
1,3±0,15
0,5+0,2
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	400	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	400	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	11,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	7,4	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	46	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	400	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 400 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 5,5 A	–	0,35	0,4	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 5,5 A	3,3	4,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	300	500	pF
C_{rss}	Feedback capacitance		–	120	200	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,9 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	11,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	46	A
V_{SD}	Diode forward on-voltage	I_F = 23 A; V_{GS} = 0 V	–	1,3	1,7	V
t_{rr}	Reverse recovery time	I_F = 11,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1,0	–	µs
Q_{rr}	Reverse recovery charge		–	10	–	µC

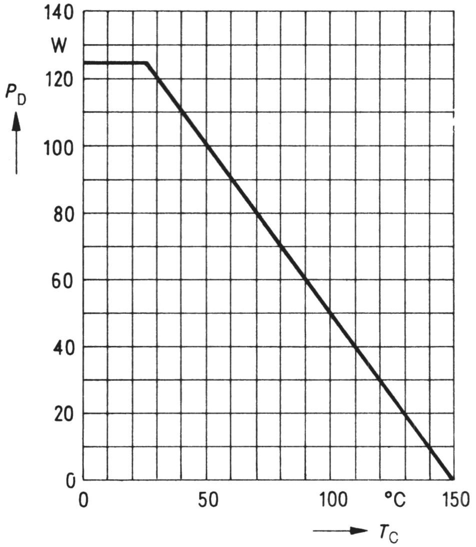


Fig. 2 Power dissipation $P_D = f(T_{mb})$.

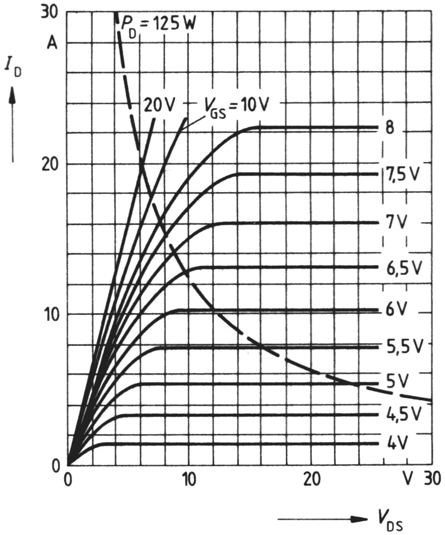


Fig. 3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 μs pulse test;
$T_{mb} = 25$ °C.

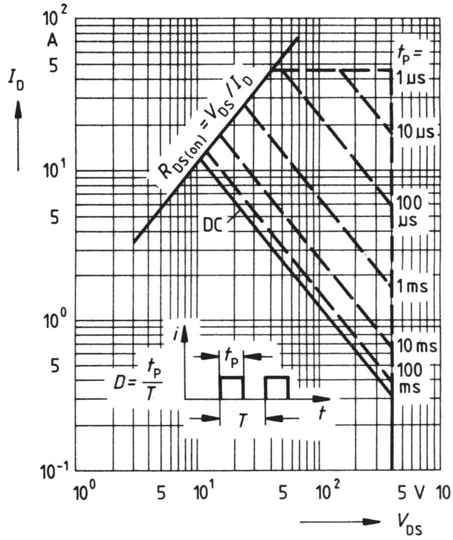


Fig. 4 Safe operating area I_D(DC) and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

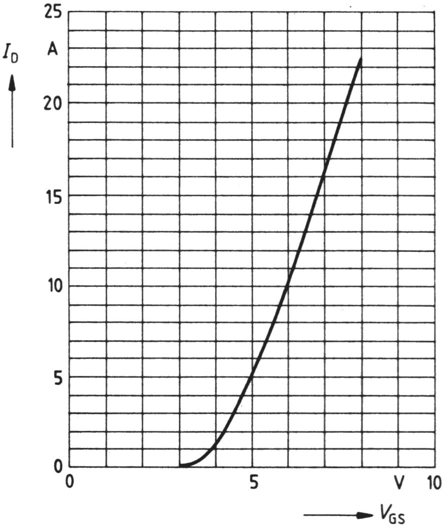


Fig. 5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 μs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

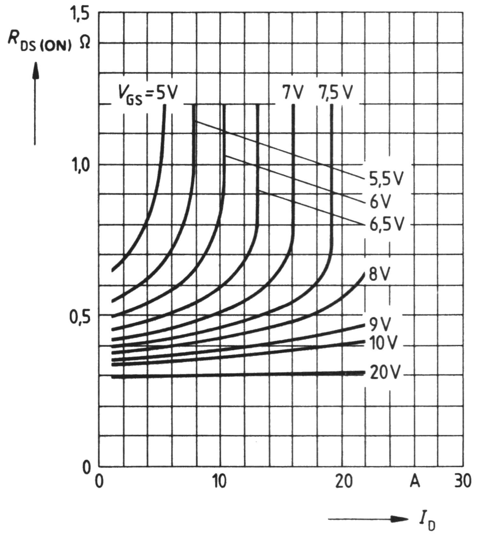


Fig.6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$*
Parameter: V_{GS}; T_j = 25 °C.

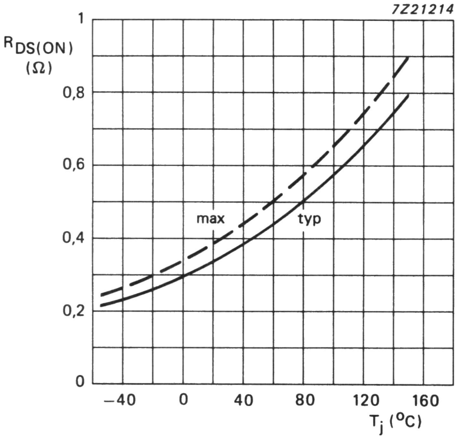


Fig.7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$*
Conditions: I_D = 5,5 A; V_{GS} = 10 V.

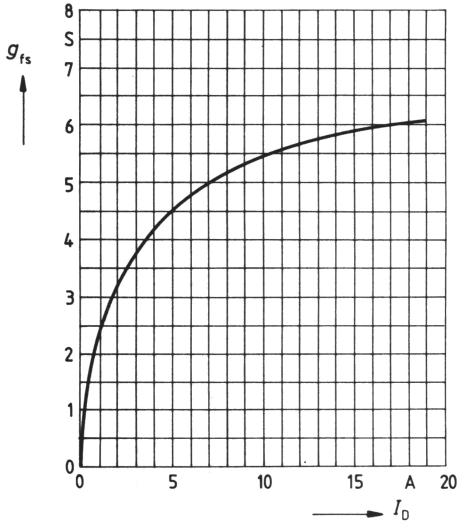


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

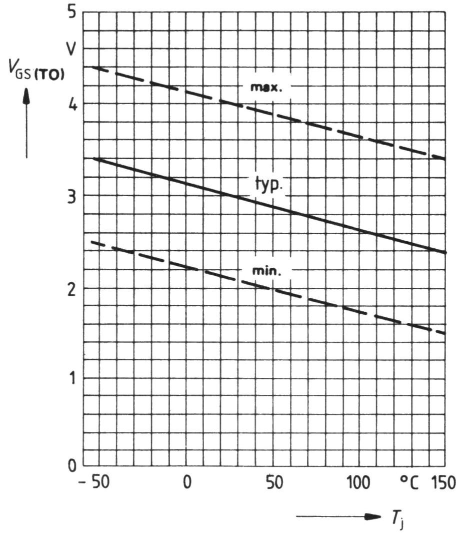


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

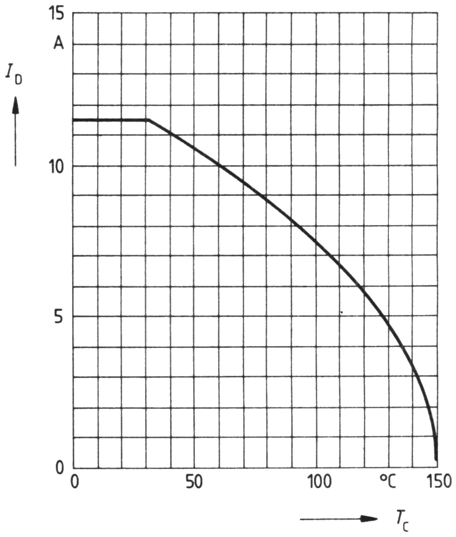


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

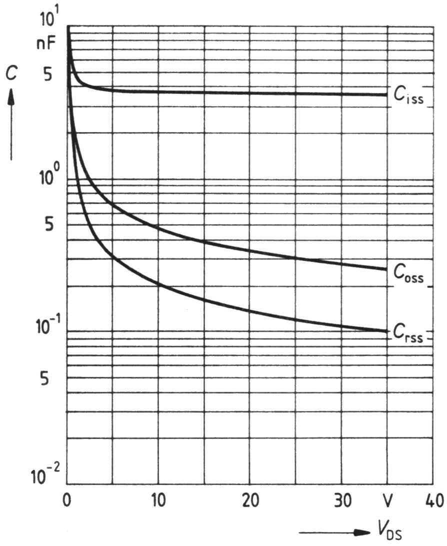


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

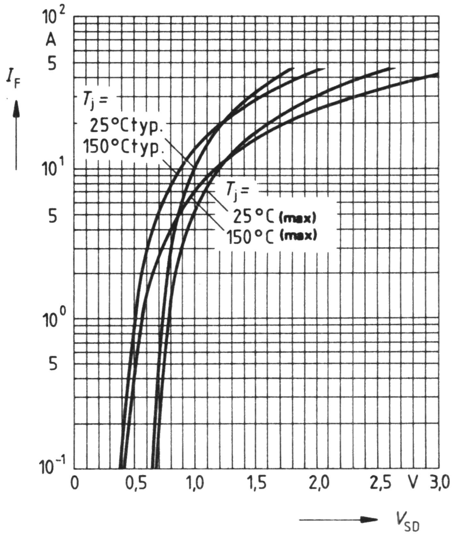


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

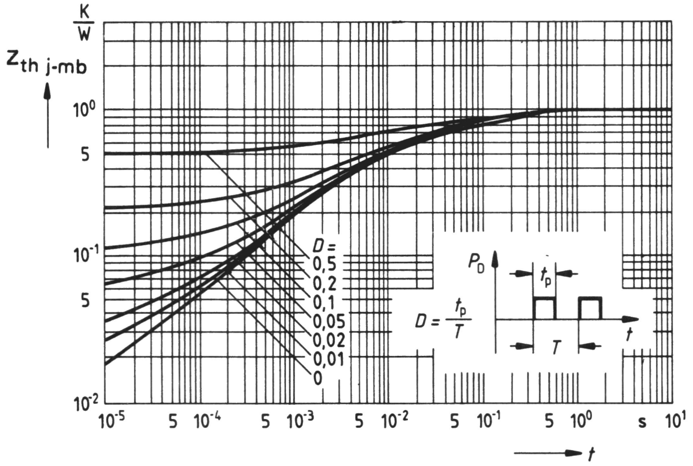


Fig.13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

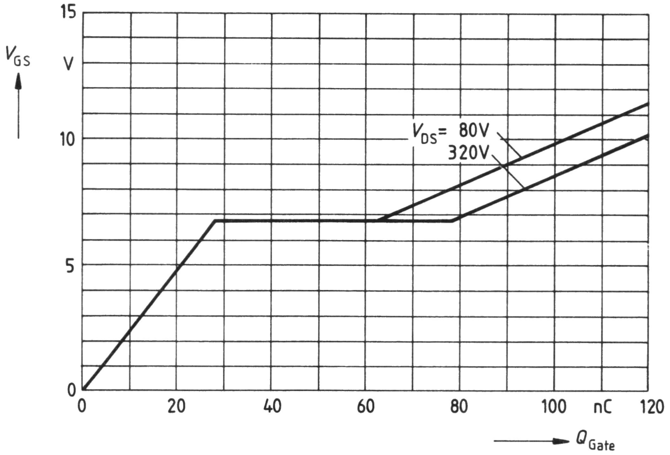


Fig.14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 17{,}3$ A.

PowerMOS transistor BUZ330

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

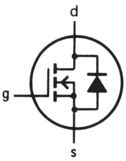
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	9,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,6	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



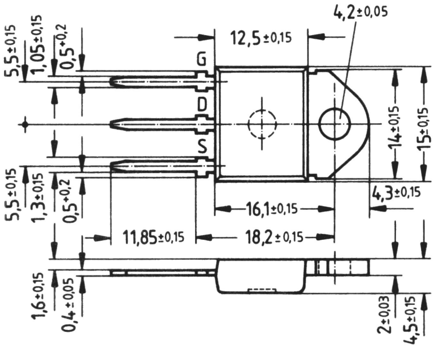

4,2±0,05
12,5±0,15
5,5±0,15
1,05±0,15
0,5+0,2
G
D
S
14±0,15
15±0,15
5,5±0,15
1,3±0,15
0,5+0,2
16,1±0,15
4,3±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	9,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	38	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6 A	–	0,5	0,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6 A	5,0	8,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1350	1800	pF
C_{oss}	Output capacitance		–	180	270	pF
C_{rss}	Feedback capacitance		–	80	120	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	45	70	ns
$t_{d\ off}$	Turn-off delay time		–	250	310	ns
t_f	Turn-off fall time		–	75	90	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	9,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	38	A
V_{SD}	Diode forward on-voltage	I_F = 19 A; V_{GS} = 0 V; T_j = 25 °C	–	1,0	1,4	V
t_{rr}	Reverse recovery time	I_F = 9,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	–	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	–	–	µC

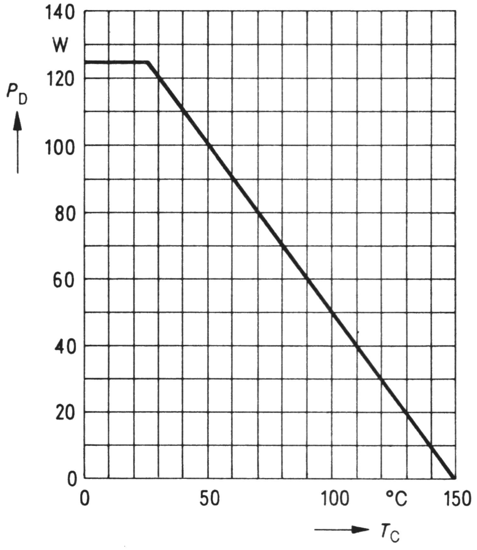


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

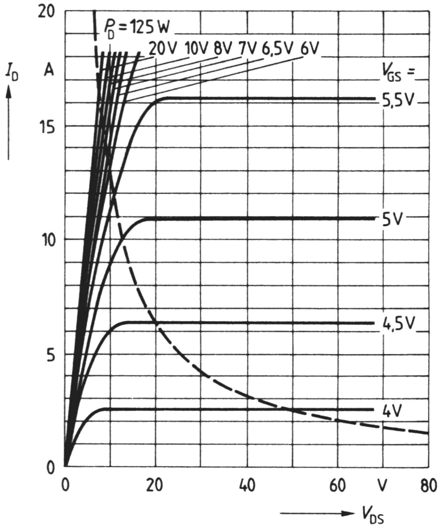


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

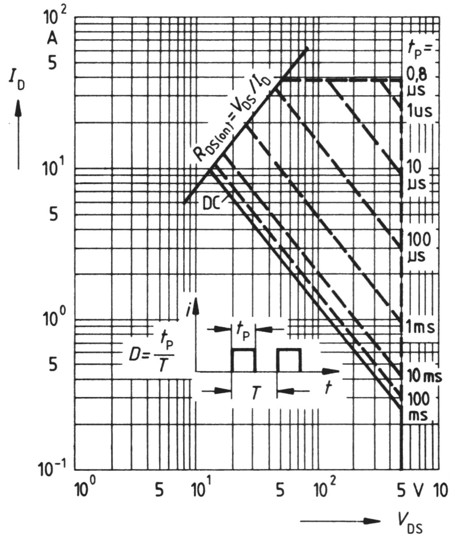


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

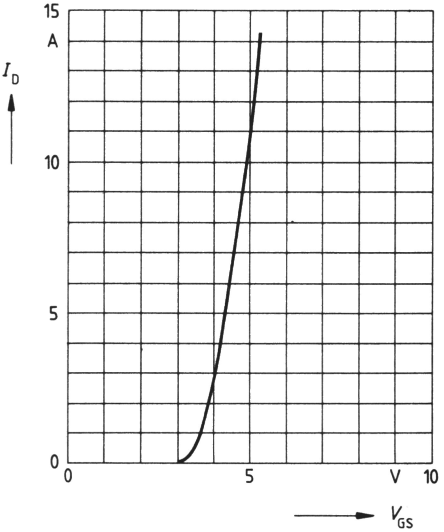


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

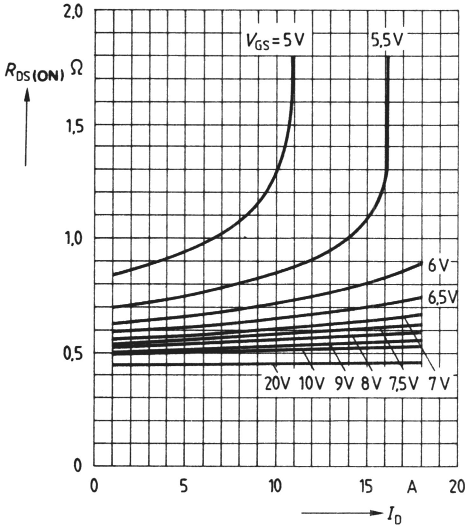


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

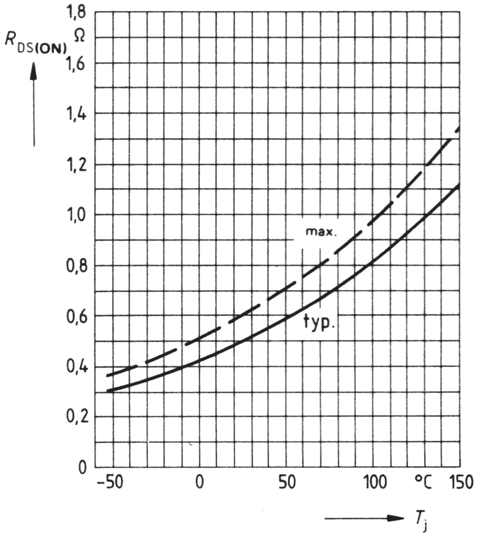


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 6,0 A; V_{GS} = 10 V.

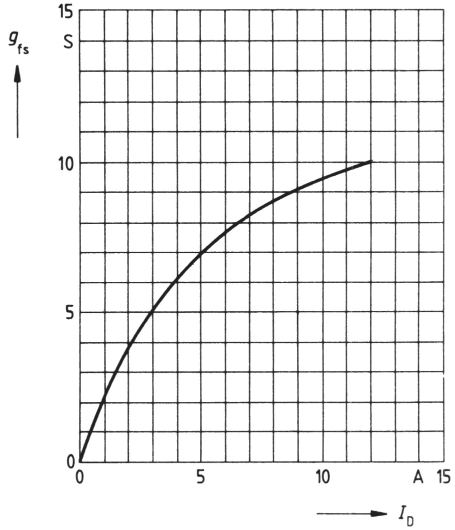


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

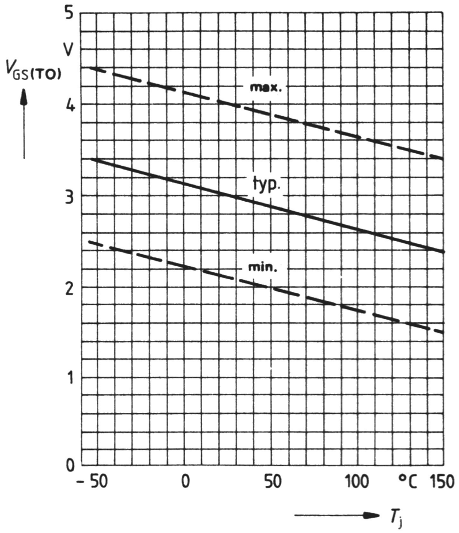


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

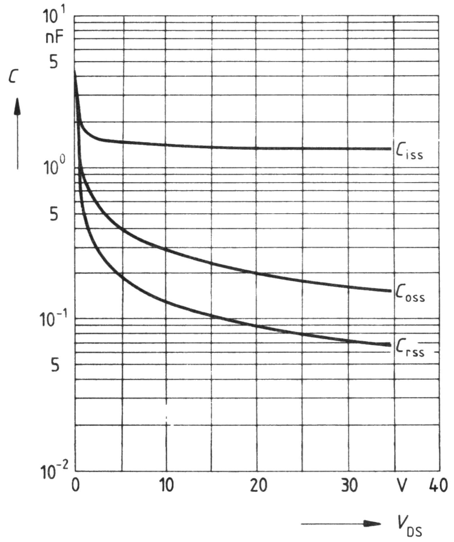


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

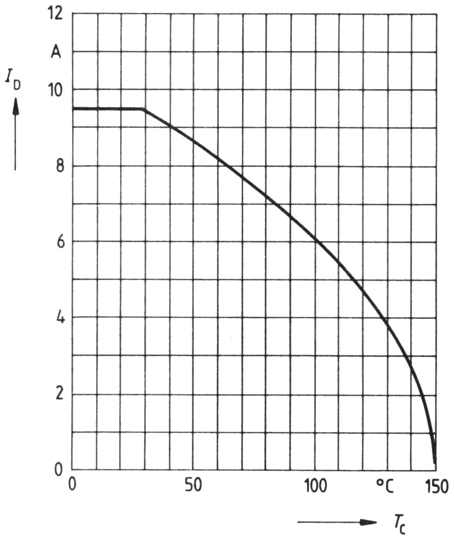


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

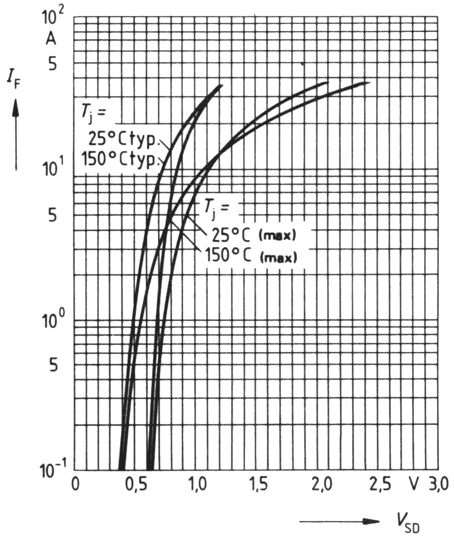


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

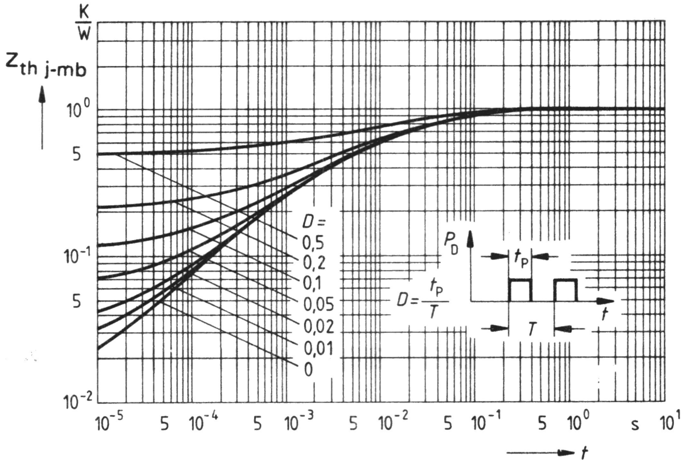


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

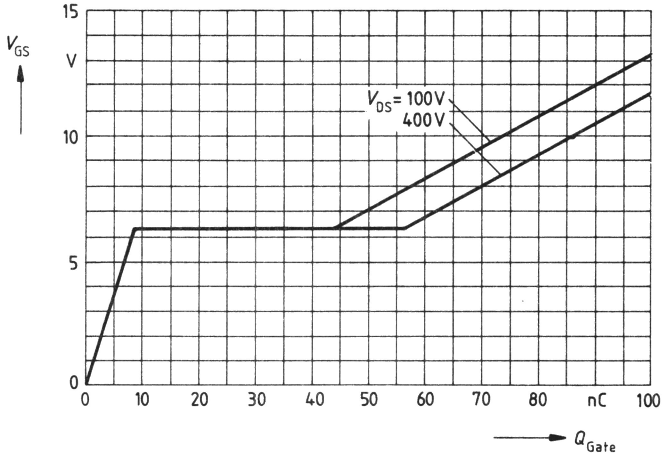


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 12,8 A.

PowerMOS transistor BUZ331

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

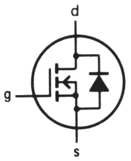
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	8,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,8	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



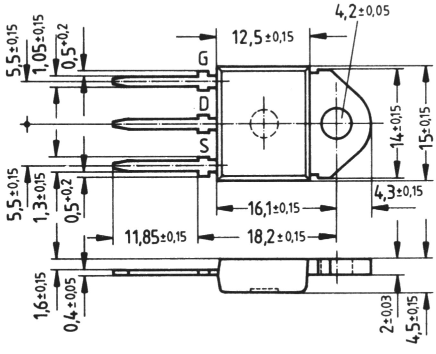

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
5,5±0,15
1,3±0,15
0,5+0,2
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	8,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	5,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	32	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6 A	–	0,7	0,8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6 A	5,0	8,0	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1350	1800	pF
C_{oss}	Output capacitance		–	180	270	pF
C_{rss}	Feedback capacitance		–	80	120	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	25	40	ns
t_r	Turn-on rise time		–	45	70	ns
$t_{d\ off}$	Turn-off delay time		–	250	310	ns
t_f	Turn-off fall time		–	75	90	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	8,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	32	A
V_{SD}	Diode forward on-voltage	I_F = 16 A; V_{GS} = 0 V; T_j = 25 °C	–	1,0	1,4	V
t_{rr}	Reverse recovery time	I_F = 8 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	–	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	–	–	µC

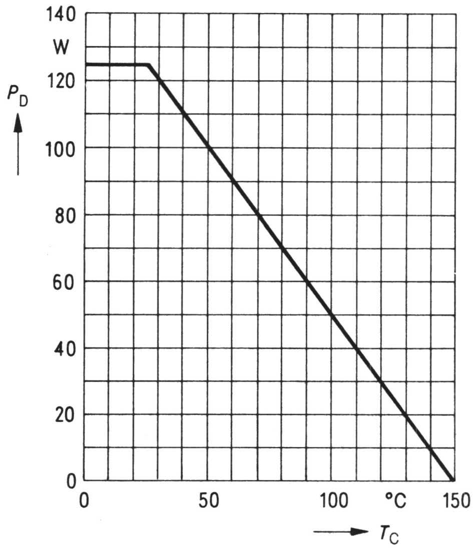


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

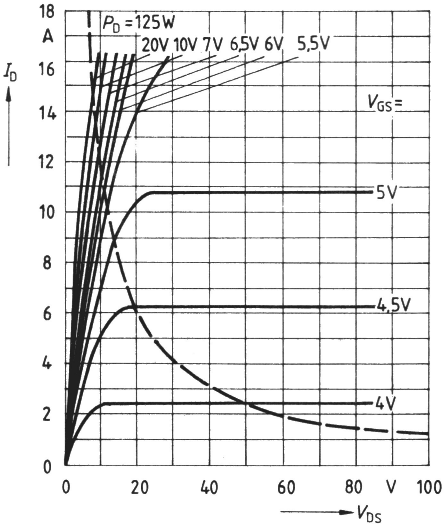


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

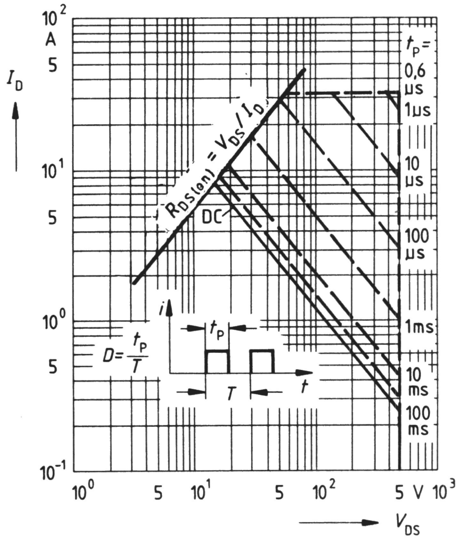


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

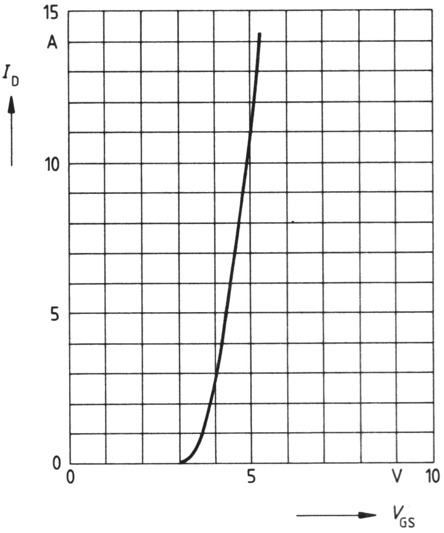


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

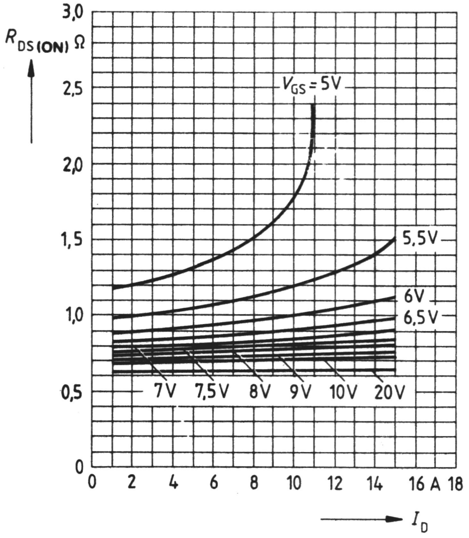


Fig. 6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; T_j *= 25 °C.*

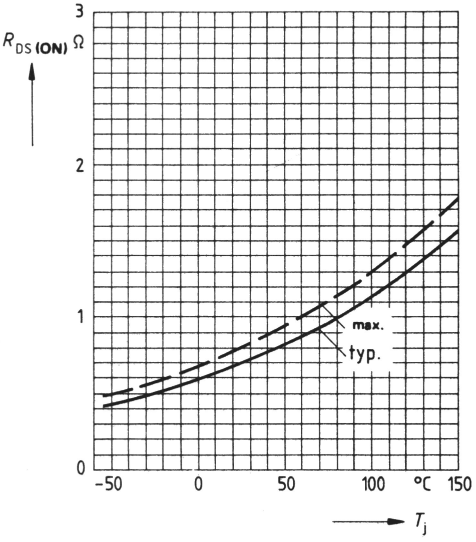


Fig. 7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* I_D *= 6,0 A;* V_{GS} *= 10 V.*

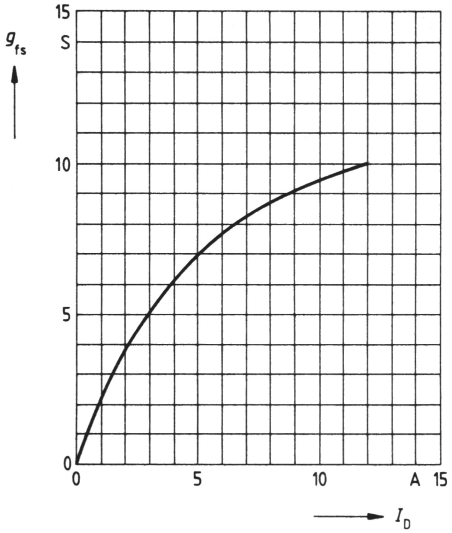


Fig. 8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 μs pulse test;* V_{DS} *= 25 V;* T_j *= 25 °C.*

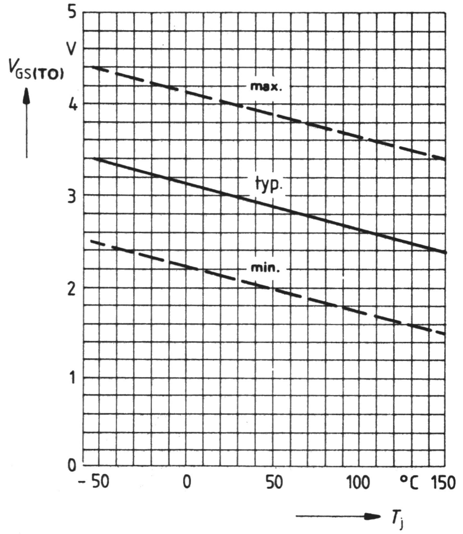


Fig. 9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; I_D *= 1 mA.*

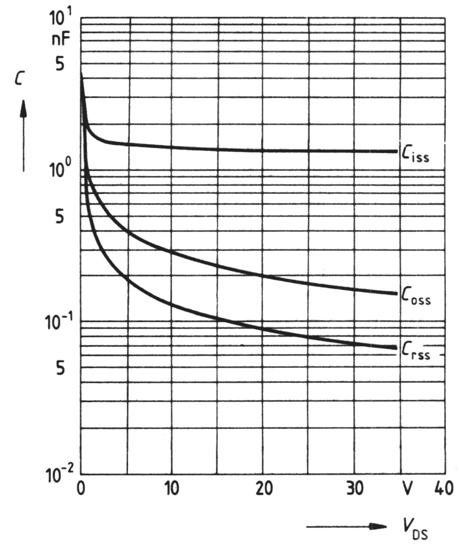


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

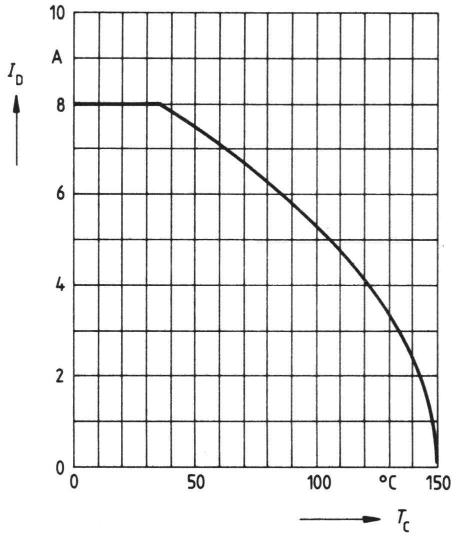


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

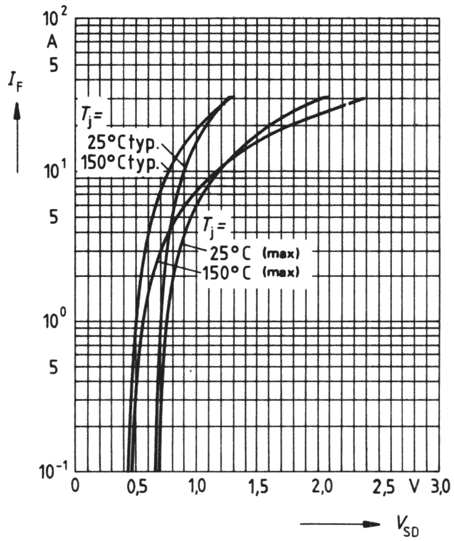


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

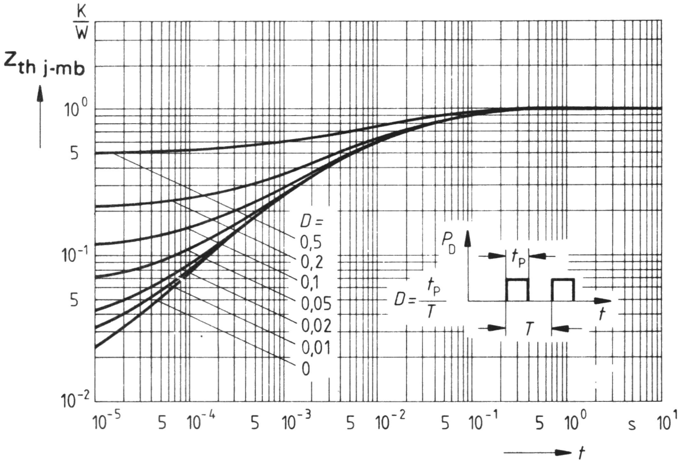


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

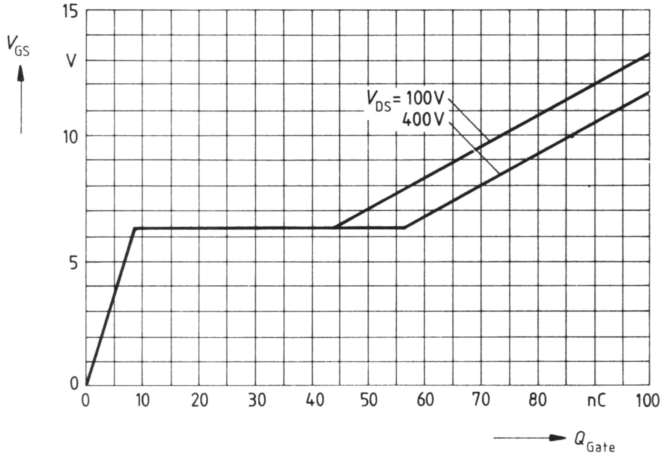


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 12,8 A.

PowerMOS transistor BUZ384

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

FREDFET* with fast-recovery reverse diode. This device is particularly suitable for motor control applications, e.g. in full-bridge configurations for which faster recovery characteristics simplify design for inductive loads.

QUICK REFERENCE DATA

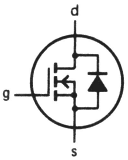
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	10,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,6	Ω

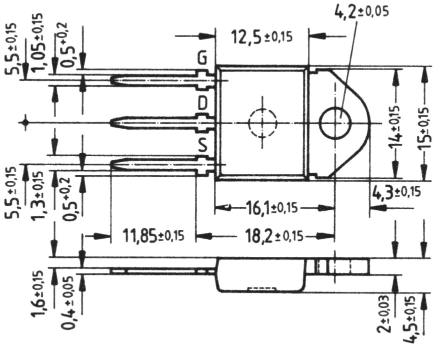
* Fast Recovery Epitaxial Diode FET.

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g





4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
5,5±0,15
1,3±0,15
0,5+0,2
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	10,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	6,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	42	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6,6 A	–	0,55	0,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6,6 A	2,7	5,4	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	10,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	42	A
V_{SD}	Diode forward on-voltage	I_F = 21 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	1,9	V
t_{rr}	Reverse recovery time	I_F = 10,5 A; T_j = 25 °C	–	180	250	ns
		$-dI_F/dt$ = T_j = 150 °C	–	220	300	ns
Q_{rr}	Reverse recovery charge	100 A/µs; T_j = 25 °C	–	0,65	1,2	µC
		V_{GS} = 0 V; T_j = 150 °C	–	2,6	5,0	µC
I_{rrm}	Reverse recovery current	V_R = 100 V T_j = 150 °C	–	15	–	A

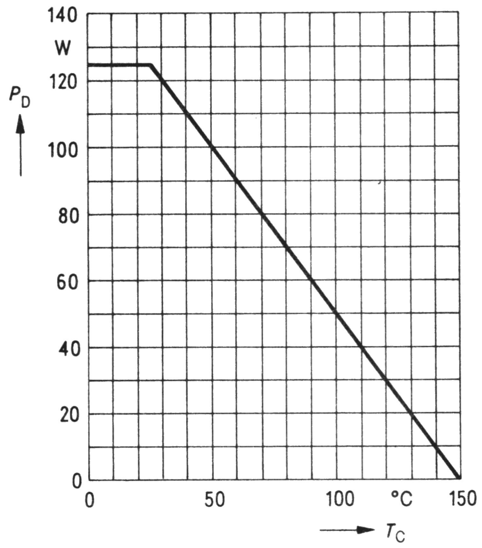


Fig.2 *Power dissipation* $P_D = f(T_{mb})$.

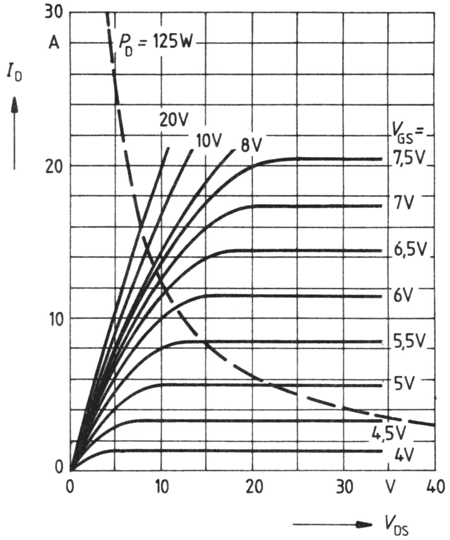


Fig.3 *Typical output characteristics* $I_D = f(V_{DS})$ *Parameter:* V_{GS}*; 80 µs pulse test;* T_{mb} *= 25 °C.*

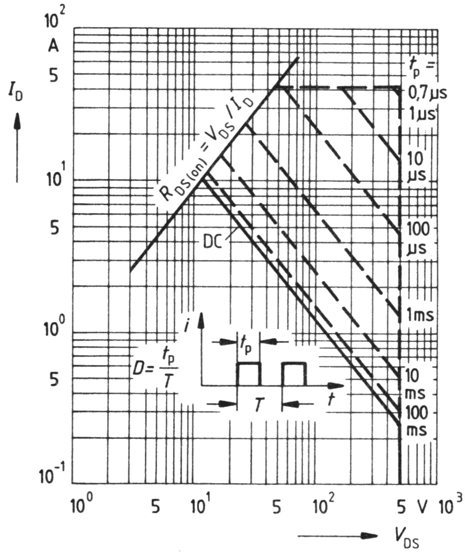


Fig.4 *Safe operating area* $I_D(DC)$ *and* $I_{DM} = f(V_{DS})$ *Parameter:* t_p*;* $D = 0{,}01$*;* T_{mb} *= 25 °C.*

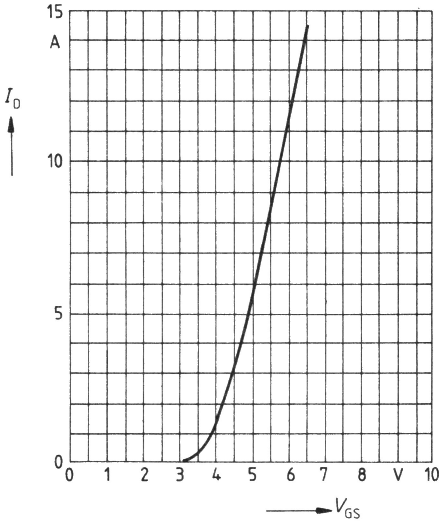


Fig.5 *Typical transfer characteristic* $I_D = f(V_{GS})$ *Conditions: 80 µs pulse test;* V_{DS} *= 25 V,* T_{mb} *= 25 °C.*

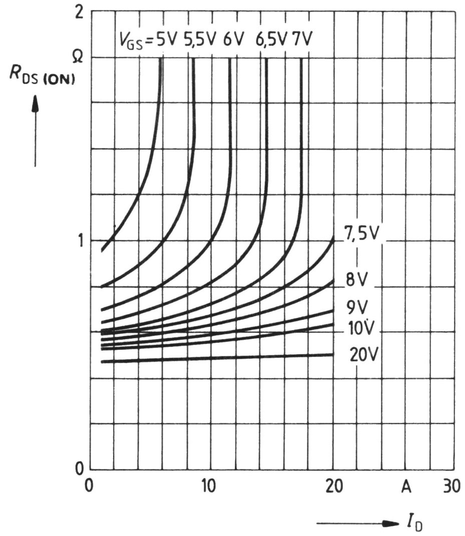


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

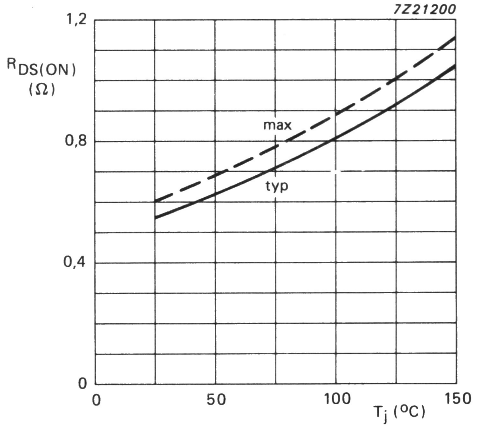


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 6,5 A; V_{GS} = 10 V.

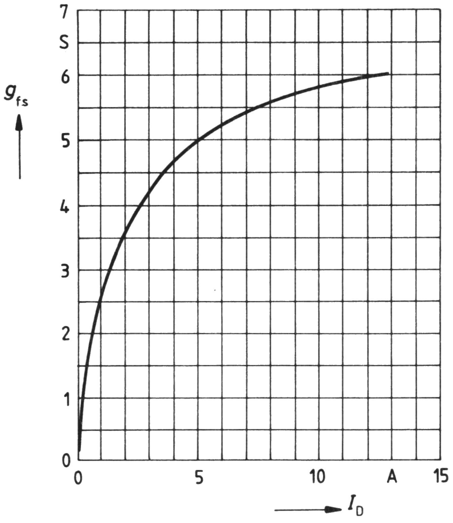


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

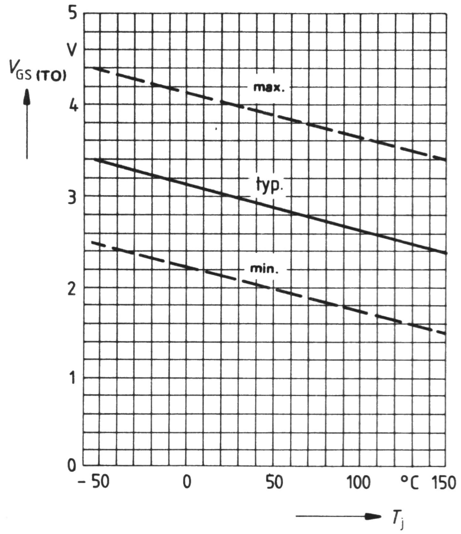


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

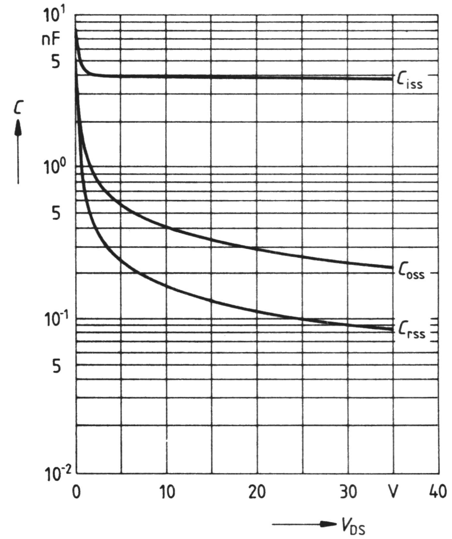


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

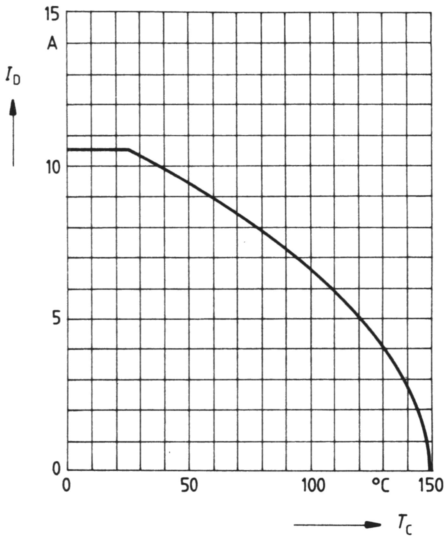


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

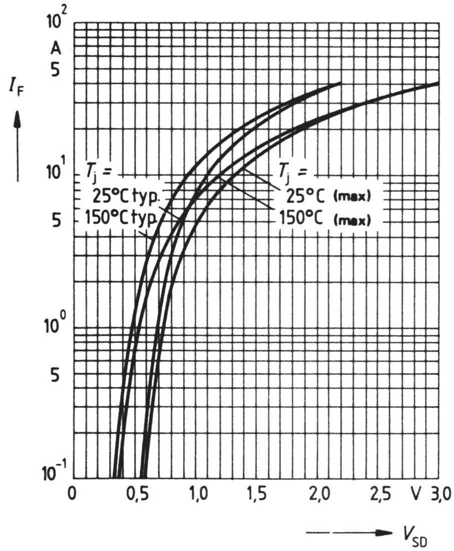


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ μs.

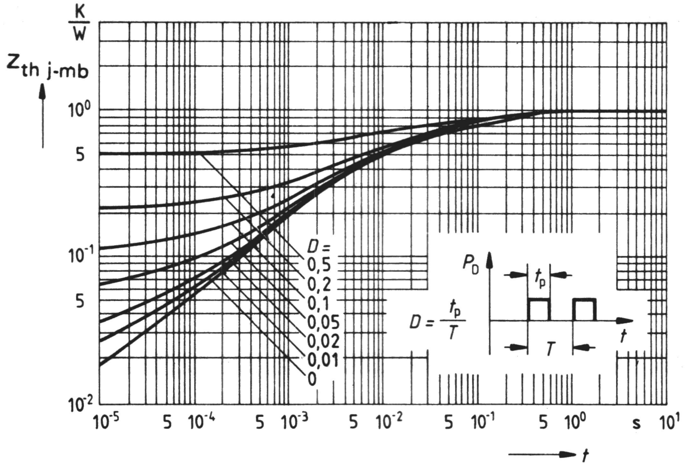


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

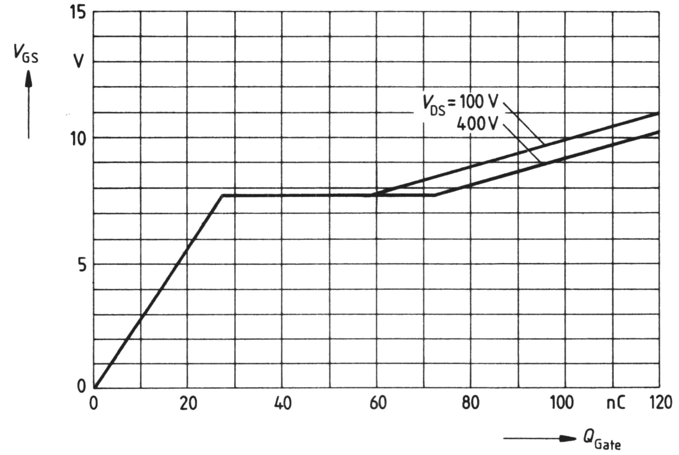


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 14,4 A.

PowerMOS transistor BUZ385

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

FREDFET* with fast-recovery reverse diode. This device is particularly suitable for motor control applications, e.g. in full-bridge configurations for which faster recovery characteristics simplify design for inductive loads.

QUICK REFERENCE DATA

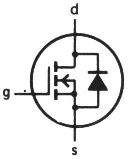
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	500	V
I_D	Drain current (d.c.)	9,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	0,8	Ω

* Fast Recovery Epitaxial Diode FET.

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



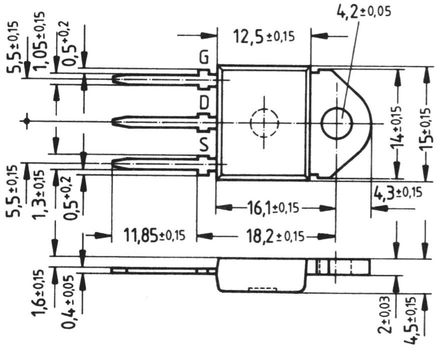

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	500	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	500	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	9,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	5,7	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	36	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	500	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 500 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 6,5 A	–	0,7	0,8	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 6,5 A	2,7	6,6	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3800	4900	pF
C_{oss}	Output capacitance		–	250	400	pF
C_{rss}	Feedback capacitance		–	100	170	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,8 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	50	75	ns
t_r	Turn-on rise time		–	80	120	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reserve drain current	T_{mb} = 25 °C	–	–	9,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	36	A
V_{SD}	Diode forward on-voltage	I_F = 18 A; V_{GS} = 0 V; T_j = 25 °C	–	1,5	1,9	V
t_{rr}	Reverse recovery time	I_F = 9,0 A; T_j = 25 °C	–	180	250	ns
		$-dI_F/dt$ = T_j = 150 °C	–	220	300	ns
Q_{rr}	Reverse recovery charge	100 A/μs; T_j = 25 °C	–	0,65	1,2	μC
		V_{GS} = 0 V; T_j = 150 °C	–	2,6	5,0	μC
I_{rrm}	Reverse recovery current	V_R = 100 V T_j = 150 °C	–	15	–	A

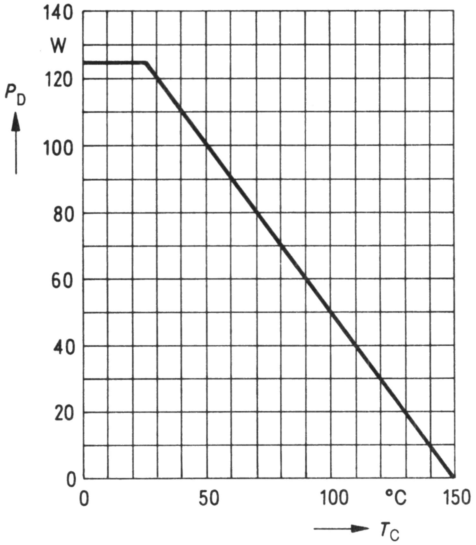


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

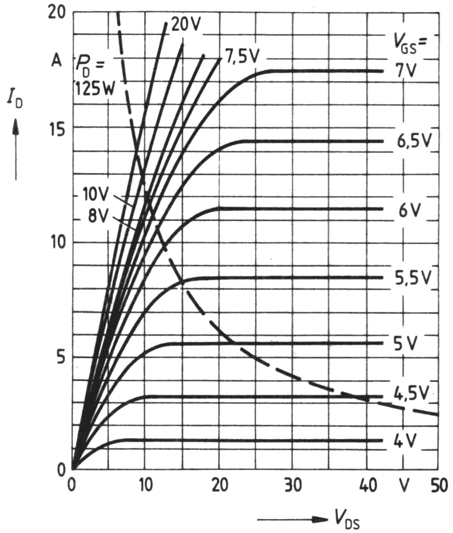


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

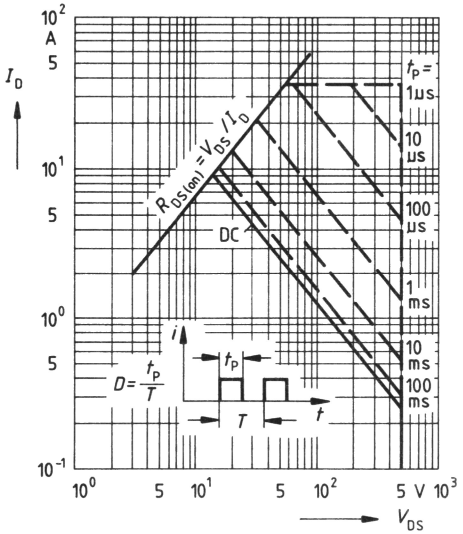


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

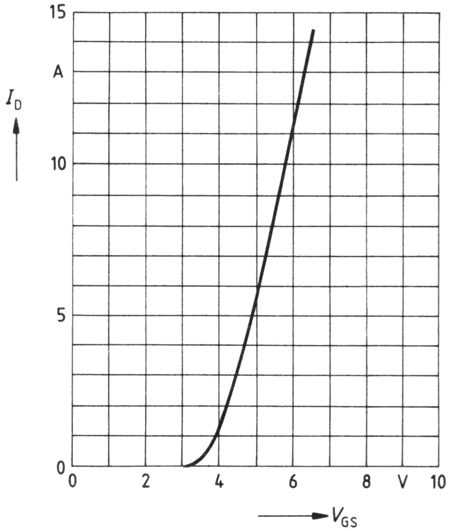


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

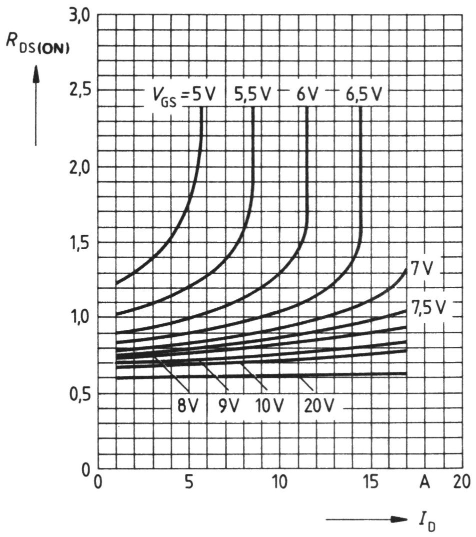


Fig. 6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; $T_j = 25$ °C.

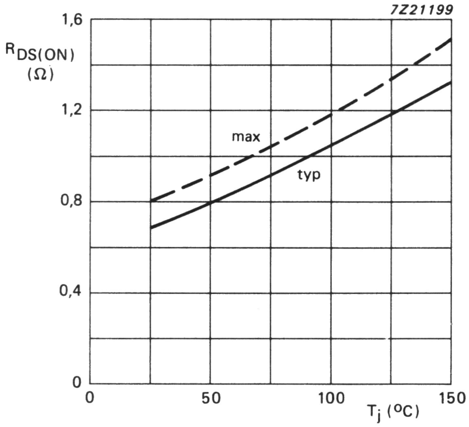


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: $I_D = 6{,}5$ A; $V_{GS} = 10$ V.

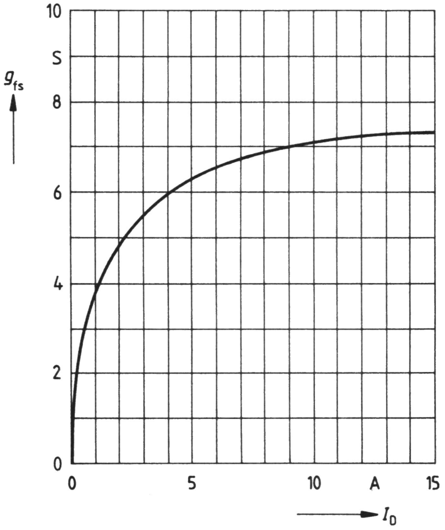


Fig. 8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
$V_{DS} = 25$ V; $T_j = 25$ °C.

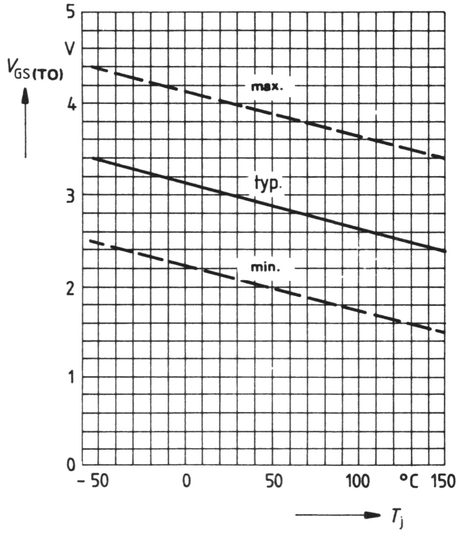


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; $I_D = 1$ mA.

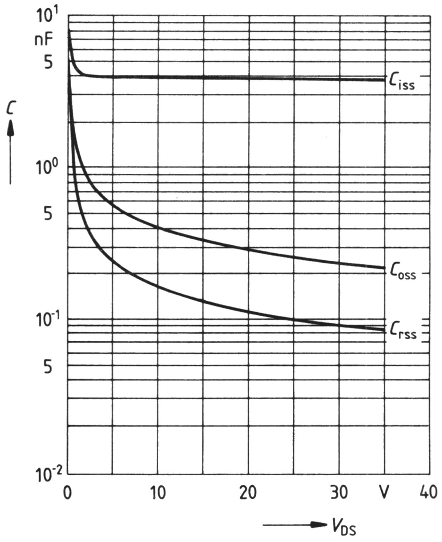


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

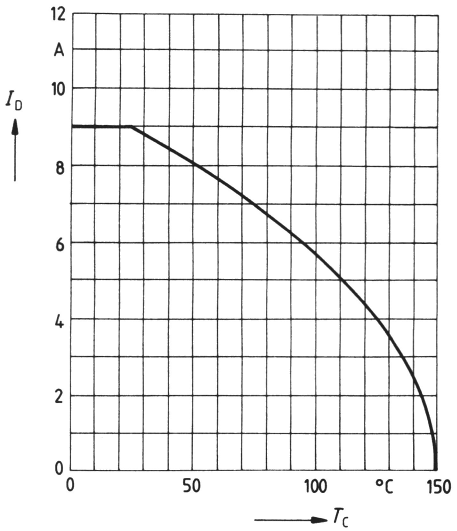


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

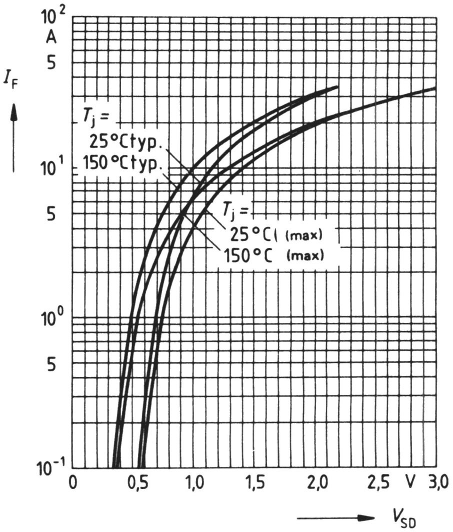


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

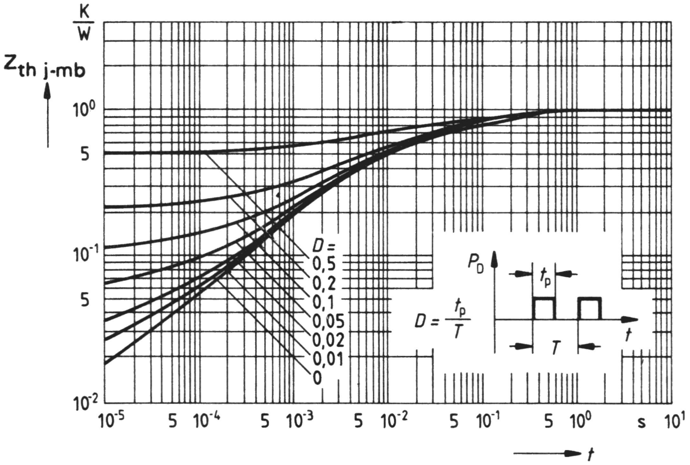


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

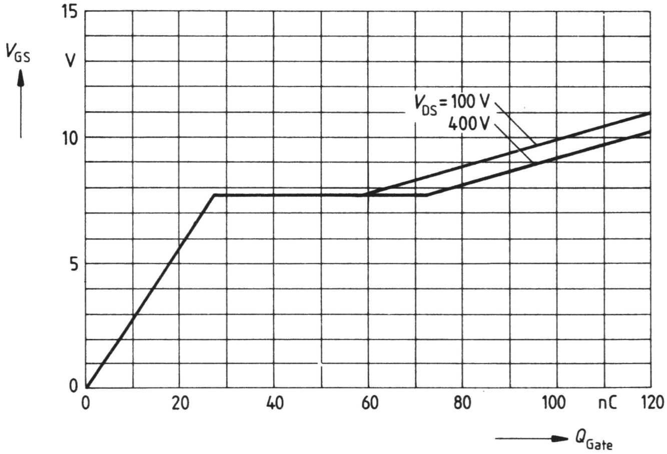


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; I_{DM} = 14,4 A.

PowerMOS transistor BUZ307

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

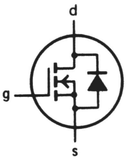
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	3,0	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	3,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



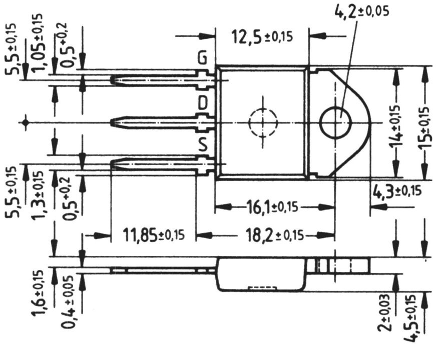

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 50 °C	–	3,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,1	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	12	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	2,7	3,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	1,0	1,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,3 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	3,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	12	A
V_{SD}	Diode forward on-voltage	I_F = 6 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,30	V
t_{rr}	Reverse recovery time	I_F = 3 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	1800	–	ns
Q_{rr}	Reverse recovery charge	100 A/μs	–	12	–	μC

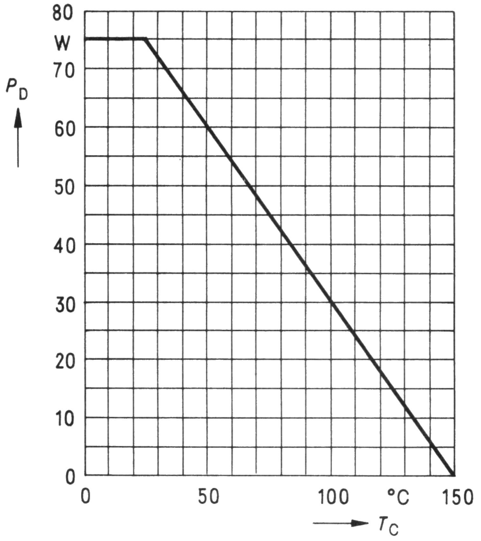


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

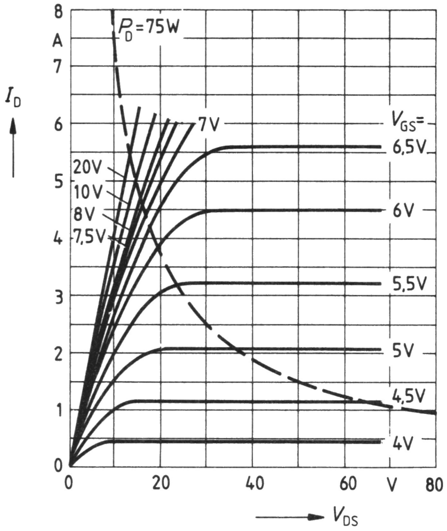


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

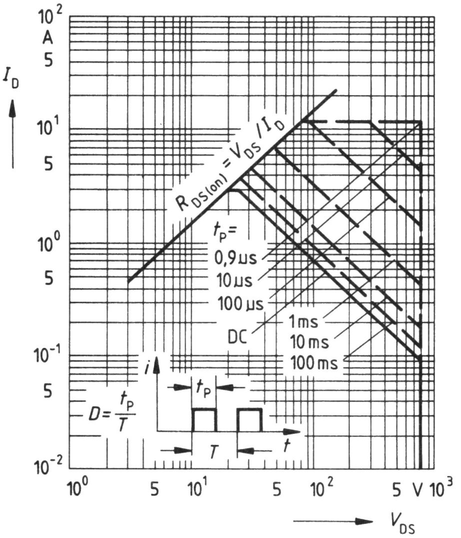


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

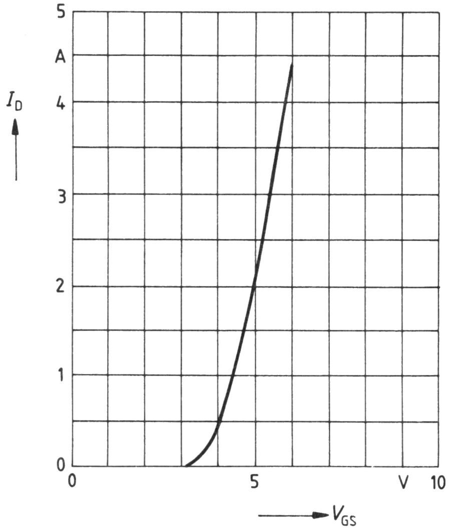


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

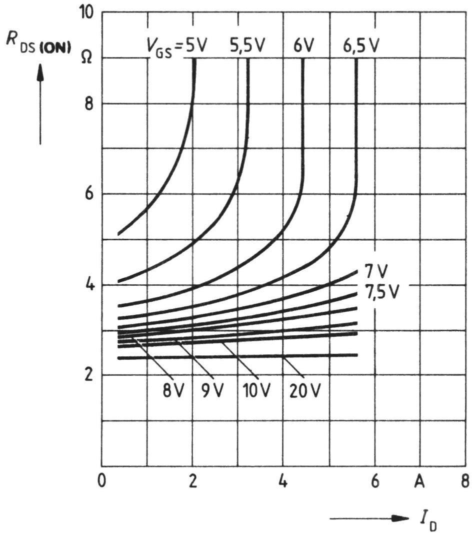


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

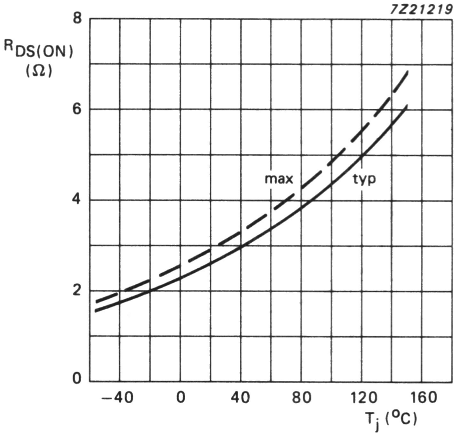


Fig.7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 1,5 A; V_{GS} = 10 V.

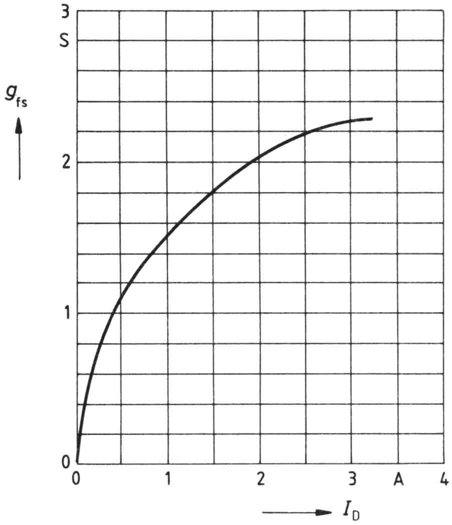


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

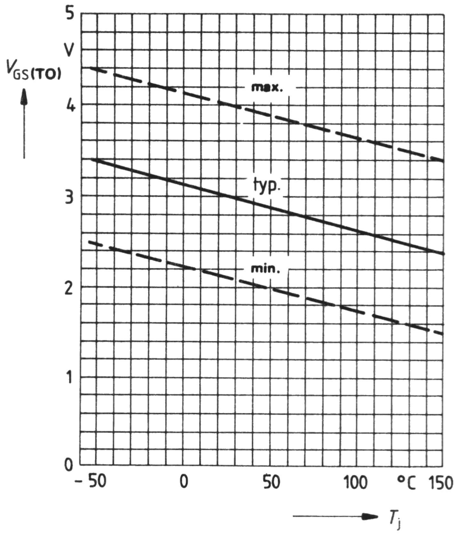


Fig.9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

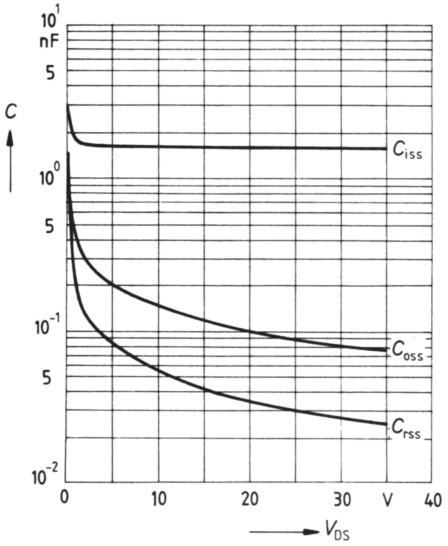


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

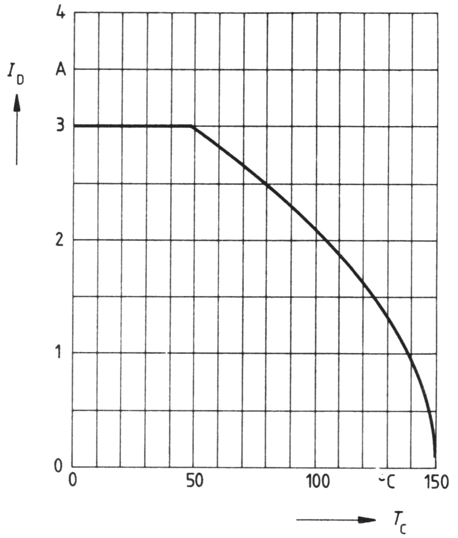


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

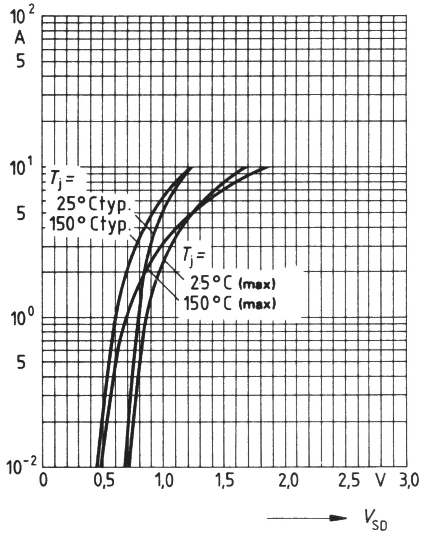


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

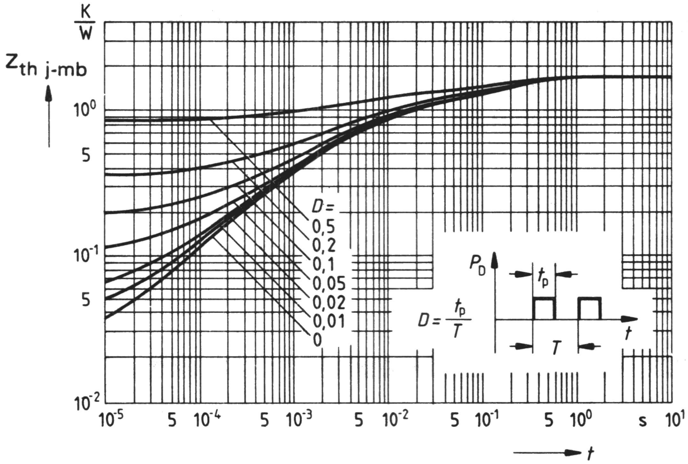


Fig. 13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

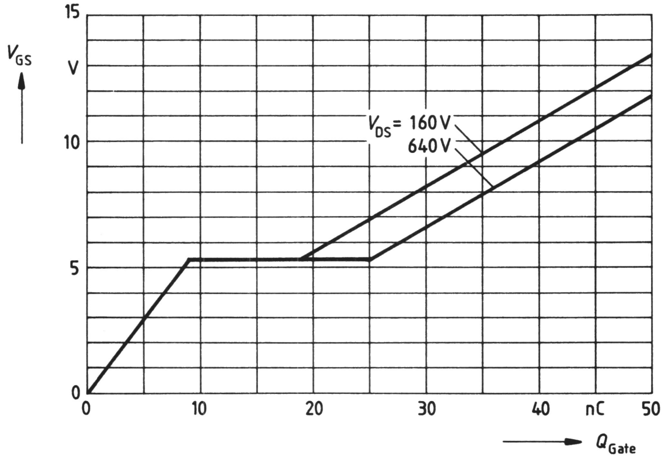


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5{,}0$ A.

PowerMOS transistor BUZ308

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

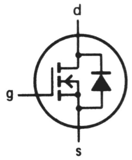
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	2,6	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	4,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



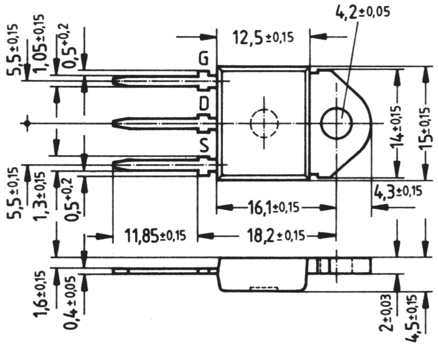

5,5±0,15
1,05±0,15
0,5+0,2
G
D
S
12,5±0,15
4,2±0,05
14±0,15
15±0,15
4,3±0,15
16,1±0,15
18,2±0,15
11,85±0,15
5,5±0,15
1,3±0,15
0,5+0,2
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 *TO218AA; drain connected to mounting base.*

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 50 °C	–	2,6	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	10	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,5 A	–	3,5	4,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,5 A	1,0	1,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	90	150	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,1 A; VGS = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,6	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5,2 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,30	V
t_{rr}	Reverse recovery time	I_F = 2,6 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1800	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	12	–	µC

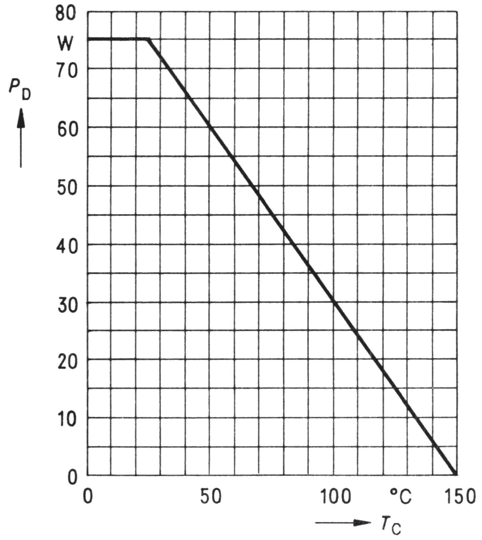


Fig.2 Power dissipation $P_D = f(T_{mb})$.

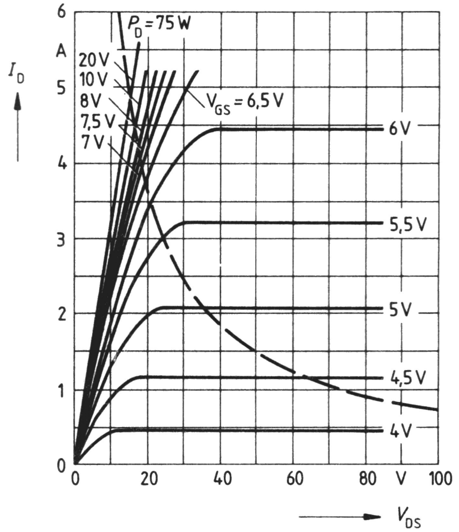


Fig.3 Typical output characteristics $I_D = f(V_{DS})$
Parameter: V_{GS}; 80 μs pulse test;
$T_{mb} = 25$ °C.

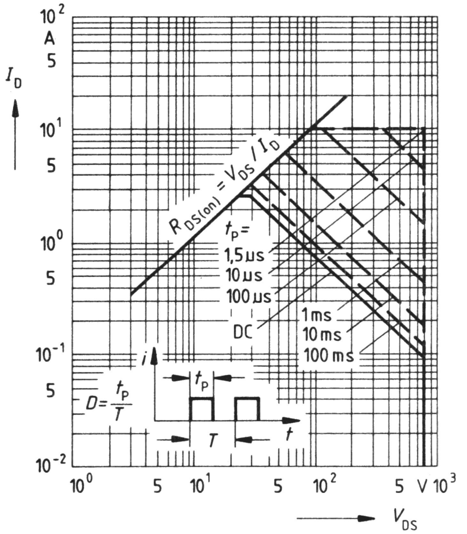


Fig.4 Safe operating area $I_D(DC)$ and
$I_{DM} = f(V_{DS})$
Parameter: t_p; $D = 0{,}01$; $T_{mb} = 25$ °C.

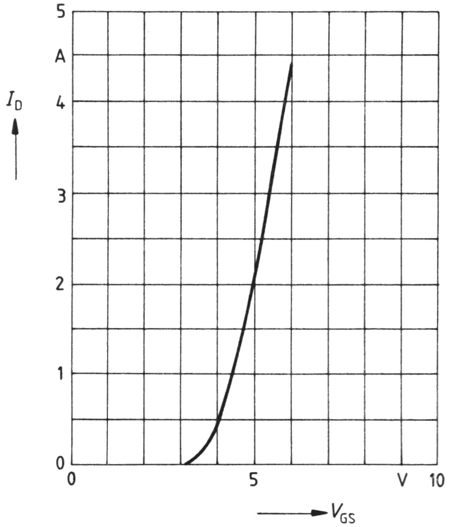


Fig.5 Typical transfer characteristic $I_D = f(V_{GS})$
Conditions: 80 μs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

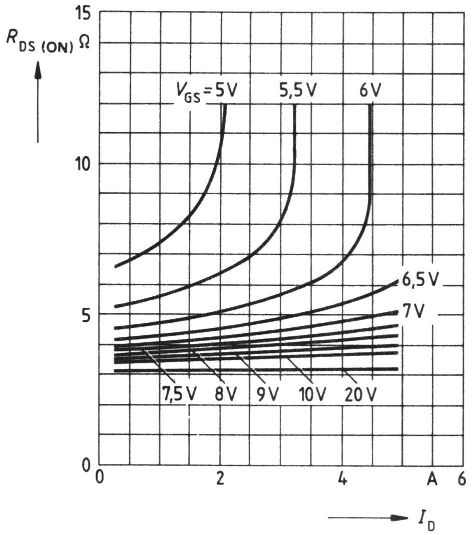


Fig.6 *Typical drain-source on-state resistance* $R_{DS(ON)} = f(I_D)$ *Parameter:* V_{GS}; $T_j = 25$ °C.

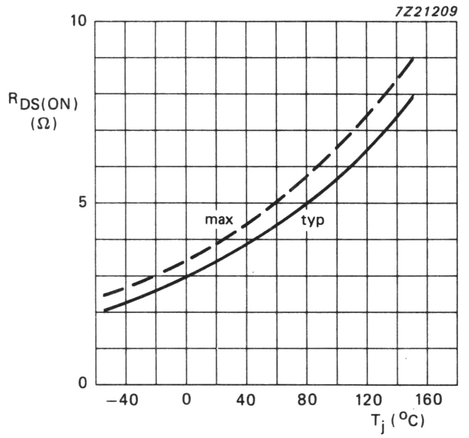


Fig.7 *Drain-source on-state resistance* $R_{DS(ON)} = f(T_j)$ *Conditions:* $I_D = 1{,}5$ A; $V_{GS} = 10$ V.

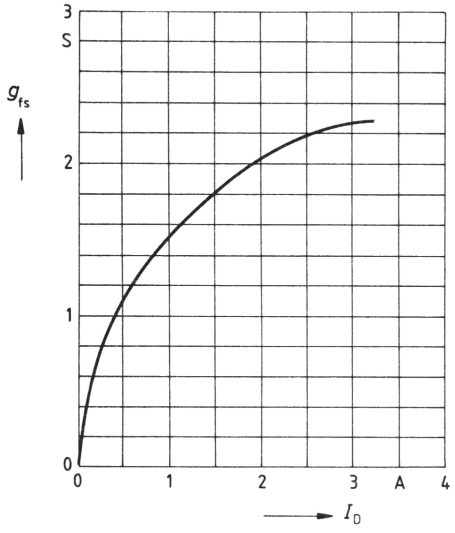


Fig.8 *Typical transconductance* $g_{fs} = f(I_D)$ *Conditions: 80 μs pulse test;* $V_{DS} = 25$ V; $T_j = 25$ °C.

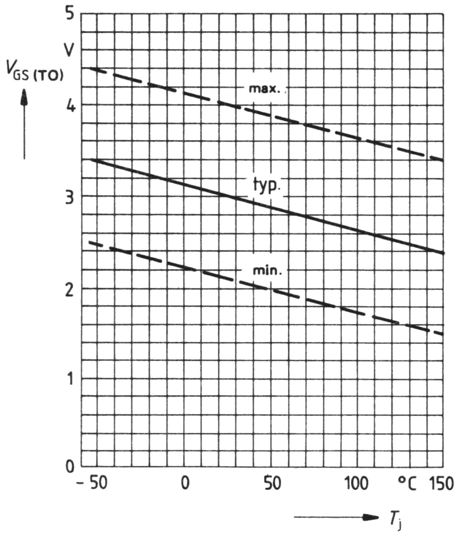


Fig.9 *Gate threshold voltage* $V_{GS(TO)} = f(T_j)$ *Conditions:* $V_{DS} = V_{GS}$; $I_D = 1$ mA.

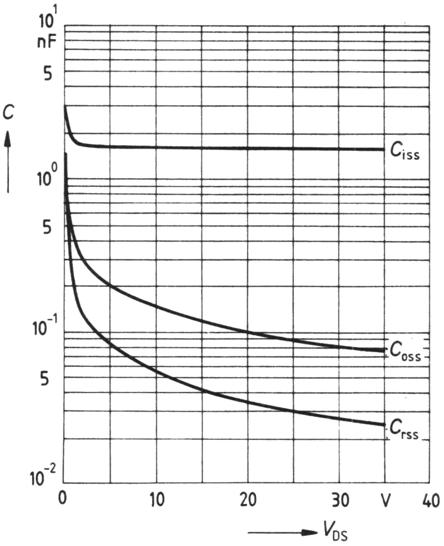


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

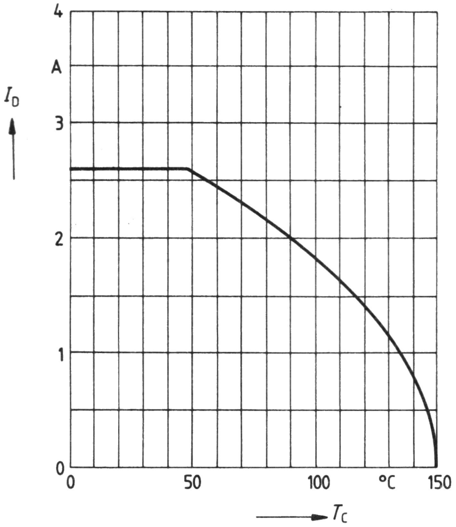


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

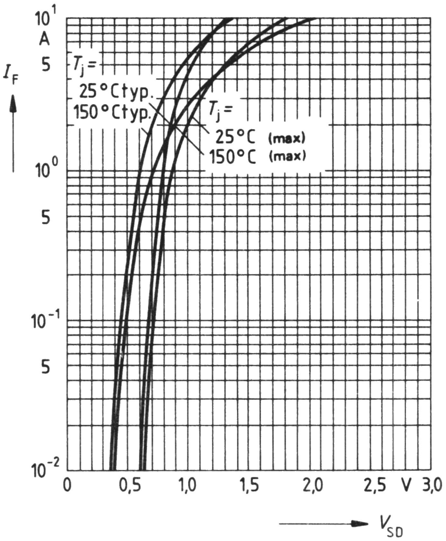


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

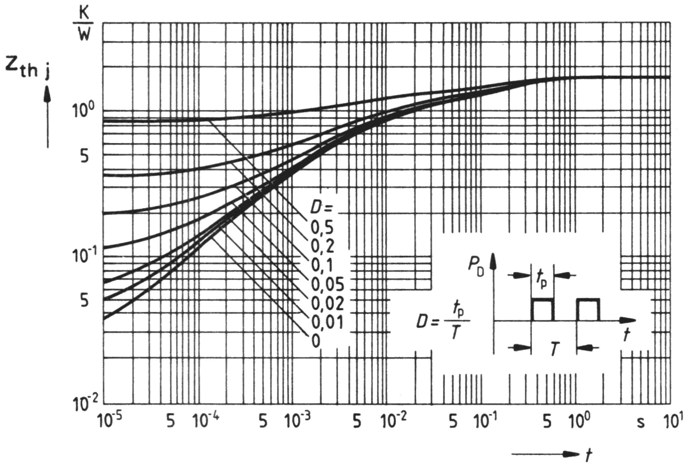


Fig. 13 Transient thermal impedance $Z_{th\,j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

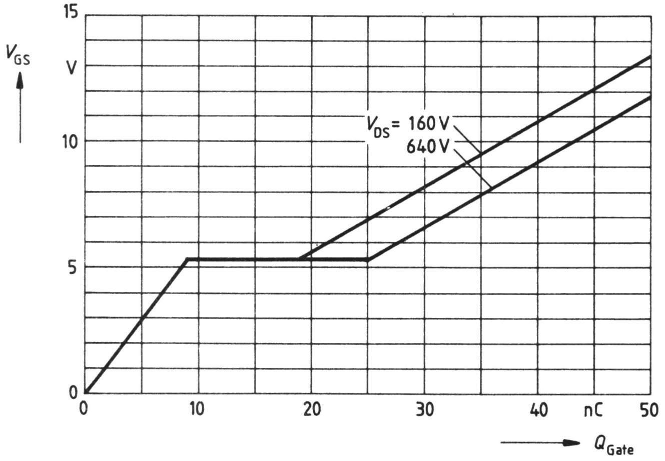


Fig. 14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 5{,}0$ A.

PowerMOS transistor

BUZ355

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

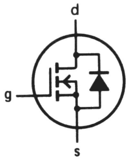
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	6,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	1,5	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



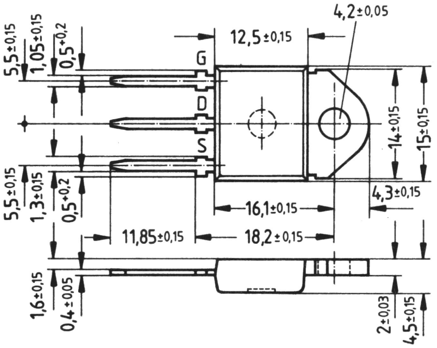

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
18,2±0,15
11,85±0,15
5,5±0,15
1,3±0,15
0,5+0,2
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	6,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,9	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	24	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,8 A	–	1,3	1,5	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,8 A	1,8	3,3	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	200	350	pF
C_{rss}	Feedback capacitance		–	80	140	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,6 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	6,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	24	A
V_{SD}	Diode forward on-voltage	I_F = 12 A; V_{GS} = 0 V; T_j = 25 °C	–	1,1	1,3	V
t_{rr}	Reverse recovery time	I_F = 6 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	1,8	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	25	–	µC

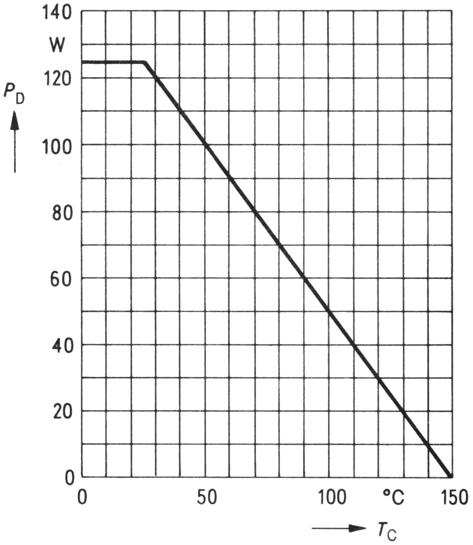


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

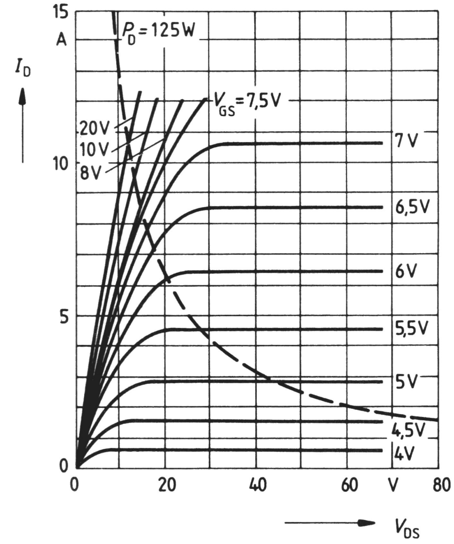


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

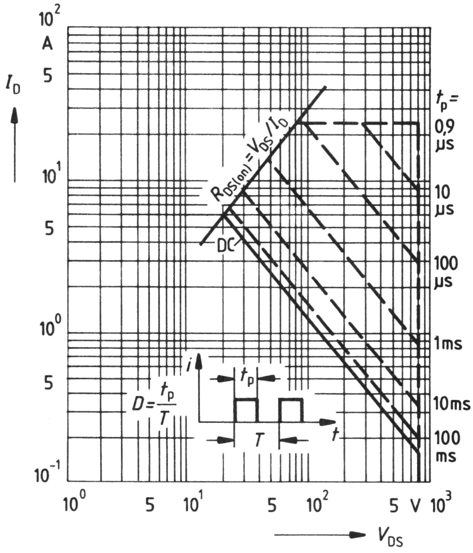


Fig.4 *Safe operating area $I_D(DC)$ and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

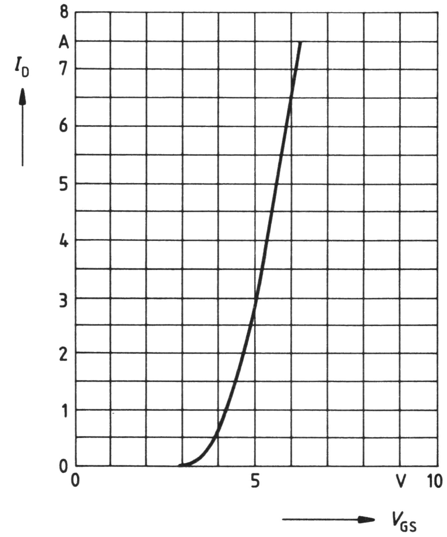


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

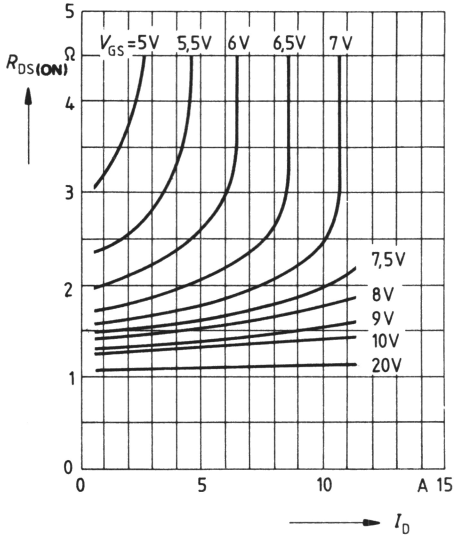


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

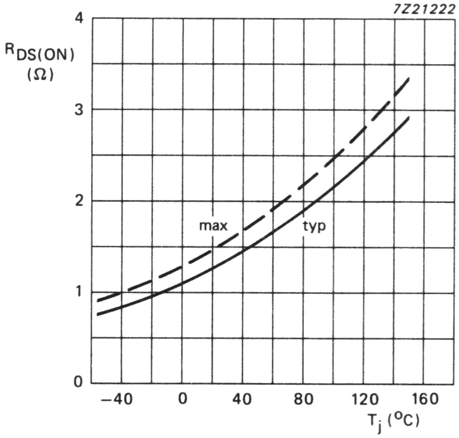


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 4,2 A; V_{GS} = 10 V.

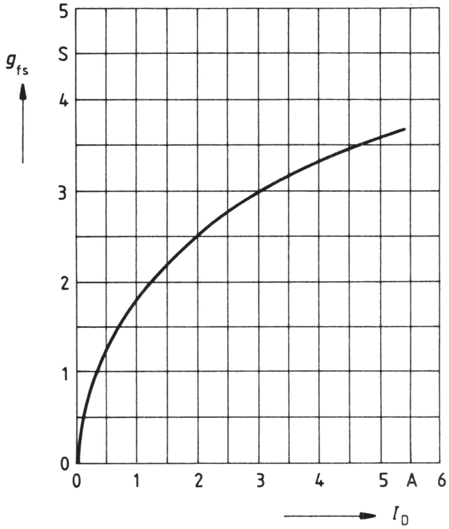


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 μs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

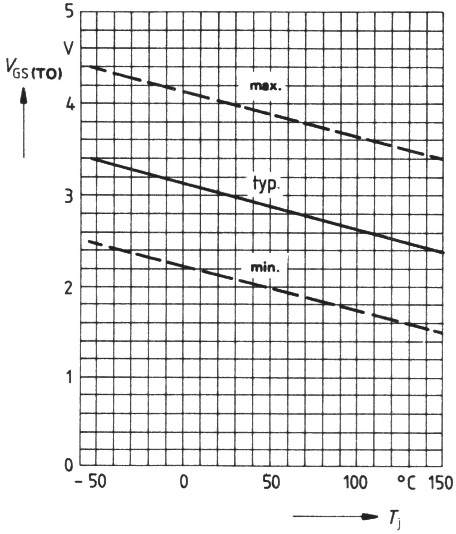


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

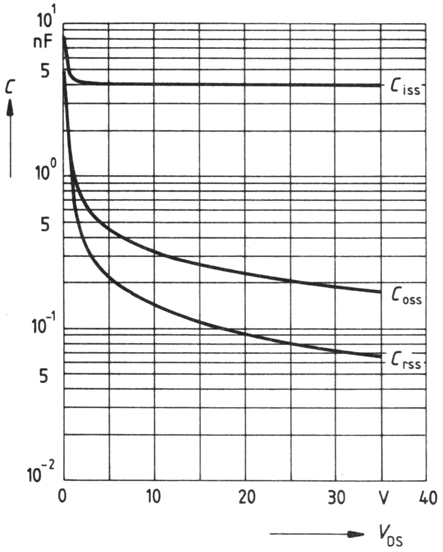


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

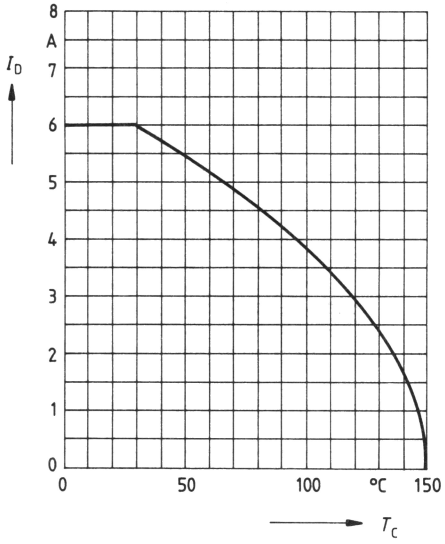


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

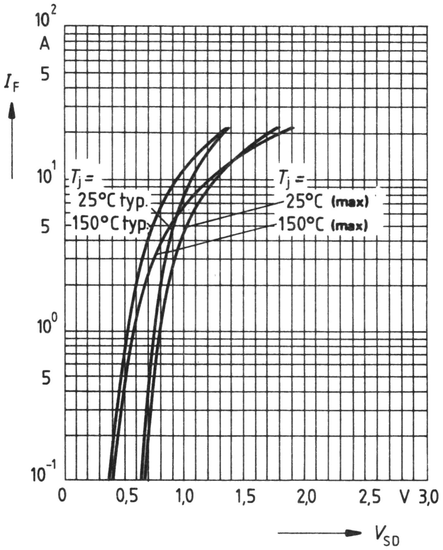


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

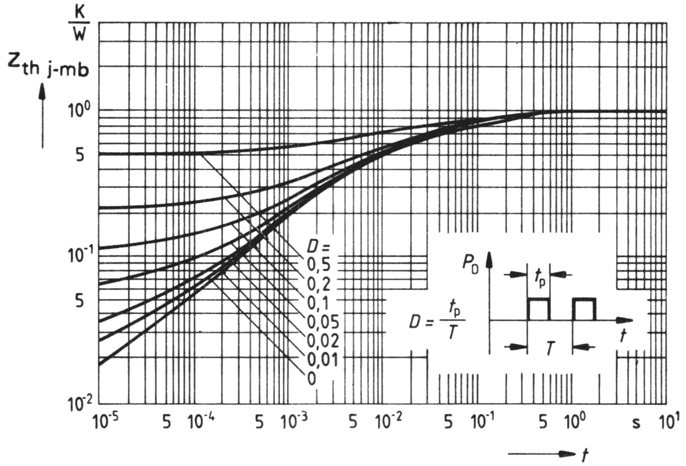


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

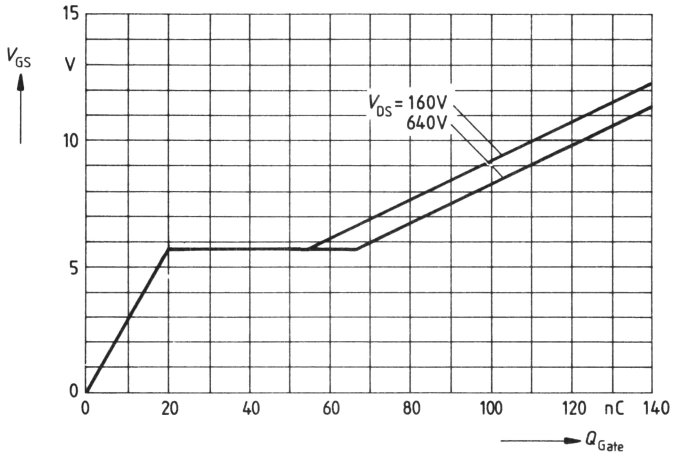


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 9{,}0\ A$.

PowerMOS transistor

BUZ356

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

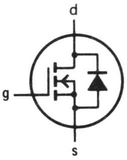
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	800	V
I_D	Drain current (d.c.)	5,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



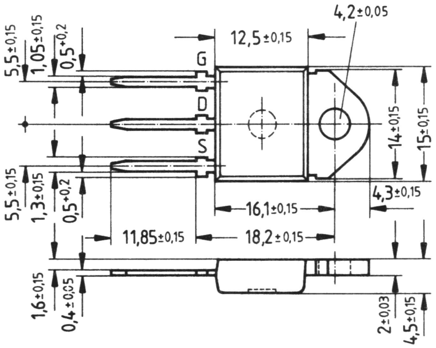

4,2±0,05
12,5±0,15
5,5±0,15
1,05±0,15
0,5+0,2
G
D
S
14±0,15
15±0,15
4,3±0,15
16,1±0,15
5,5±0,15
1,3±0,15
0,5+0,2
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	800	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	800	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 35 °C	–	5,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,3	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	21	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	800	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 800 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,8 A	–	1,6	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,8 A	1,8	3,3	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	200	350	pF
C_{rss}	Feedback capacitance		–	80	140	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	20	A
V_{SD}	Diode forward on-voltage	I_F = 10 A; V_{GS} = 0 V; T_j = 25 °C	–	1,0	1,3	V
t_{rr}	Reverse recovery time	I_F = 5 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	1,8	–	ns
Q_{rr}	Reverse recovery charge	100 A/μs	–	25	–	μC

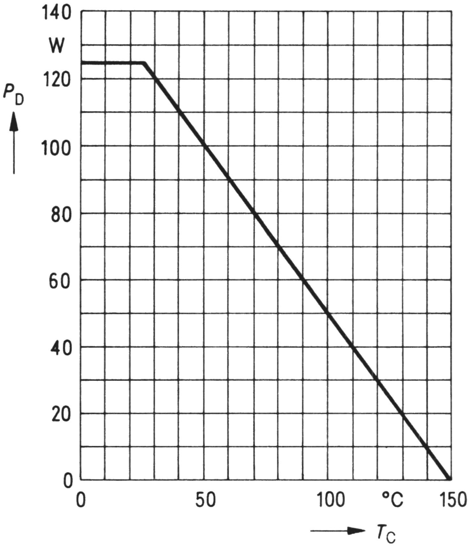


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

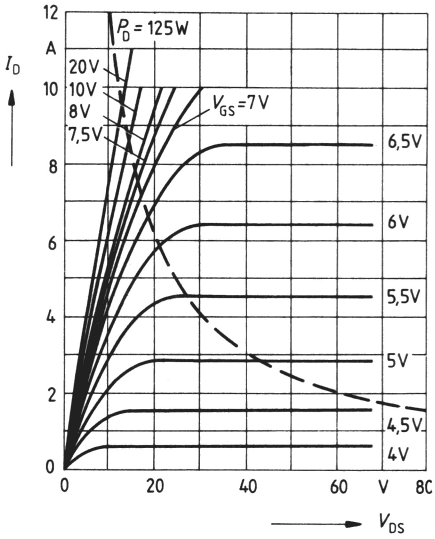


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 µs pulse test; T_{mb} = 25 °C.*

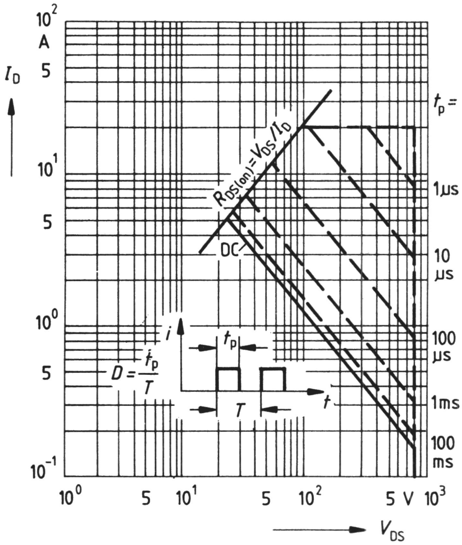


Fig.4 *Safe operating area $I_D(DC)$ and $I_{DM} = f(V_{DS})$ Parameter: t_p; D = 0,01; T_{mb} = 25 °C.*

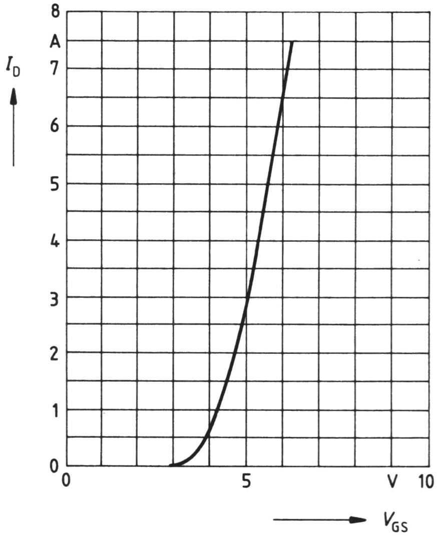


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 µs pulse test; V_{DS} = 25 V, T_{mb} = 25 °C.*

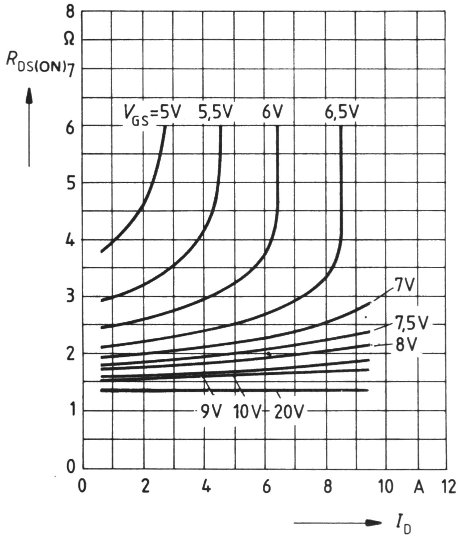


Fig.6 Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

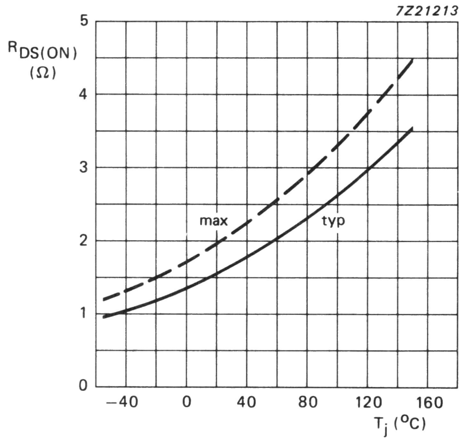


Fig. 7 Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$
Conditions: I_D = 3,8 A; V_{GS} = 10 V.

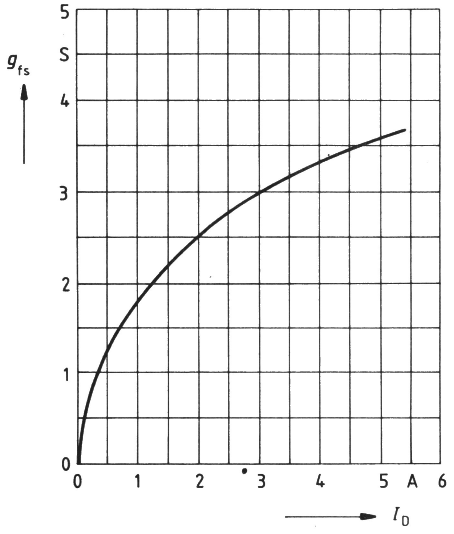


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

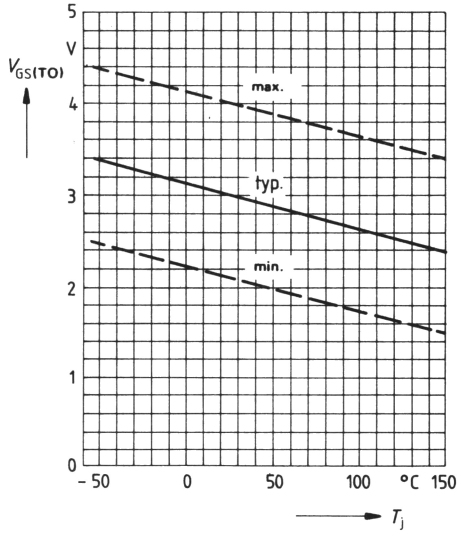


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

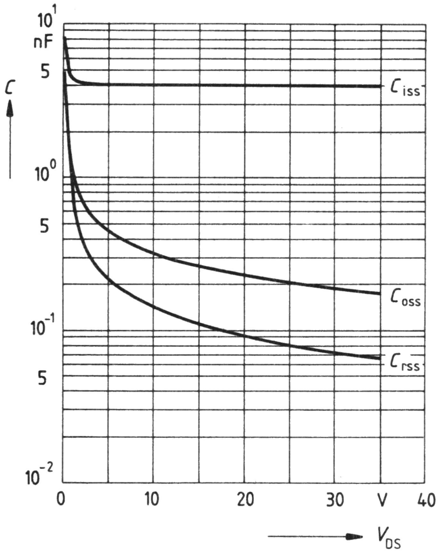


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

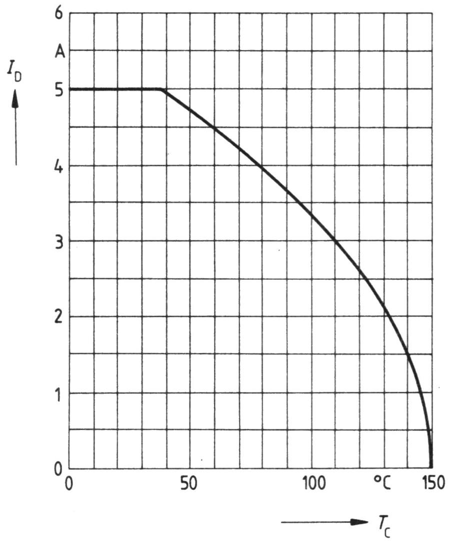


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

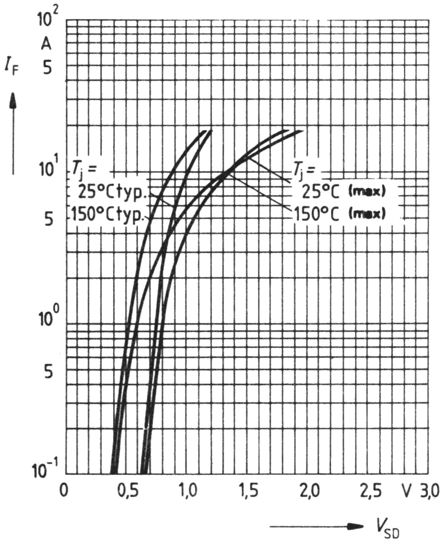


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

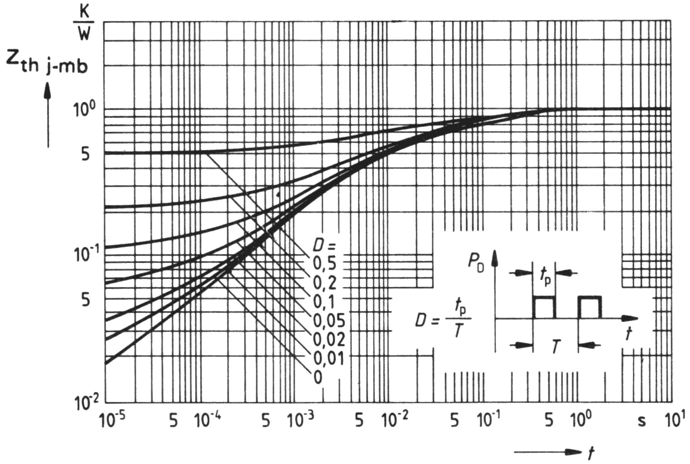


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

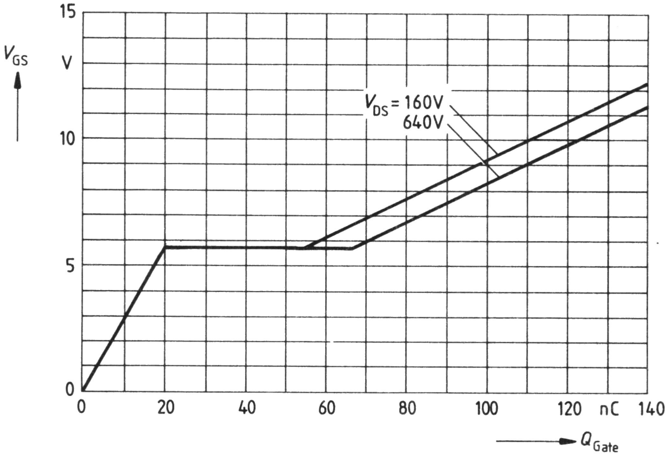


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 9,0$ A.

PowerMOS transistor BUZ310

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

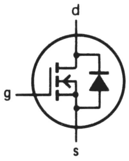
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,5	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	5,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



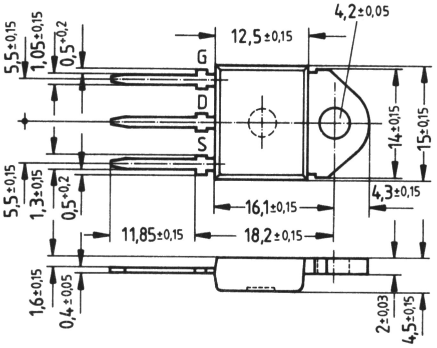

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\ k\Omega$	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	$T_{mb} = 25\ °C$	–	2,5	A
I_D	Drain current (d.c.)	$T_{mb} = 100\ °C$	–	1,6	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\ °C$	–	10	A
P_{tot}	Total power dissipation	$T_{mb} = 25\ °C$	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb} = 1{,}67$ K/W
From junction to ambient	$R_{th\ j\text{-}a} = 45$ K/W

STATIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\ V$; $I_D = 0{,}25\ mA$	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\ mA$	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 1000\ V$; $V_{GS} = 0\ V$; $T_j = 25\ °C$	–	20	250	µA
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 1000\ V$; $V_{GS} = 0\ V$; $T_j = 125\ °C$	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\ V$; $V_{DS} = 0\ V$	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 1{,}6\ A$	–	4,5	5,0	Ω

DYNAMIC CHARACTERISTICS

$T_{mb} = 25\ °C$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	$V_{DS} = 25\ V$; $I_D = 1{,}6\ A$	0,7	1,5	–	S
C_{iss}	Input capacitance	$V_{GS} = 0\ V$; $V_{DS} = 25\ V$; $f = 1\ MHz$	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	$V_{DD} = 30\ V$; $I_D = 2\ A$; $V_{GS} = 10\ V$; $R_{GS} = 50\ \Omega$; $R_{gen} = 50\ \Omega$	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	10	A
V_{SD}	Diode forward on-voltage	I_F = 5 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	2,0	–	µs
Q_{rr}	Reverse recovery charge	100 A/µs	–	15	–	µC

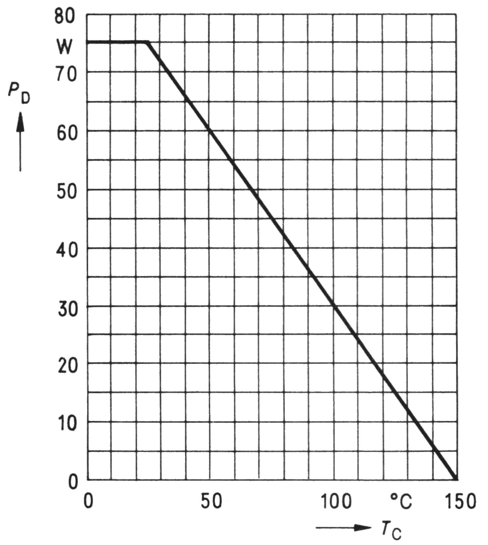


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

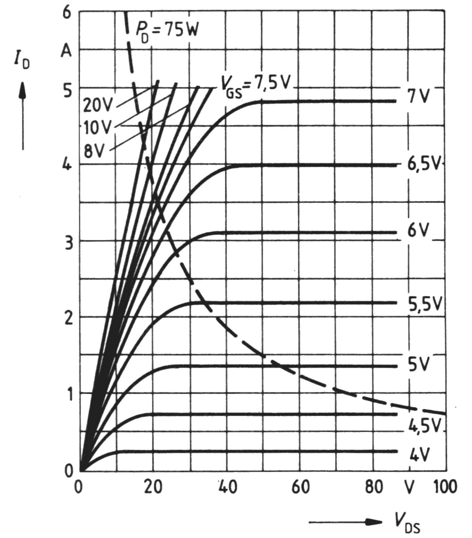


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
$T_{mb} = 25$ °C.

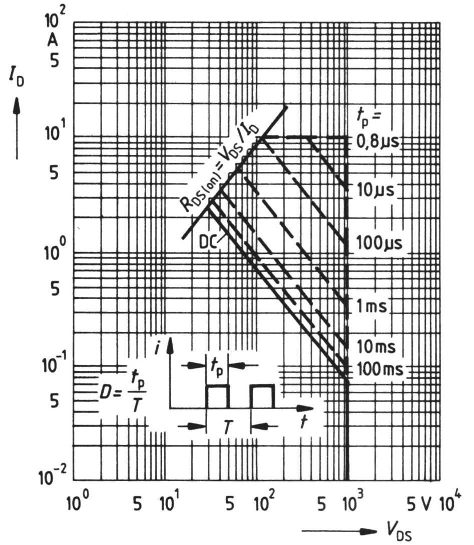


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; $T_{mb} = 25$ °C.

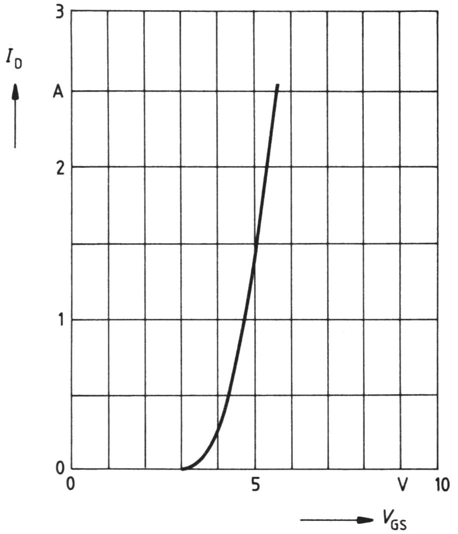


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; $V_{DS} = 25$ V,
$T_{mb} = 25$ °C.

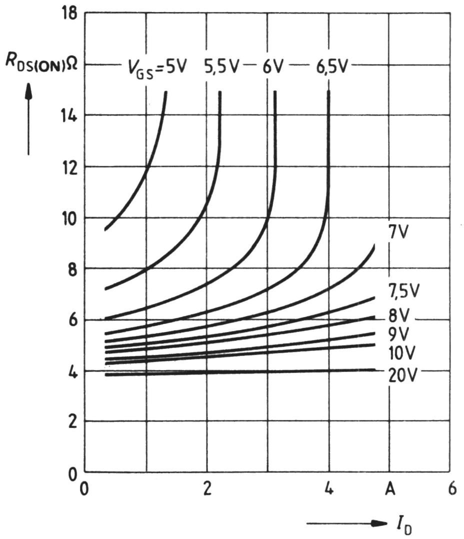


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

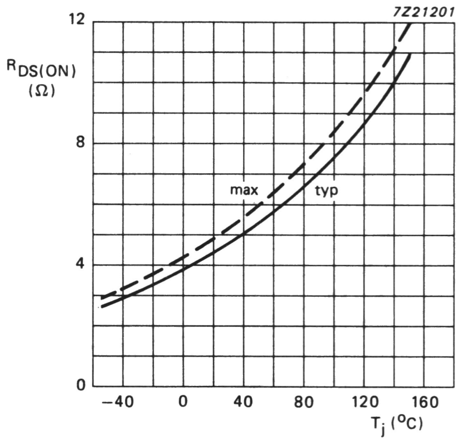


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 1,6 A; V_{GS} = 10 V.

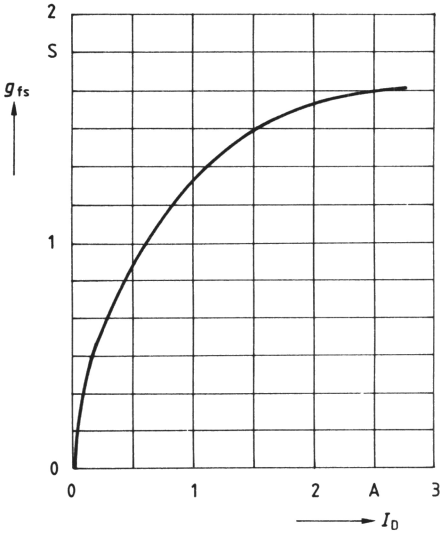


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

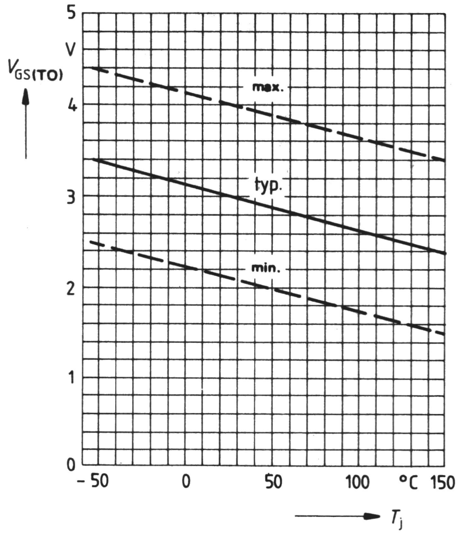


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

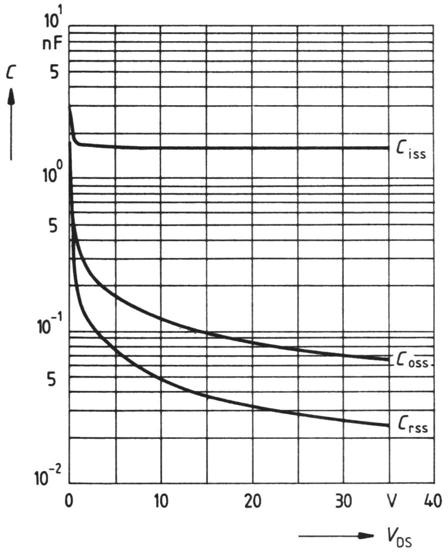


Fig.10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

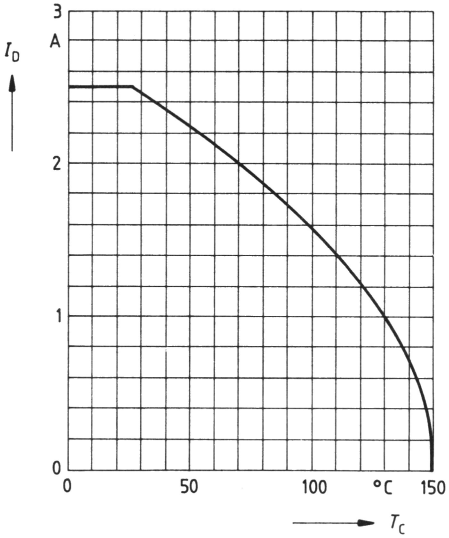


Fig.11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geqslant 10$ V.

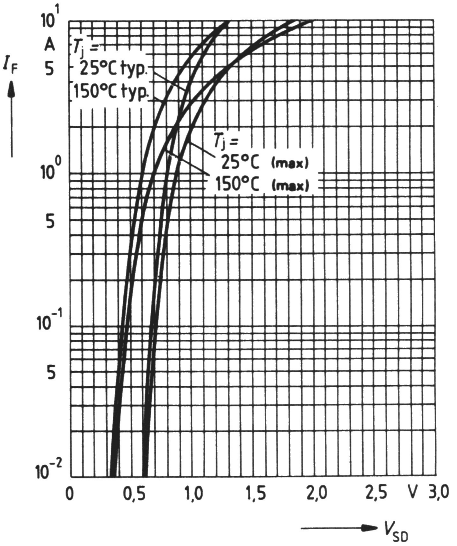


Fig.12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

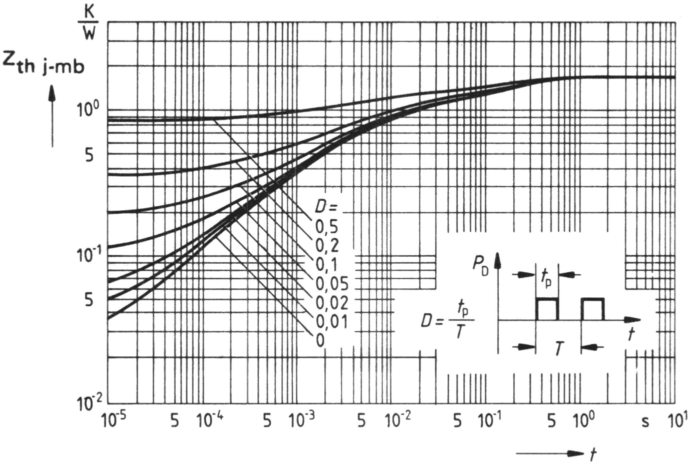


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

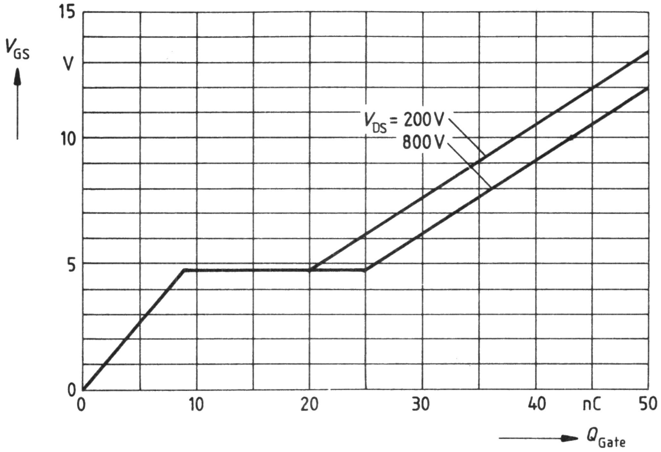


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 3{,}75$ A.

PowerMOS transistor BUZ311

May 1987

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

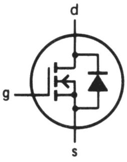
QUICK REFERENCE DATA

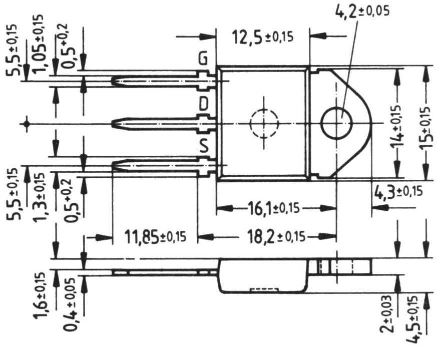
SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	2,3	A
P_{tot}	Total power dissipation	75	W
$R_{DS(ON)}$	Drain-source on-state resistance	6,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g





5,5±0,15
1,05±0,15
0,5+0,2
12,5±0,15
4,2±0,05
G
D
S
14±0,15
15±0,15
5,5±0,15
1,3±0,15
0,5+0,2
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig. 1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	2,3	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	1,5	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	9,0	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	75	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,67 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 1,6 A	–	5,0	6,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 1,6 A	0,7	1,5	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	1600	2100	pF
C_{oss}	Output capacitance		–	70	120	pF
C_{rss}	Feedback capacitance		–	30	55	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 1,7 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	30	45	ns
t_r	Turn-on rise time		–	40	60	ns
$t_{d\ off}$	Turn-off delay time		–	110	140	ns
t_f	Turn-off fall time		–	60	80	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	2,3	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	9,0	A
V_{SD}	Diode forward on-voltage	I_F = 4,6 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 2,3 A; $-dI_F/dt$ = 100 A/μs; V_{GS} = 0 V; V_R = 100 V	–	2,0	–	μs
Q_{rr}	Reverse recovery charge	100 A/μs	–	15	–	μC

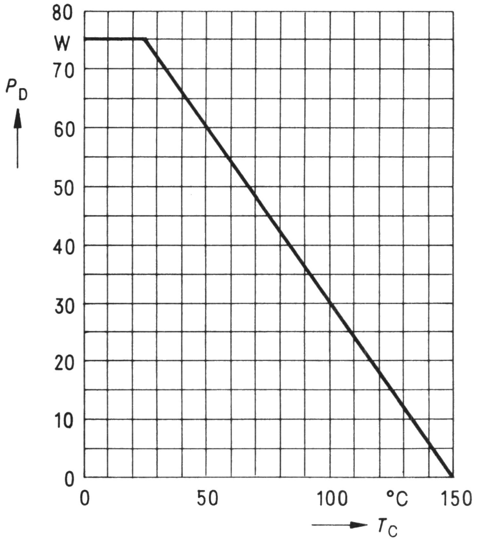


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

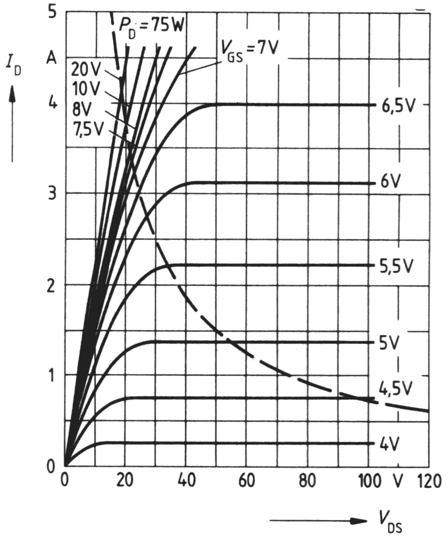


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$ Parameter: V_{GS}; 80 μs pulse test; $T_{mb} = 25$ °C.*

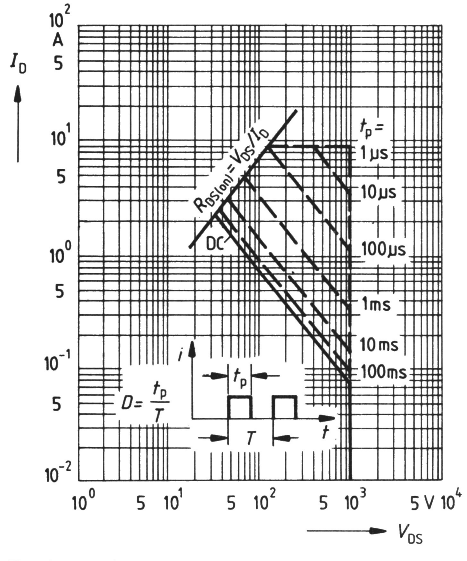


Fig.4 *Safe operating area $I_D(DC)$ and $I_{DM} = f(V_{DS})$ Parameter: t_p; $D = 0,01$; $T_{mb} = 25$ °C.*

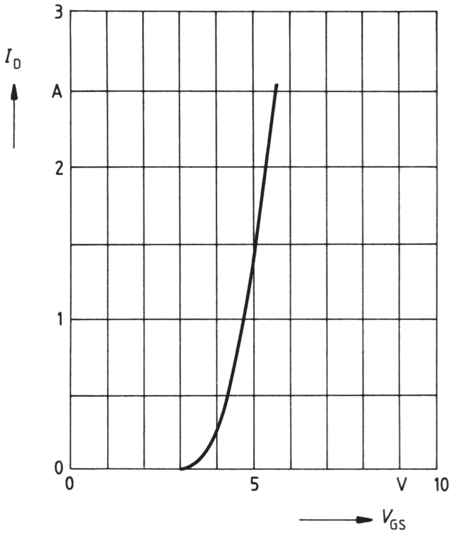


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$ Conditions: 80 μs pulse test; $V_{DS} = 25$ V, $T_{mb} = 25$ °C.*

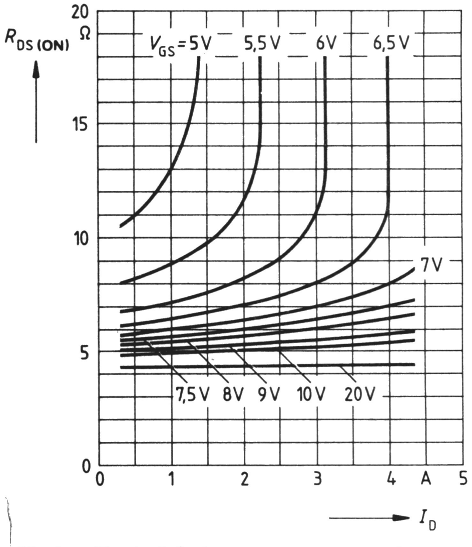


Fig. 6 *Typical drain-source on-state resistance $R_{DS(ON)} = f(I_D)$ Parameter: V_{GS}; T_j = 25 °C.*

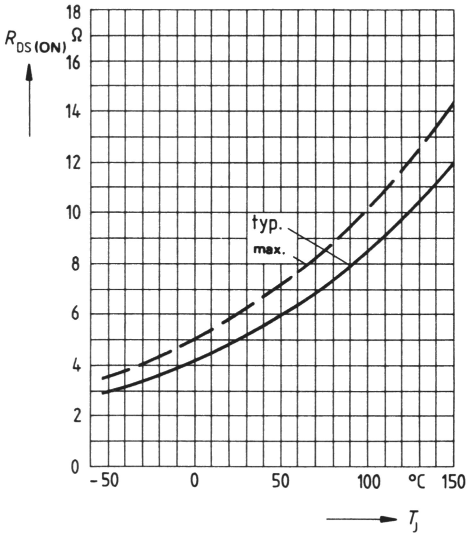


Fig. 7 *Drain-source on-state resistance $R_{DS(ON)} = f(T_j)$ Conditions: I_D = 1,6 A; V_{GS} = 10 V.*

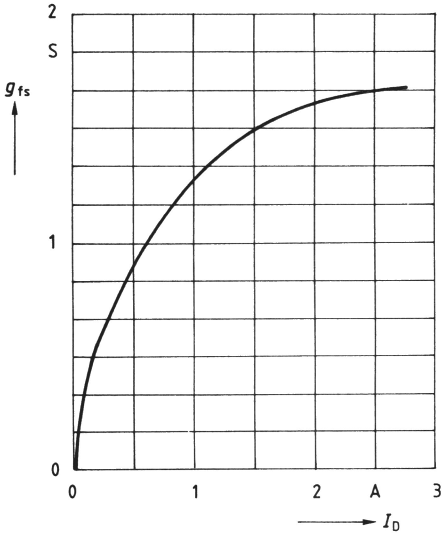


Fig. 8 *Typical transconductance $g_{fs} = f(I_D)$ Conditions: 80 µs pulse test; V_{DS} = 25 V; T_j = 25 °C.*

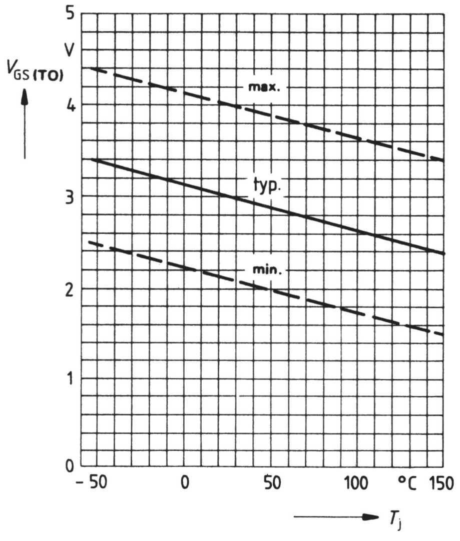


Fig. 9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$ Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.*

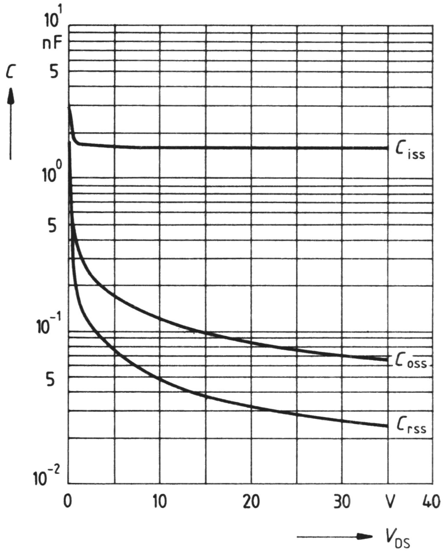


Fig. 10 Typical capacitances $C = f(V_{DS})$ Conditions: $V_{GS} = 0$; $f = 1$ MHz.

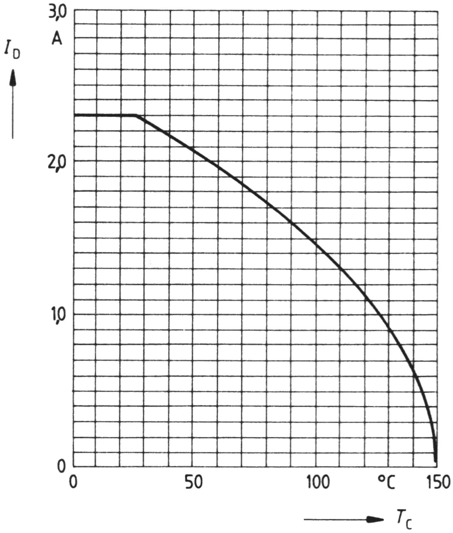


Fig. 11 Continuous drain current $I_D = f(T_{mb})$ Conditions: $V_{GS} \geq 10$ V.

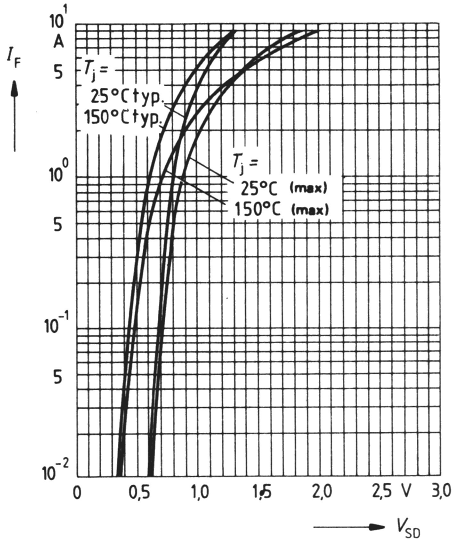


Fig. 12 Forward characteristics of reverse diode $I_F = f(V_{SD})$ Parameter: T_j; $t_p = 80$ μs.

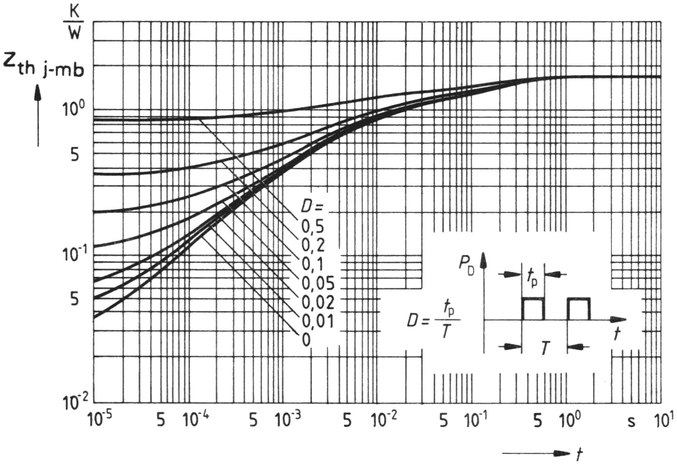


Fig. 13 *Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$*
Parameter: $D = t_p/T$.

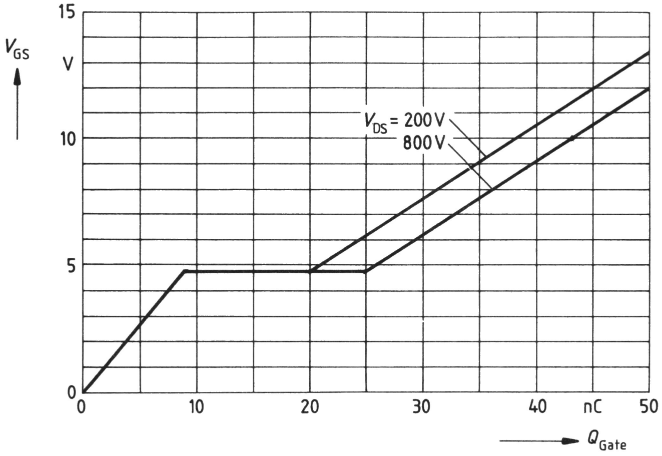


Fig. 14 *Typical gate-charge $V_{GS} = f(Q_{Gate})$*
Parameter: V_{DS}; $I_{DM} = 3{,}75$ A.

PowerMOS transistor

BUZ357

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

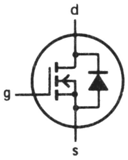
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	5,0	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,0	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



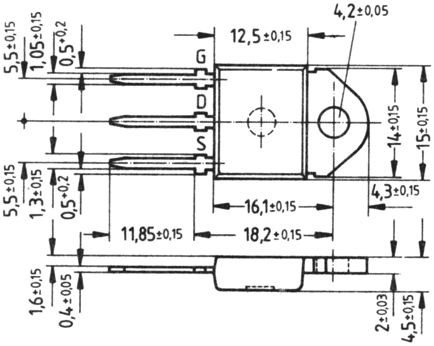

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
5,5±0,15
1,3±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
11,85±0,15
18,2±0,15
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 30 °C	–	5,0	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	3,2	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	20	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,2 A	–	1,7	2,0	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,2 A	1,4	3,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	180	300	pF
C_{rss}	Feedback capacitance		–	70	120	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,5 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	5,0	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	20	A
V_{SD}	Diode forward on-voltage	I_F = 10 A; V_{GS} = 0 V; T_j = 25 °C	–	1,05	1,3	V
t_{rr}	Reverse recovery time	I_F = 5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	2,0	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	30	–	µC

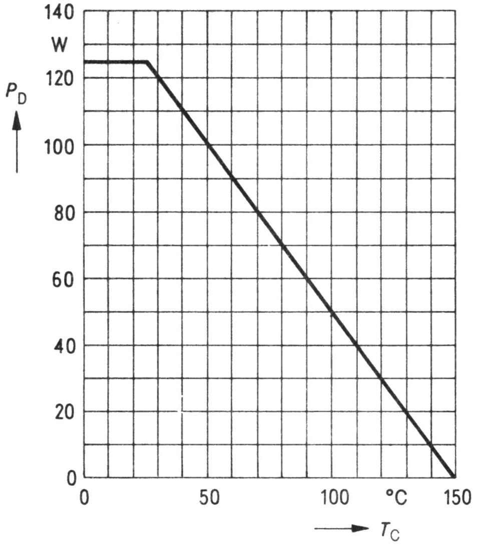


Fig. 2 *Power dissipation $P_D = f(T_{mb})$.*

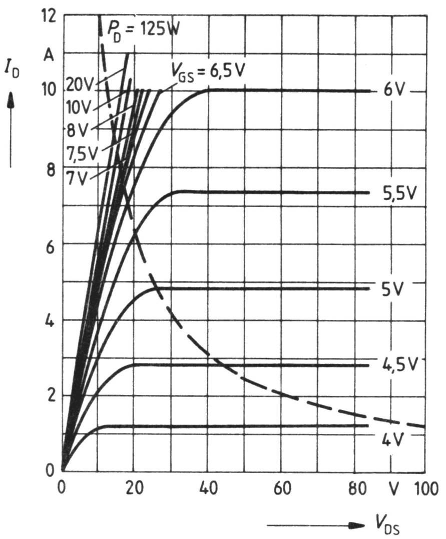


Fig. 3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 μs pulse test;
T_{mb} = 25 °C.

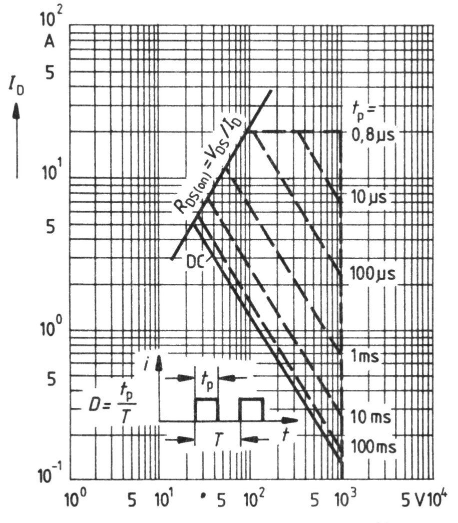


Fig. 4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

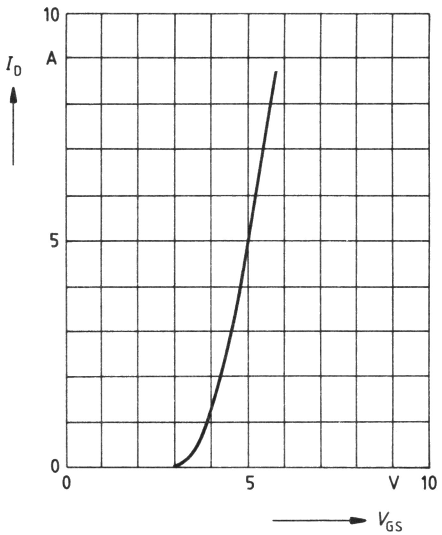


Fig. 5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 μs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

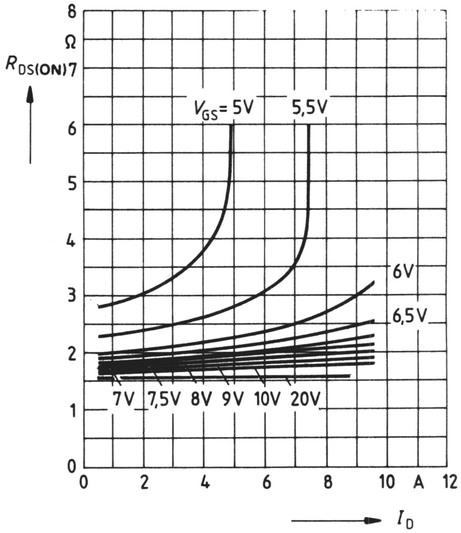


Fig.6 *Typical drain-source on-state resistance*
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

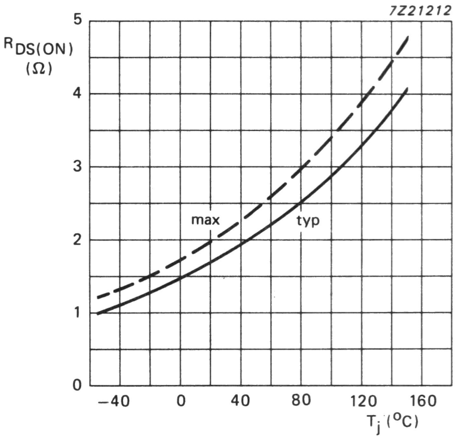


Fig. 7 *Drain-source on-state resistance*
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 3,2 A; V_{GS} = 10 V.

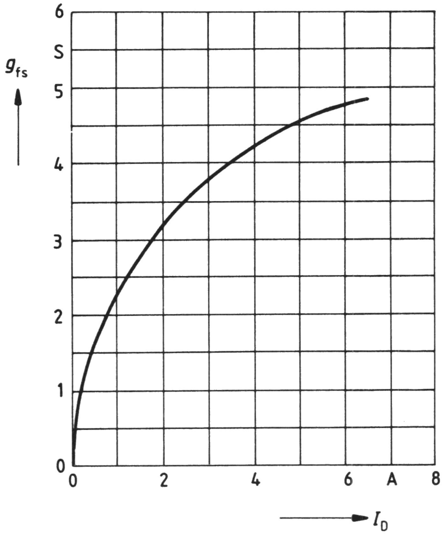


Fig.8 *Typical transconductance $g_{fs} = f(I_D)$*
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

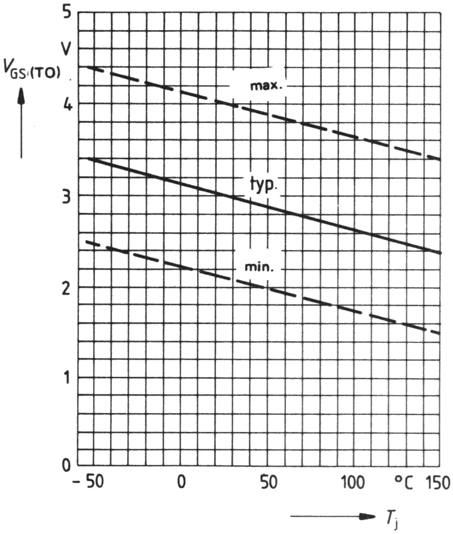


Fig.9 *Gate threshold voltage $V_{GS(TO)} = f(T_j)$*
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

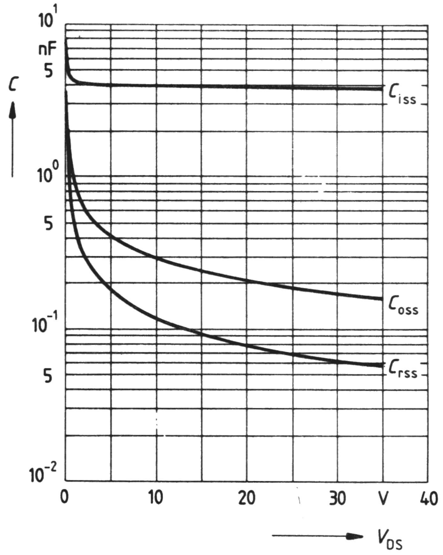


Fig. 10 *Typical capacitances $C = f(V_{DS})$*
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

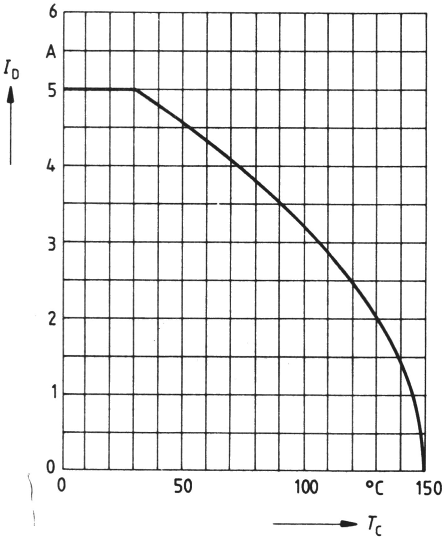


Fig. 11 *Continuous drain current $I_D = f(T_{mb})$*
Conditions: $V_{GS} \geq 10$ V.

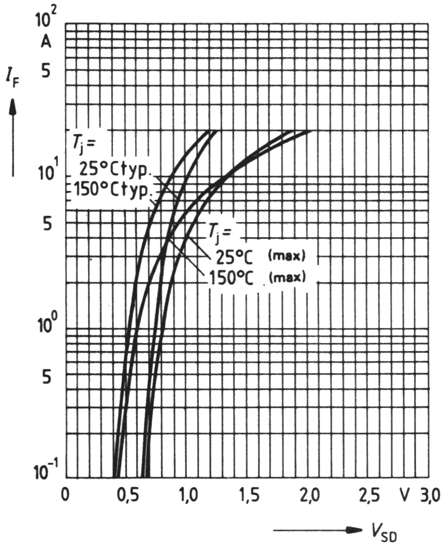


Fig. 12 *Forward characteristics of reverse diode*
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

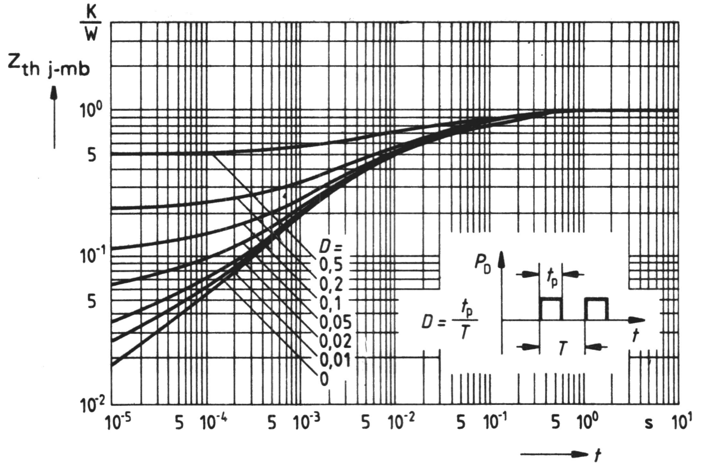


Fig. 13 *Transient thermal impedance* $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

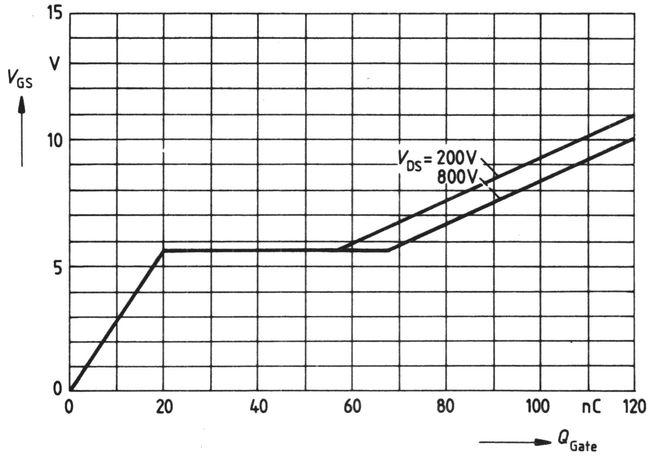


Fig. 14 *Typical gate-charge* $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 8{,}0$ *A.*

PowerMOS transistor BUZ358

May 1987

GENERAL DESCRIPTION

N-channel enchancement mode field-effect power transistor in a plastic envelope.

The device is intended for use in Switched Mode Power Supplies (SMPS), motor control, welding, DC/DC and DC/AC converters, and in general purpose switching applications.

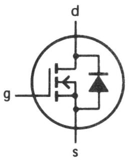
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	1000	V
I_D	Drain current (d.c.)	4,5	A
P_{tot}	Total power dissipation	125	W
$R_{DS(ON)}$	Drain-source on-state resistance	2,6	Ω

MECHANICAL DATA

Dimensions in mm

Net mass: 4,5 g



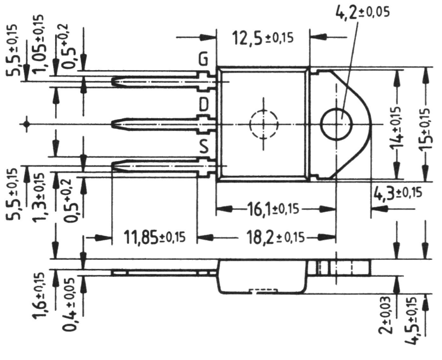

4,2±0,05
12,5±0,15
G
D
S
5,5±0,15
1,05±0,15
0,5+0,2
14±0,15
15±0,15
4,3±0,15
16,1±0,15
18,2±0,15
11,85±0,15
5,5±0,15
1,3±0,15
0,5+0,2
1,6±0,15
0,4±0,05
2±0,03
4,5±0,15

Fig.1 TO218AA; drain connected to mounting base.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Accessories supplied on request: refer to Mounting instructions for TO218AA envelopes.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	–	–	1000	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	–	1000	V
$\pm V_{GS}$	Gate-source voltage	–	–	20	V
I_D	Drain current (d.c.)	T_{mb} = 25 °C	–	4,5	A
I_D	Drain current (d.c.)	T_{mb} = 100 °C	–	2,8	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 °C	–	18	A
P_{tot}	Total power dissipation	T_{mb} = 25 °C	–	125	W
T_{stg}	Storage temperature	–	–55	150	°C
T_j	Junction temperature	–	–	150	°C

THERMAL RESISTANCES

From junction to mounting base	$R_{th\ j\text{-}mb}$ = 1,0 K/W
From junction to ambient	$R_{th\ j\text{-}a}$ = 45 K/W

STATIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0,25 mA	1000	–	–	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2,1	3,0	4,0	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 25 °C	–	20	250	μA
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1000 V; V_{GS} = 0 V; T_j = 125 °C	–	0,1	1,0	mA
I_{GSS}	Gate source leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	–	10	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 3,2 A	–	2,3	2,6	Ω

DYNAMIC CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 3,2 A	1,4	3,8	–	S
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	–	3900	5000	pF
C_{oss}	Output capacitance		–	180	300	pF
C_{rss}	Feedback capacitance		–	70	120	pF
$t_{d\ on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 2,4 A; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	–	60	90	ns
t_r	Turn-on rise time		–	90	140	ns
$t_{d\ off}$	Turn-off delay time		–	330	430	ns
t_f	Turn-off fall time		–	110	140	ns
L_d	Internal drain inductance	Measured from contact screw on tab to centre of die	–	5,0	–	nH
L_d	Internal drain inductance	Measured from drain lead 6 mm from package to centre of die	–	5,0	–	nH
L_s	Internal source inductance	Measured from source lead 6 mm from package to source bond pad	–	12,5	–	nH

REVERSE DIODE RATINGS AND CHARACTERISTICS

T_{mb} = 25 °C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	T_{mb} = 25 °C	–	–	4,5	A
I_{DRM}	Pulsed reverse drain current	T_{mb} = 25 °C	–	–	18	A
V_{SD}	Diode forward on-voltage	I_F = 9 A; V_{GS} = 0 V; T_j = 25 °C	–	1,0	1,3	V
t_{rr}	Reverse recovery time	I_F = 4,5 A; $-dI_F/dt$ = 100 A/µs; V_{GS} = 0 V; V_R = 100 V	–	2,0	–	ns
Q_{rr}	Reverse recovery charge	100 A/µs	–	30	–	µC

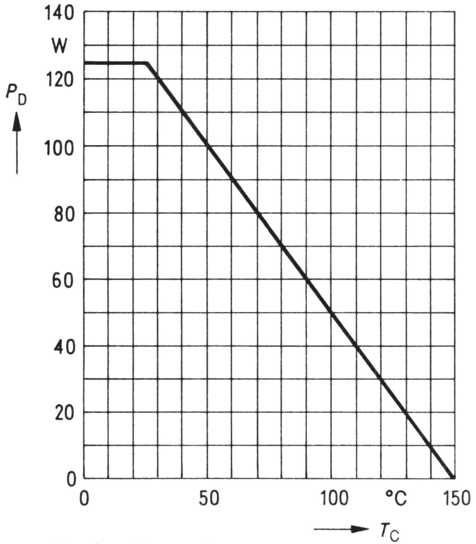


Fig.2 *Power dissipation $P_D = f(T_{mb})$.*

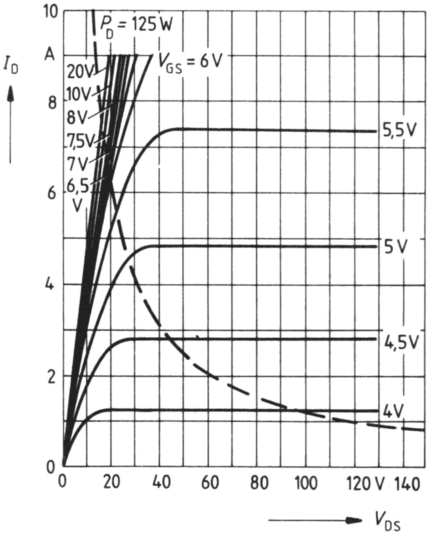


Fig.3 *Typical output characteristics $I_D = f(V_{DS})$*
Parameter: V_{GS}; 80 µs pulse test;
T_{mb} = 25 °C.

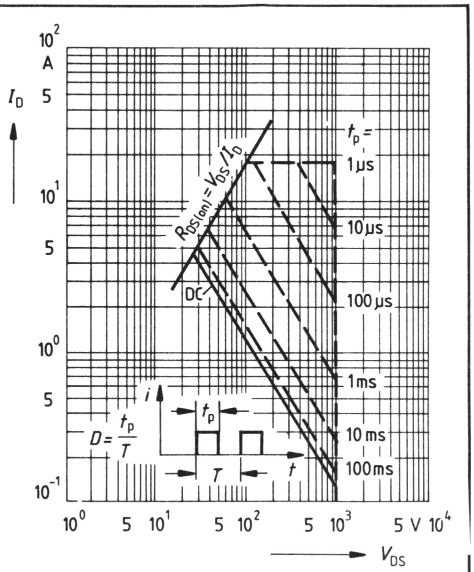


Fig.4 *Safe operating area I_D(DC) and*
$I_{DM} = f(V_{DS})$
Parameter: t_p; D = 0,01; T_{mb} = 25 °C.

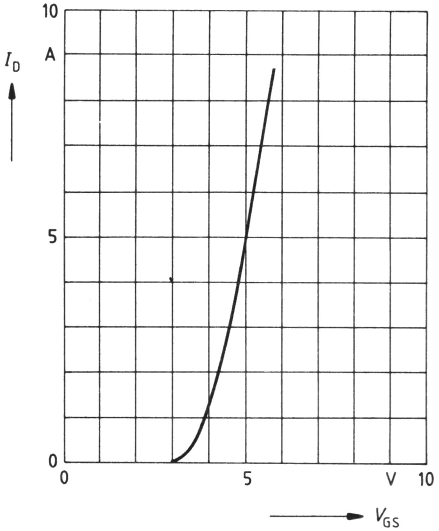


Fig.5 *Typical transfer characteristic $I_D = f(V_{GS})$*
Conditions: 80 µs pulse test; V_{DS} = 25 V,
T_{mb} = 25 °C.

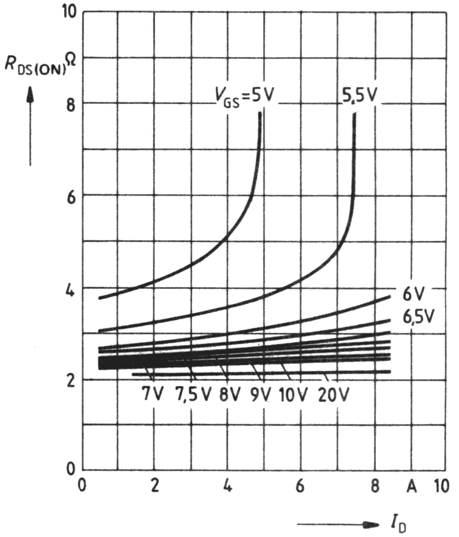


Fig.6 Typical drain-source on-state resistance
$R_{DS(ON)} = f(I_D)$
Parameter: V_{GS}; T_j = 25 °C.

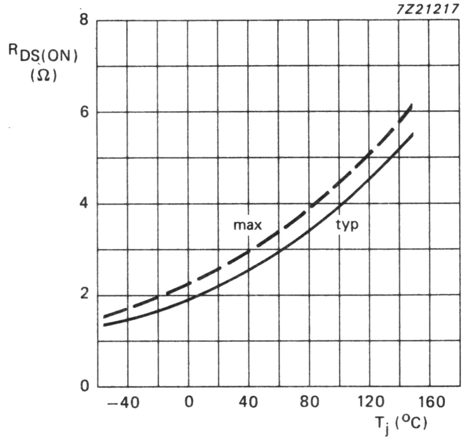


Fig. 7 Drain-source on-state resistance
$R_{DS(ON)} = f(T_j)$
Conditions: I_D = 3,2 A; V_{GS} = 10 V.

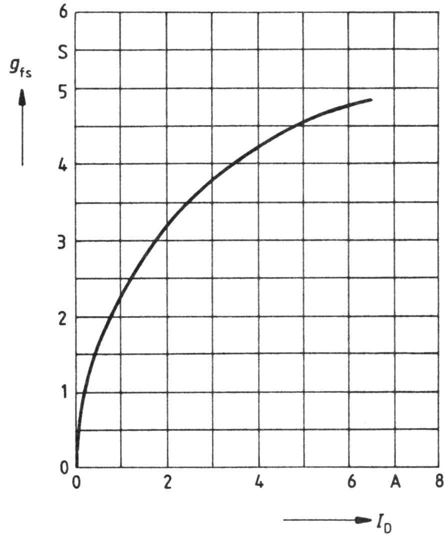


Fig.8 Typical transconductance $g_{fs} = f(I_D)$
Conditions: 80 µs pulse test;
V_{DS} = 25 V; T_j = 25 °C.

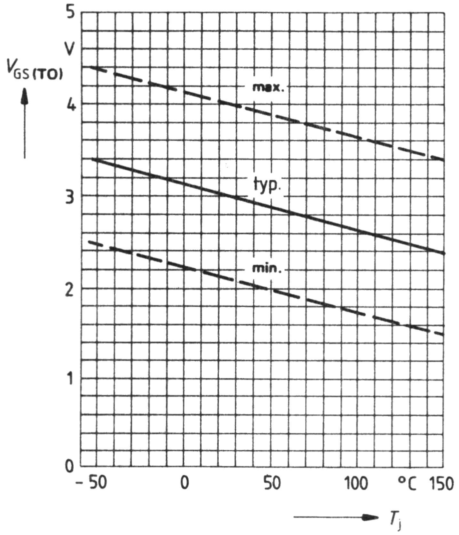


Fig. 9 Gate threshold voltage $V_{GS(TO)} = f(T_j)$
Conditions: $V_{DS} = V_{GS}$; I_D = 1 mA.

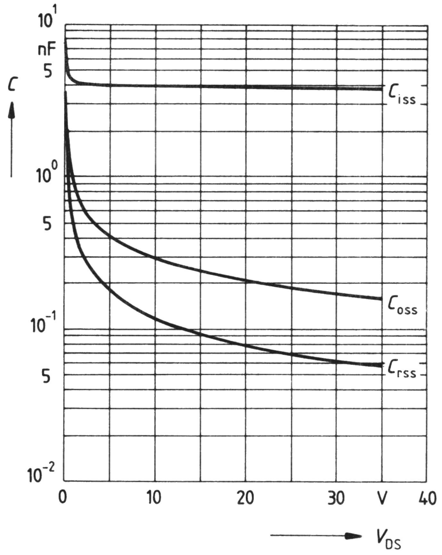


Fig.10 Typical capacitances $C = f(V_{DS})$
Conditions: $V_{GS} = 0$; $f = 1$ MHz.

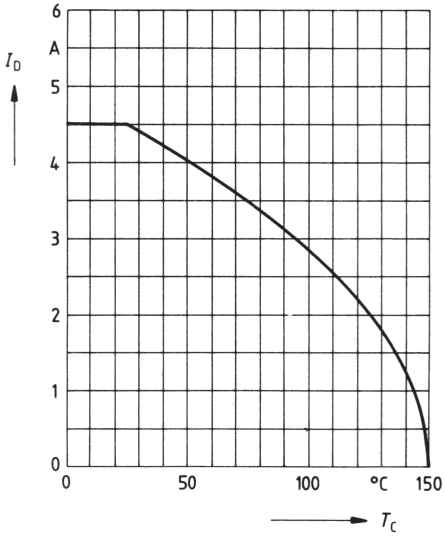


Fig.11 Continuous drain current $I_D = f(T_{mb})$
Conditions: $V_{GS} \geqslant 10$ V.

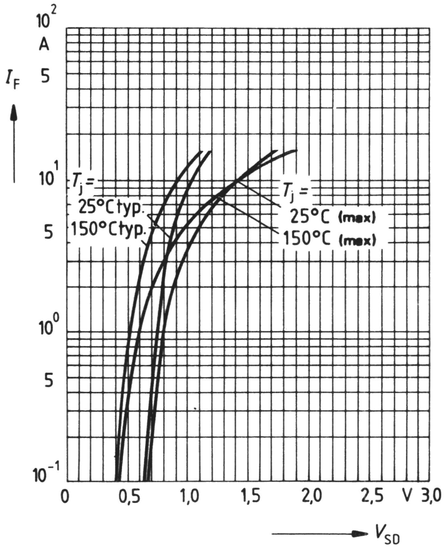


Fig.12 Forward characteristics of reverse diode
$I_F = f(V_{SD})$
Parameter: T_j; $t_p = 80$ µs.

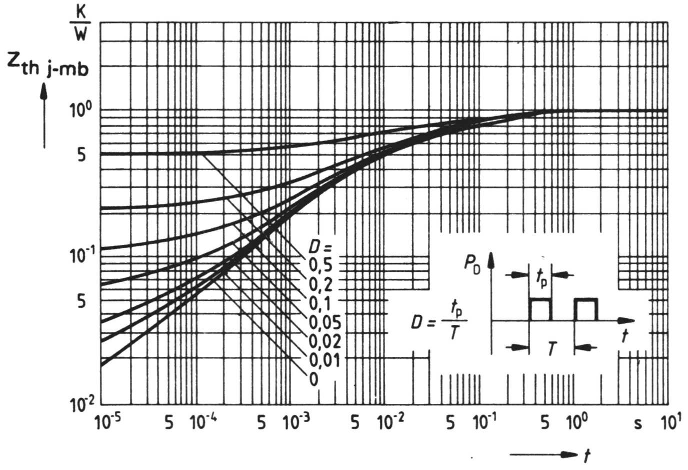


Fig.13 Transient thermal impedance $Z_{th\ j\text{-}mb} = f(t)$
Parameter: $D = t_p/T$.

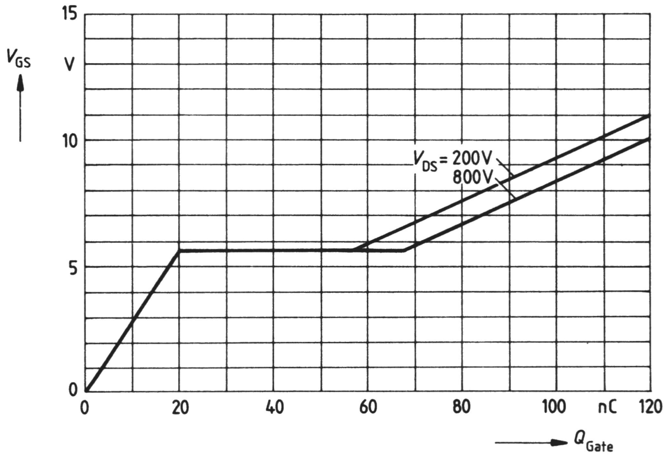


Fig.14 Typical gate-charge $V_{GS} = f(Q_{Gate})$
Parameter: V_{DS}; $I_{DM} = 8{,}0$ A.

INDEX OF ALL DEVICES IN SEMICONDUCTOR DATA HANDBOOKS

The inclusion of a type number in this publication does not necessarily imply its availability.

type no.	book	section	type no.	book	section	type no.	book	section
BA220	S1	SD	BAS29	S7/S1	Mm/SD	BAV99	S7/S1	Mm/SD
BA221	S1	SD	BAS31	S7/S1	Mm/SD	BAV100	S7/S1	Mm/SD
BA223	S1	T	BAS32	S7/S1	Mm/SD	BAV101	S7/S1	Mm/SD
BA281	S1	SD	BAS35	S7/S1	Mm/SD	BAV102	S7/S1	Mm/SD
BA314	S1	Vrg	BAS45	S1	SD	BAV103	S7/S1	Mm/SD
BA315	S1	Vrg	BAS56	S1/S7	SD/Mm	BAW56	S7/S1	Mm/SD
BA316	S1	SD	BAT17	S7/S1	Mm/T	BAW62	S1	SD
BA317	S1	SD	BAT18	S7/S1	Mm/T	BAX12	S1	SD
BA318	S1	SD	BAT54	S1/S7	SD/Mm	BAX14	S1	SD
BA423	S1	T	BAT74	S1/S7	SD/Mm	BAX18	S1	SD
BA480	S1	T	BAT81	S1	T	BAY80	S1	SD
BA481	S1	T	BAT82	S1	T	BB112	S1	T
BA482	S1	T	BAT83	S1	T	BB119	S1	T
BA483	S1	T	BAT85	S1	T	BB130	S1	T
BA484	S1	T	BAT86	S1	T	BB204B	S1	T
BA682	S1/S7	T/Mm	BAV10	S1	SD	BB204G	S1	T
BA683	S1/S7	T/Mm	BAV18	S1	SD	BB212	S1	T
BAS11	S1	SD	BAV19	S1	SD	BB215	S7/S1	Mm/SD
BAS15	S1	SD	BAV20	S1	SD	BB219	S7/S1	Mm/SD
BAS16	S7/S1	Mm/SD	BAV21	S1	SD	BB405B	S1	T
BAS17	S7/S1	Mm/Vrg	BAV23	S7/S1	Mm/SD	BB417	S1	T
BAS19	S7/S1	Mm/SD	BAV45	S1	Sp	BB809	S1	T
BAS20	S7/S1	Mm/SD	BAV45A	S1	Sp	BB909A	S1	T
BAS21	S7/S1	Mm/SD	BAV70	S7/S1	Mm/SD	BB909B	S1	T
BAS28	S7/S1	Mm/SD	BAV74	S1	SD	BBY31	S7/S1	Mm/T

Mm = Microminiature semiconductors for hybrid circuits
SD = Small-signal diodes
Sp = Special diodes
T = Tuner diodes
Vrg = Voltage regulator diodes
* = series
FET = Field-effect transistors
P = Low-frequency power transistors
Sm = Small-signal transistors
RFP = R.F. power transistors and modules
RT = Tripler
Th = Thyristors
ThM = Thyristor modules
WBM = Wideband hybrid IC modules
WBT = Wideband transistors

HVP = High-voltage power transistors
PDT = Photodiodes or transistors
PM = PowerMOS transistors
R = Rectifier diodes
SP = Low-frequency switching power transistors
Tri = Triacs
I = Infrared devices
LED = Light-emitting diodes
M = Microwave transistors
PhC = Photocouplers
SEN = Sensors
Ph = Photoconductive devices
TS = Transient suppressor diodes
Vrf = Voltage reference diodes
St = Rectifier stacks

type no.	book	section
BBY39	S1	T
BBY40	S7/S1	Mm/T
BC107	S3	Sm
BC108	S3	Sm
BC109	S3	Sm
BC140	S3	Sm
BC141	S3	Sm
BC160	S3	Sm
BC161	S3	Sm
BC177	S3	Sm
BC178	S3	Sm
BC179	S3	Sm
BC264A	S5	FET
BC264B	S5	FET
BC264C	S5	FET
BC264D	S5	FET
BC327;A	S3	Sm
BC328	S3	Sm
BC337;A	S3	Sm
BC338	S3	Sm
BC368	S3	Sm
BC369	S3	Sm
BC375	S3	Sm
BC376	S3	Sm
BC516	S3	Sm
BC517	S3	Sm
BC546	S3	Sm
BC547	S3	Sm
BC548	S3	Sm
BC549	S3	Sm
BC550	S3	Sm
BC556	S3	Sm
BC557	S3	Sm
BC558	S3	Sm
BC559	S3	Sm
BC560	S3	Sm
BC635	S3	Sm
BC636	S3	Sm
BC637	S3	Sm
BC638	S3	Sm
BC639	S3	Sm
BC640	S3	Sm
BC807	S7	Mm
BC808	S7	Mm
BC817	S7	Mm
BC818	S7	Mm
BC846	S7	Mm
BC847	S7	Mm
BC848	S7	Mm
BC849	S7	Mm
BC850	S7	Mm
BC856	S7	Mm
BC857	S7	Mm
BC858	S7	Mm
BC859	S7	Mm
BC860	S7	Mm
BC868	S7	Mm
BC869	S7	Mm
BCF29;R	S7	Mm
BCF30;R	S7	Mm
BCF32;R	S7	Mm
BCF33;R	S7	Mm
BCF70;R	S7	Mm
BCF81;R	S7	Mm
BCV26	S7	Mm
BCV27	S7	Mm
BCV61	S7	Mm
BCV62	S7	Mm
BCV63	S7	Mm
BCV64	S7	Mm
BCV65	S7	Mm
BCV71;R	S7	Mm
BCV72;R	S7	Mm
BCW29;R	S7	Mm
BCW30;R	S7	Mm
BCW31;R	S7	Mm
BCW32;R	S7	Mm
BCW33;R	S7	Mm
BCW60*	S7	Mm
BCW61*	S7	Mm
BCW69;R	S7	Mm
BCW70;R	S7	Mm
BCW71;R	S7	Mm
BCW72;R	S7	Mm
BCW81;R	S7	Mm
BCW89;R	S7	Mm
BCX17;R	S7	Mm
BCX18;R	S7	Mm
BCX19;R	S7	Mm
BCX20;R	S7	Mm
BCX51	S7	Mm
BCX52	S7	Mm
BCX53	S7	Mm
BCX54	S7	Mm
BCX55	S7	Mm
BCX56	S7	Mm
BCX58	S3	Sm
BCX59	S3	Sm
BCX70*	S7	Mm
BCX71*	S7	Mm
BCX78	S3	Sm
BCX79	S3	Sm
BCY56	S3	Sm
BCY57	S3	Sm
BCY58	S3	Sm
BCY59	S3	Sm
BCY65	S3	Sm
BCY70	S3	Sm
BCY71	S3	Sm
BCY72	S3	Sm
BCY78	S3	Sm
BCY79	S3	Sm
BCY87	S3	Sm
BCY88	S3	Sm
BCY89	S3	Sm
BD131	S4a	P
BD132	S4a	P
BD135	S4a	P
BD136	S4a	P
BD137	S4a	P

type no.	book	section
BD138	S4a	P
BD139	S4a	P
BD140	S4a	P
BD201	S4a	P
BD202	S4a	P
BD203	S4a	P
BD204	S4a	P
BD226	S4a	P
BD227	S4a	P
BD228	S4a	P
BD229	S4a	P
BD230	S4a	P
BD231	S4a	P
BD233	S4a	P
BD234	S4a	P
BD235	S4a	P
BD236	S4a	P
BD237	S4a	P
BD238	S4a	P
BD239	S4a	P
BD239A	S4a	P
BD239B	S4a	P
BD239C	S4a	P
BD240	S4a	P
BD240A	S4a	P
BD240B	S4a	P
BD240C	S4a	P
BD241	S4a	P
BD241A	S4a	P
BD241B	S4a	P
BD241C	S4a	P
BD242	S4a	P
BD242A	S4a	P
BD242B	S4a	P
BD242C	S4a	P
BD243	S4a	P
BD243A	S4a	P
BD243B	S4a	P
BD243C	S4a	P
BD244	S4a	P
BD244A	S4a	P
BD244B	S4a	P
BD244C	S4a	P
BD329	S4a	P
BD330	S4a	P
BD331	S4a	P
BD332	S4a	P
BD333	S4a	P
BD334	S4a	P
BD335	S4a	P
BD336	S4a	P
BD337	S4a	P
BD338	S4a	P
BD433	S4a	P
BD434	S4a	P
BD435	S4a	P
BD436	S4a	P
BD437	S4a	P
BD438	S4a	P
BD645	S4a	P
BD646	S4a	P
BD647	S4a	P
BD648	S4a	P
BD649	S4a	P
BD650	S4a	P
BD651	S4a	P
BD652	S4a	P
BD675	S4a	P
BD676	S4a	P
BD677	S4a	P
BD678	S4a	P
BD679	S4a	P
BD680	S4a	P
BD681	S4a	P
BD682	S4a	P
BD683	S4a	P
BD684	S4a	P
BD813	S4a	P
BD814	S4a	P
BD815	S4a	P
BD816	S4a	P
BD817	S4a	P
BD818	S4a	P
BD825	S4a	P
BD826	S4a	P
BD827	S4a	P
BD828	S4a	P
BD829	S4a	P
BD830	S4a	P
BD839	S4a	P
BD840	S4a	P
BD841	S4a	P
BD842	S4a	P
BD843	S4a	P
BD844	S4a	P
BD845	S4a	P
BD846	S4a	P
BD847	S4a	P
BD848	S4a	P
BD849	S4a	P
BD850	S4a	P
BD933	S4a	P
BD934	S4a	P
BD935	S4a	P
BD936	S4a	P
BD937	S4a	P
BD938	S4a	P
BD939	S4a	P
BD940	S4a	P
BD941	S4a	P
BD942	S4a	P
BD943	S4a	P
BD944	S4a	P
BD945	S4a	P
BD946	S4a	P
BD947	S4a	P
BD948	S4a	P
BD949	S4a	P
BD950	S4a	P
BD951	S4a	P

type no.	book	section
BD952	S4a	P
BD953	S4a	P
BD954	S4a	P
BD955	S4a	P
BD956	S4a	P
BDT20	S4a	P
BDT21	S4a	P
BDT29	S4a	P
BDT29A	S4a	P
BDT29B	S4a	P
BDT29C	S4a	P
BDT30	S4a	P
BDT30A	S4a	P
BDT30B	S4a	P
BDT30C	S4a	P
BDT31	S4a	P
BDT31A	S4a	P
BDT31B	S4a	P
BDT31C	S4a	P
BDT32	S4a	P
BDT32A	S4a	P
BDT32B	S4a	P
BDT32C	S4a	P
BDT41	S4a	P
BDT41A	S4a	P
BDT41B	S4a	P
BDT41C	S4a	P
BDT42	S4a	P
BDT42A	S4a	P
BDT42B	S4a	P
BDT42C	S4a	P
BDT51	S4a	P
BDT52	S4a	P
BDT53	S4a	P
BDT54	S4a	P
BDT55	S4a	P
BDT56	S4a	P
BDT57	S4a	P
BDT58	S4a	P
BDT60	S4a	P
BDT60A	S4a	P
BDT60B	S4a	P
BDT60C	S4a	P
BDT61	S4a	P
BDT61A	S4a	P
BDT61B	S4a	P
BDT61C	S4a	P
BDT62	S4a	P
BDT62A	S4a	P
BDT62B	S4a	P
BDT62C	S4a	P
BDT63	S4a	P
BDT63A	S4a	P
BDT63B	S4a	P
BDT63C	S4a	P
BDT64	S4a	P
BDT64A	S4a	P
BDT64B	S4a	P
BDT64C	S4a	P
BDT65	S4a	P
BDT65A	S4a	P
BDT65B	S4a	P
BDT65C	S4a	P
BDT81	S4a	P
BDT82	S4a	P
BDT83	S4a	P
BDT84	S4a	P
BDT85	S4a	P
BDT86	S4a	P
BDT87	S4a	P
BDT88	S4a	P
BDT91	S4a	P
BDT92	S4a	P
BDT93	S4a	P
BDT94	S4a	P
BDT95	S4a	P
BDT96	S4a	P
BDV64	S4a	P
BDV64A	S4a	P
BDV64B	S4a	P
BDV64C	S4a	P
BDV65	S4a	P
BDV65A	S4a	P
BDV65B	S4a	P
BDV65C	S4a	P
BDV66A	S4a	P
BDV66B	S4a	P
BDV66C	S4a	P
BDV66D	S4a	P
BDV67A	S4a	P
BDV67B	S4a	P
BDV67C	S4a	P
BDV67D	S4a	P
BDV91	S4a	P
BDV92	S4a	P
BDV93	S4a	P
BDV94	S4a	P
BDV95	S4a	P
BDV96	S4a	P
BDW55	S4a	P
BDW56	S4a	P
BDW57	S4a	P
BDW58	S4a	P
BDW59	S4a	P
BDW60	S4a	P
BDX35	S4a	P
BDX36	S4a	P
BDX37	S4a	P
BDX42	S4a	P
BDX43	S4a	P
BDX44	S4a	P
BDX45	S4a	P
BDX46	S4a	P
BDX47	S4a	P
BDX62	S4a	P
BDX62A	S4a	P
BDX62B	S4a	P
BDX62C	S4a	P
BDX63	S4a	P
BDX63A	S4a	P

type no.	book	section
BDX63B	S4a	P
BDX63C	S4a	P
BDX64	S4a	P
BDX64A	S4a	P
BDX64B	S4a	P
BDX64C	S4a	P
BDX65	S4a	P
BDX65A	S4a	P
BDX65B	S4a	P
BDX65C	S4a	P
BDX66	S4a	P
BDX66A	S4a	P
BDX66B	S4a	P
BDX66C	S4a	P
BDX67	S4a	P
BDX67A	S4a	P
BDX67B	S4a	P
BDX67C	S4a	P
BDX68	S4a	P
BDX68A	S4a	P
BDX68B	S4a	P
BDX68C	S4a	P
BDX69	S4a	P
BDX69A	S4a	P
BDX69B	S4a	P
BDX69C	S4a	P
BDX77	S4a	P
BDX78	S4a	P
BDX91	S4a	P
BDX92	S4a	P
BDX93	S4a	P
BDX94	S4a	P
BDX95	S4a	P
BDX96	S4a	P
BDY90	S4a	P
BDY90A	S4a	P
BDY91	S4a	P
BDY92	S4a	P
BF198	S3	Sm
BF199	S3	Sm
BF240	S3	Sm
BF241	S3	Sm
BF245A	S5	FET
BF245B	S5	FET
BF245C	S5	FET
BF247A	S5	FET
BF247B	S5	FET
BF247C	S5	FET
BF256A	S5	FET
BF256B	S5	FET
BF256C	S5	FET
BF324	S3	Sm
BF370	S3	Sm
BF410A	S5	FET
BF410B	S5	FET
BF410C	S5	FET
BF410D	S5	FET
BF419	S4b	HVP
BF420	S3	Sm
BF421	S3	Sm
BF422	S3	Sm
BF423	S3	Sm
BF450	S3	Sm
BF451	S3	Sm
BF457	S4b	HVP
BF458	S4b	HVP
BF459	S4b	HVP
BF469	S4b	HVP
BF470	S4b	HVP
BF471	S4b	HVP
BF472	S4b	HVP
BF483	S3	Sm
BF485	S3	Sm
BF487	S3	Sm
BF494	S3	Sm
BF495	S3	Sm
BF496	S3	Sm
BF510	S7/S5	Mm/FET
BF511	S7/S5	Mm/FET
BF512	S7/S5	Mm/FET
BF513	S7/S5	Mm/FET
BF536	S7	Mm
BF550;R	S7	Mm
BF569	S7	Mm
BF570	S7	Mm
BF579	S7	Mm
BF583	S4b	HVP
BF585	S4b	HVP
BF587	S4b	HVP
BF591	S4b	HVP
BF593	S4b	HVP
BF620	S7	Mm
BF621	S7	Mm
BF622	S7	Mm
BF623	S7	Mm
BF660;R	S7	Mm
BF689K	S10	WBT
BF763	S10	WBT
BF767	S7	Mm
BF819	S4b	HVP
BF820	S7	Mm
BF821	S7	Mm
BF822	S7	Mm
BF823	S7	Mm
BF824	S7	Mm
BF840	S7	Mm
BF841	S7	Mm
BF857	S4b	HVP
BF858	S4b	HVP
BF859	S4b	HVP
BF869	S4b	HVP
BF870	S4b	HVP
BF871	S4b	HVP
BF872	S4b	HVP
BF926	S3	Sm
BF936	S3	Sm
BF939	S3	Sm
BF960	S5	FET
BF964	S5	FET
BF966	S5	FET

type no.	book	section
BF967	S3	Sm
BF970	S3	Sm
BF970A	S3	Sm
BF979	S3	Sm
BF980	S5	FET
BF981	S5	FET
BF982	S5	FET
BF989	S7/S5	Mm/FET
BF990	S7/S5	Mm/FET
BF991	S7/S5	Mm/FET
BF992	S7/S5	Mm/FET
BF994	S7/S5	Mm/FET
BF994S	S7	Mm/FET
BF996	S7/S5	Mm/FET
BF996S	S7	Mm/FET
BF997	S7	Mm/FET
BFG23	S10	WBT
BFG32	S10	WBT
BFG34	S10	WBT
BFG51	S10	WBT
BFG65	S10	WBT
BFG67	S7/S10	Mm
BFG90A	S10	WBT
BFG91A	S10	WBT
BFG92A	S10	WBT
BFG93A	S10	WBT
BFG96	S10	WBT
BFG195	S10	WBT
BFP90A	S10	WBT
BFP91A	S10	WBT
BFP96	S10	WBT
BFQ10	S5	FET
BFQ11	S5	FET
BFQ12	S5	FET
BFQ13	S5	FET
BFQ14	S5	FET
BFQ15	S5	FET
BFQ16	S5	FET
BFQ17	S7/S10	Mm/WBT
BFQ18A	S7/S10	Mm/WBT
BFQ19	S7/S10	Mm/WBT
BFQ22S	S10	WBT
BFQ23	S10	WBT
BFQ23C	S10	WBT
BFQ24	S10	WBT
BFQ32	S10	WBT
BFQ32C	S10	WBT
BFQ32M	S10	WBT
BFQ32S	S10	WBT
BFQ33	S10	WBT
BFQ33C	S10	WBT
BFQ34	S10	WBT
BFQ34T	S10	WBT
BFQ42	S6	RFP
BFQ43	S6	RFP
BFQ43S	S6	RFP
BFQ51	S10	WBT
BFQ51C	S10	WBT
BFQ52	S10	WBT
BFQ53	S10	WBT
BFQ63	S10	WBT
BFQ65	S10	WBT
BFQ66	S10	WBT
BFQ67	S7/S10	Mm/WBT
BFQ68	S10	WBT
BFQ136	S10	WBT
BFR29	S5	FET
BFR30	S7/S5	Mm/FET
BFR31	S7/S5	Mm/FET
BFR49	S10	WBT
BFR53	S7/S10	Mm/WBT
BFR54	S3	Sm
BFR64	S10	WBT
BFR65	S10	WBT
BFR84	S5	FET
BFR90	S10	WBT
BFR90A	S10	WBT
BFR91	S10	WBT
BFR91A	S10	WBT
BFR92	S7/S10	Mm/WBT
BFR92A	S7/S10	Mm
BFR93	S7/S10	Mm/WBT
BFR93A	S7/S10	Mm/WBT
BFR94	S10	WBT
BFR95	S10	WBT
BFR96	S10	WBT
BFR96S	S10	WBT
BFR101A;B	S7/S5	Mm/FET
BFS17	S7/S10	Mm/WBT
BFS17A	S10	WBT
BFS18;R	S7	Mm
BFS19;R	S7	Mm
BFS20;R	S7	Mm
BFS21	S5	FET
BFS21A	S5	FET
BFS22A	S6	RFP
BFS23A	S6	RFP
BFT24	S10	WBT
BFT25	S7/S10	Mm/WBT
BFT25R	S7	Mm
BFT44	S3	Sm
BFT45	S3	Sm
BFT46	S7/S5	Mm/FET
BFT92	S7/S10	Mm/WBT
BFT93	S7/S10	Mm/WBT
BFW10	S5	FET
BFW11	S5	FET
BFW12	S5	FET
BFW13	S5	FET
BFW16A	S10	WBT
BFW17A	S10	WBT
BFW30	S10	WBT
BFW61	S5	FET
BFW92	S10	WBT
BFW92A	S10	WBT
BFW93	S10	WBT
BFX34	S3	Sm
BFX89	S10	WBT
BFY50	S3	Sm
BFY51	S3	Sm

type no.	book	section
BFY52	S3	Sm
BFY55	S3	Sm
BFY90	S10	WBT
BG2000	S1	RT
BG2097	S1	RT
BGD102	S10	WBM
BGD102E	S10	WBM
BGD104	S10	WBM
BGD104E	S10	WBM
BGD502	S10	WBM
BGD504	S10	WBM
BGX885	S10	WBM
BGY22	S6	RFP
BGY22A	S6	RFP
BGY23	S6	RFP
BGY23A	S6	RFP
BGY32	S6	RFP
BGY33	S6	RFP
BGY35	S6	RFP
BGY36	S6	RFP
BGY40A	S6	RFP
BGY40B	S6	RFP
BGY41A	S6	RFP
BGY41B	S6	RFP
BGY43	S6	RFP
BGY45A	S6	RFP
BGY45B	S6	RFP
BGY46A	S6	RFP
BGY46B	S6	RFP
BGY47 *	S6	RFP
BGY48 *	S6	RFP
BGY50	S10	WBM
BGY51	S10	WBM
BGY52	S10	WBM
BGY53	S10	WBM
BGY54	S10	WBM
BGY55	S10	WBM
BGY56	S10	WBM
BGY57	S10	WBM
BGY58	S10	WBM
BGY58A	S10	WBM
BGY59	S10	WBM
BGY60	S10	WBM
BGY61	S10	WBM
BGY65	S10	WBM
BGY67	S10	WBM
BGY67A	S10	WBM
BGY70	S10	WBM
BGY71	S10	WBM
BGY74	S10	WBM
BGY75	S10	WBM
BGY78	S10	WBM
BGY84	S10	WBM
BGY84A	S10	WBM
BGY85	S10	WBM
BGY85A	S10	WBM
BGY86	S10	WBM
BGY87	S10	WBM
BGY88	S10	WBM
BGY90A	S6	RFP
BGY90B	S6	RFP
BGY93 *	S6	RFP
BGY94 *	S6	RFP
BGY95A	S6	RFP
BGY95B	S6	RFP
BGY96A	S6	RFP
BGY96B	S6	RFP
BGY584A	S10	WBM
BGY585A	S10	WBM
BGY586	S10	WBM
BGY587	S10	WBM
BLF146	S6	RFP/FET
BLF242	S6	RFP/FET
BLF244	S6	RFP/FET
BLF245	S6	RFP/FET
BLT90/SL	S6	RFP
BLT91/SL	S6	RFP
BLT92/SL	S6	RFP
BLU20/12	S6	RFP
BLU30/12	S6	RFP
BLU45/12	S6	RFP
BLU50	S6	RFP
BLU51	S6	RFP
BLU52	S6	RFP
BLU53	S6	RFP
BLU60/12	S6	RFP
BLU97	S6	RFP
BLU98	S6	RFP
BLU99	S6	RFP
BLV10	S6	RFP
BLV11	S6	RFP
BLV20	S6	RFP
BLV21	S6	RFP
BLV25	S6	RFP
BLV30	S6	RFP
BLV30/12	S6	RFP
BLV31	S6	RFP
BLV32F	S6	RFP
BLV33	S6	RFP
BLV33F	S6	RFP
BLV36	S6	RFP
BLV45/12	S6	RFP
BLV57	S6	RFP
BLV59	S6	RFP
BLV75/12	S6	RFP
BLV80/28	S6	RFP
BLV90	S6	RFP
BLV90/SL	S6	RFP
BLV91	S6	RFP
BLV91/SL	S6	RFP
BLV92	S6	RFP
BLV93	S6	RFP
BLV94	S6	RFP
BLV95	S6	RFP
BLV97	S6	RFP
BLV98	S6	RFP
BLV99	S6	RFP
BLW29	S6	RFP
BLW31	S6	RFP
BLW32	S6	RFP

type no.	book	section
BLW33	S6	RFP
BLW34	S6	RFP
BLW50F	S6	RFP
BLW60	S6	RFP
BLW60C	S6	RFP
BLW76	S6	RFP
BLW77	S6	RFP
BLW78	S6	RFP
BLW79	S6	RFP
BLW80	S6	RFP
BLW81	S6	RFP
BLW83	S6	RFP
BLW84	S6	RFP
BLW85	S6	RFP
BLW86	S6	RFP
BLW87	S6	RFP
BLW89	S6	RFP
BLW90	S6	RFP
BLW91	S6	RFP
BLW95	S6	RFP
BLW96	S6	RFP
BLW97	S6	RFP
BLW98	S6	RFP
BLW99	S6	RFP
BLX13	S6	RFP
BLX13C	S6	RFP
BLX14	S6	RFP
BLX15	S6	RFP
BLX39	S6	RFP
BLX65	S6	RFP
BLX65E	S6	RFP
BLX65ES	S6	RFP
BLX67	S6	RFP
BLX68	S6	RFP
BLX69A	S6	RFP
BLX91A	S6	RFP
BLX91CB	S6	RFP
BLX92A	S6	RFP
BLX93A	S6	RFP
BLX94A	S6	RFP
BLX94C	S6	RFP
BLX95	S6	RFP
BLX96	S6	RFP
BLX97	S6	RFP
BLX98	S6	RFP
BLY87A	S6	RFP
BLY87C	S6	RFP
BLY88A	S6	RFP
BLY88C	S6	RFP
BLY89A	S6	RFP
BLY89C	S6	RFP
BLY90	S6	RFP
BLY91A	S6	RFP
BLY91C	S6	RFP
BLY92A	S6	RFP
BLY92C	S6	RFP
BLY93A	S6	RFP
BLY93C	S6	RFP
BLY94	S6	RFP
BPF24	S8b	PDT
BPW22A	S8a/b	PDT
BPW50	S8a/b	PDT
BPW71	S8b	PDT
BPX25	S8b	PDT
BPX29	S8b	PDT
BPX40	S8b	PDT
BPX41	S8b	PDT
BPX42	S8b	PDT
BPX61	S8b	PDT
BPX61P	S8b	PDT
BPX71	S8b	PDT
BPX72	S8b	PDT
BR100/03	S2b	Th
BR101	S3	Sm
BR210*	S2a	Th
BR216*	S2a	Th
BR220*	S2a	Th
BRY39	S3	Sm
BRY56	S3	Sm
BRY61	S7	Mm
BRY62	S7	Mm
BS107	S5	FET
BS170	S5	FET
BSD10	S5	FET
BSD12	S5	FET
BSD20	S5/7	FET
BSD22	S5/7	FET
BSD212	S5	FET
BSD213	S5	FET
BSD214	S5	FET
BSD215	S5	FET
BSR12;R	S7	Mm
BSR13;R	S7	Mm
BSR14;R	S7	Mm
BSR15;R	S7	Mm
BSR16;R	S7	Mm
BSR17;R	S7	Mm
BSR17A;R	S7	Mm
BSR18;R	S7	Mm
BSR18A;R	S7	Mm
BSR19; A	S7	Mm
BSR20; A	S7	Mm
BSR30	S7	Mm
BSR31	S7	Mm
BSR32	S7	Mm
BSR33	S7	Mm
BSR40	S7	Mm
BSR41	S7	Mm
BSR42	S7	Mm
BSR43	S7	Mm
BSR50	S3	Sm
BSR51	S3	Sm
BSR52	S3	Sm
BSR56	S7/S5	Mm/FET
BSR57	S7/S5	Mm/FET
BSR58	S7/S5	Mm/FET
BSR60	S3	Sm
BSR61	S3	Sm
BSR62	S3	Sm
BSS38	S3	Sm

type no.	book	section
BSS50	S3	Sm
BSS51	S3	Sm
BSS52	S3	Sm
BSS60	S3	Sm
BSS61	S3	Sm
BSS62	S3	Sm
BSS63;R	S7	Mm
BSS64;R	S7	Mm
BSS68	S3	Sm
BSS83	S5/7	FET/Mm
BST15	S7	Mm
BST16	S7	Mm
BST39	S7	Mm
BST40	S7	Mm
BST50	S7	Mm
BST51	S7	Mm
BST52	S7	Mm
BST60	S7	Mm
BST61	S7	Mm
BST62	S7	Mm
BST70A	S5	FET
BST72A	S5	FET
BST74A	S5	FET
BST76A	S5	FET
BST78	S5	FET
BST80	S5/S7	FET/Mm
BST82	S5/S7	FET/Mm
BST84	S5/S7	FET/Mm
BST86	S5/S7	FET/Mm
BST90	S5	FET
BST97	S5	FET
BST100	S5	FET
BST110	S5	FET
BST120	S5/S7	FET/Mm
BST122	S5/S7	FET/Mm
BSV15	S3	Sm
BSV16	S3	Sm
BSV17	S3	Sm
BSV52;R	S7	Mm
BSV64	S3	Sm
BSV78	S5	FET
BSV79	S5	FET
BSV80	S5	FET
BSV81	S5	FET
BSW66A	S3	Sm
BSW67A	S3	Sm
BSW68A	S3	Sm
BSX19	S3	Sm
BSX20	S3	Sm
BSX32	S3	Sm
BSX45	S3	Sm
BSX46	S3	Sm
BSX47	S3	Sm
BSX59	S3	Sm
BSX60	S3	Sm
BSX61	S3	Sm
BT136*	S2b	Tri
BT136F*	S2b	Tri
BT137*	S2b	Tri
BT137F*	S2b	Tri
BT138*	S2b	Tri
BT138F*	S2b	Tri
BT139*	S2b	Tri
BT139F*	S2b	Tri
BT145*	S2b	Tri
BT149*	S2b	Th
BT150	S2b	Th
BT151*	S2b	Th
BT151F*	S2b	Th
BT152*	S2b	Th
BT153	S2b	Th
BT157*	S2b	Th
BT169*	S2b	Th
BTA140*	S2b	Tri
BTR59*	S2b	Tri
BTS59*	S2b	Tri
BTV58*	S2b	Th
BTV59*	S2b	Th
BTV59D*	S2b	Th
BTV60*	S2b	Th
BTV60D*	S2b	Th
BTV70*	S2b	Th
BTV70D*	S2b	Th
BTW23*	S2b	Th
BTW38*	S2b	Th
BTW40*	S2b	Th
BTW42*	S2b	Th
BTW43*	S2b	Tri
BTW45*	S2b	Th
BTW58*	S2b	Th
BTW62*	S2b	Th
BTW62D*	S2b	Th
BTW63*	S2b	Th
BTY79*	S2b	Th
BTY91*	S2b	Th
BU426	S4b	SP
BU426A	S4b	SP
BU433	S4b	SP
BU505	S4b	SP
BU506	S4b	SP
BU506D	S4b	SP
BU508A	S4b	SP
BU508D	S4b	SP
BU705	S4b	SP
BU706	S4b	SP
BU706D	S4b	SP
BU806	S4b	SP
BU807	S4b	SP
BU808	S4b	SP
BU824	S4b	SP
BU826	S4b	SP
BUP22*	S4b	SP
BUP23*	S4b	SP
BUS11;A	S4b	SP
BUS12;A	S4b	SP
BUS13;A	S4b	SP
BUS14;A	S4b	SP
BUS21*	S4b	SP
BUS22*	S4b	SP
BUS23*	S4b	SP

type no.	book	section	type no.	book	section	type no.	book	section
BUT11;A	S4b	SP	BUZ25	S9	PM	BUZ211	S9	PM
BUT11A	S4b	SP	BUZ31	S9	PM	BUZ307	S9	PM
BUT11AF	S4b	SP	BUZ32	S9	PM	BUZ308	S9	PM
BUV82	S4b	SP	BUZ34	S9	PM	BUZ310	S9	PM
BUV83	S4b	SP	BUZ35	S9	PM	BUZ311	S9	PM
BUV89	S4b	SP	BUZ36	S9	PM	BUZ326	S9	PM
BUV90;A	S4b	SP	BUZ41A	S9	PM	BUZ330	S9	PM
BUW11;A	S4b	SP	BUZ42	S9	PM	BUZ331	S9	PM
BUW12;A	S4b	SP	BUZ45	S9	PM	BUZ347	S9	PM
BUW13;A	S4b	SP	BUZ45A	S9	PM	BUZ348	S9	PM
BUW84	S4b	SP	BUZ45B	S9	PM	BUZ349	S9	PM
BUW85	S4b	SP	BUZ50A	S9	PM	BUZ350	S9	PM
BUX46;A	S4b	SP	BUZ50B	S9	PM	BUZ351	S9	PM
BUX47;A	S4b	SP	BUZ50C	S9	PM	BUZ355	S9	PM
BUX48;A	S4b	SP	BUZ53A	S9	PM	BUZ356	S9	PM
BUX80	S4b	SP	BUZ54	S9	PM	BUZ357	S9	PM
BUX81	S4b	SP	BUZ54A	S9	PM	BUZ358	S9	PM
BUX82	S4b	SP	BUZ60	S9	PM	BUZ384	S9	PM
BUX83	S4b	SP	BUZ63	S9	PM	BUZ385	S9	PM
BUX84	S4b	SP	BUZ64	S9	PM	BY224*	S2a	R
BUX84F	S4b	SP	BUZ71	S9	PM	BY225*	S2a	R
BUX85	S4b	SP	BUZ71A	S9	PM	BY228	S1	R
BUX85F	S4b	SP	BUZ72	S9	PM	BY229*	S2a	R
BUX86	S4b	SP	BUZ72A	S9	PM	BY229F*	S2a	R
BUX87	S4b	SP	BUZ73	S9	PM	BY249*	S2a	R
BUX88	S4b	SP	BUZ73A	S9	PM	BY260*	S2a	R
BUX90	S4b	SP	BUZ74	S9	PM	BY261*	S2a	R
BUX98	S4b	SP	BUZ74A	S9	PM	BY329*	S2a	R
BUX98A	S4b	SP	BUZ76	S9	PM	BY359*	S2a	R
BUX99	S4b	SP	BUZ76A	S9	PM	BY438	S1	R
BUY89	S4b	SP	BUZ78	S9	PM	BY448	S1	R
BUZ10	S9	PM	BUZ80	S9	PM	BY458	S1	R
BUZ11	S9	PM	BUZ80A	S9	PM	BY505	S1	R
BUZ11A	S9	PM	BUZ83	S9	PM	BY509	S1	R
BUZ14	S9	PM	BUZ83A	S9	PM	BY527	S1	R
BUZ15	S9	PM	BUZ84	S9	PM	BY584	S1	R
BUZ20	S9	PM	BUZ84A	S9	PM	BY588	S1	R
BUZ21	S9	PM	BUZ90	S9	PM	BY609	S1	R
BUZ23	S9	PM	BUZ90A	S9	PM	BY610	S1	R
BUZ24	S9	PM	BUZ94	S9	PM	BY614	S1	R

type no.	book	section
BY619	S1	R
BY620	S1	R
BY627	S1	R
BY707	S1	R
BY708	S1	R
BY709	S1	R
BY710	S1	R
BY711	S1	R
BY712	S1	R
BY713	S1	R
BY714	S1	R
BYD13 *	S1	R
BYD14 *	S1	R
BYD17 *	S1/7	R
BYD33 *	S1	R
BYD37 *	S1/7	R
BYD73 *	S1	R
BYD74 *	S1	R
BYD77 *	S1	R
BYM26 *	S1	R
BYM36 *	S1	R
BYM56 *	S1	R
BYP21*	S2a	R
BYP22*	S2a	R
BYP59*	S2a	R
BYQ28*	S2a	R
BYR29*	S2a	R
BYR29F*	S2a	R
BYT28*	S2a	R
BYT79*	S2a	R
BYV10	S1	R
BYV18*	S2a	R
BYV19*	S2a	R
BYV20*	S2a	R
BYV21*	S2a	R
BYV22*	S2a	R
BYV23*	S2a	R
BYV24*	S2a	R
BYV26 *	S1/S2a	R
BYV27*	S1/S2a	R
BYV28*	S1/S2a	R
BYV29*	S2a	R
BYV29F*	S2a	R
BYV30*	S2a	R
BYV31*	S2a	R
BYV32*	S2a	R
BYV32F*	S2a	R
BYV33*	S2a	R
BYV33F*	S2a	R
BYV34*	S2a	R
BYV36 *	S1	R
BYV39*	S2a	R
BYV42*	S2a	R
BYV43*	S2a	R
BYV43F*	S2a	R
BYV44*	S2a	R
BYV60*	S2a	R
BYV72*	S2a	R
BYV73*	S2a	R
BYV74*	S2a	R
BYV79*	S2a	R
BYV92*	S2a	R
BYV95A	S1	R
BYV95B	S1	R
BYV95C	S1	R
BYV96D	S1	R
BYV96E	S1	R
BYW25*	S2a	R
BYW29*	S2a	R
BYW29F*	S2a	R
BYW30*	S2a	R
BYW31*	S2a	R
BYW54	S1	R
BYW55	S1	R
BYW56	S1	R
BYW92*	S2a	R
BYW93*	S2a	R
BYW95A	S1	R
BYW95B	S1	R
BYW95C	S1	R
BYW96D	S1	R
BYW96E	S1	R
BYX10G	S1	R
BYX25*	S2a	R
BYX30*	S2a	R
BYX32*	S2a	R
BYX38*	S2a	R
BYX39*	S2a	R
BYX42*	S2a	R
BYX46*	S2a	R
BYX50*	S2a	R
BYX52*	S2a	R
BYX56*	S2a	R
BYX90G	S1	R
BYX96*	S2a	R
BYX97*	S2a	R
BYX98*	S2a	R
BYX99*	S2a	R
BZD23	S1	Vrg
BZD27	S1/7	Vrg
BZT03	S1	Vrg
BZV10	S1	Vrf
BZV11	S1	Vrf
BZV12	S1	Vrf
BZV13	S1	Vrf
BZV14	S1	Vrf
BZV37	S1	Vrf
BZV46	S1	Vrg
BZV49*	S1/S7	Vrg/Mm
BZV55*	S7	Mm
BZV80	S1	Vrf
BZV81	S1	Vrf
BZV85 *	S1	Vrg
BZW03 *	S1	Vrg
BZW14	S1	Vrg
BZW86*	S2a	TS
BZX55 *	S1	Vrg
BZX70*	S2a	Vrg
BZX75 *	S1	Vrg
BZX79*	S1	Vrg

type no.	book	section
BZX84*	S7/S1	Mm/Vrg
BZY91*	S2a	Vrg
BZY93*	S2a	Vrg
CFX13	S11	M
CFX21	S11	M
CFX30	S11	M
CFX31	S11	M
CFX32	S11	M
CFX33	S11	M
CNG35	S8b	PhC
CNG36	S8b	PhC
CNR36	S8b	PhC
CNX21	S8b	PhC
CNX35	S8b	PhC
CNX35U	S8b	PhC
CNX36	S8b	PhC
CNX36U	S8b	PhC
CNX38	S8b	PhC
CNX38U	S8b	PhC
CNX39	S8b	PhC
CNX39U	S8b	PhC
CNX44	S8b	PhC
CNX44A	S8b	PhC
CNX46	S8b	PhC
CNX48	S8b	PhC
CNX48U	S8b	PhC
CNX62	S8b	PhC
CNX72	S8b	PhC
CNX82	S8b	PhC
CNX83	S8b	PhC
CNX91	S8b	PhC
CNX92	S8b	PhC
CNY17-1	S8b	PhC
CNY17-2	S8b	PhC
CNY17-3	S8b	PhC
CNY50	S8b	PhC
CNY57	S8b	PhC
CNY57A	S8b	PhC
CNY57AU	S8b	PhC
CNY57U	S8b	PhC
CNY62	S8b	PhC
CNY63	S8b	PhC
CQF24	S8b	Ph
CQL10A	S8b	Ph
CQL13A	S8b	Ph
CQL16	S8b	Ph
CQS51L	S8a	LED
CQS54	S8a	LED
CQS82L	S8a	LED
CQS82AL	S8a	LED
CQS84L	S8a	LED
CQS86L	S8a	LED
CQS93	S8a	LED
CQS93E	S8a	LED
CQS93L	S8a	LED
CQS95	S8a	LED
CQS95E	S8a	LED
CQS95L	S8a	LED
CQS97	S8a	LED
CQS97E	S8a	LED
CQS97L	S8a	LED
CQT10B	S8a	LED
CQT24	S8a	LED
CQT60	S8a	LED
CQT70	S8a	LED
CQT80L	S8a	LED
CQV70(L)	S8a	LED
CQV70A(L)	S8a	LED
CQV70U(L)	S8a	LED
CQV71A(L)	S8a	LED
CQV72(L)	S8a	LED
CQV80L	S8a	LED
CQV80AL	S8a	LED
CQV80UL	S8a	LED
CQV81L	S8a	LED
CQV82L	S8a	LED
CQW10A(L)	S8a	LED
CQW10B(L)	S8a	LED
CQW10U(L)	S8a	LED
CQW11B(L)	S8a	LED
CQW12B(L)	S8a	LED
CQW20A	S8a	LED
CQW21	S8a	LED
CQW22	S8a	LED
CQW24(L)	S8a	LED
CQW54	S8a	LED
CQW60(L)	S8a	LED
CQW60A(L)	S8a	LED
CQW60U(L)	S8a	LED
CQW61(L)	S8a	LED
CQW62(L)	S8a	LED
CQW89A	S8a/b	I
CQW93	S8a	LED
CQW95	S8a	LED
CQW97	S8a	LED
CQX24(L)	S8a	LED
CQX51(L)	S8a	LED
CQX54(L)	S8a	LED
CQX54D	S8a	LED
CQX64(L)	S8a	LED
CQX64D	S8a	LED
CQX74(L)	S8a	LED
CQX74D	S8a	LED
CQY11B	S8b	LED
CQY11C	S8b	LED
CQY24B(L)	S8a	LED
CQY49B	S8b	LED
CQY49C	S8b	LED
CQY50	S8b	LED
CQY52	S8b	LED
CQY53S	S8b	LED
CQY54A	S8a	LED
CQY58A	S8a/b	I
CQY89A	S8a/b	I
CQY94B(L)	S8a	LED
CQY95B	S8a	LED
CQY96(L)	S8a	LED
CQY97A	S8a	LED
Fresnel-lens	S8b	A

type no.	book	section
H11A1	S8b	PhC
H11A2	S8b	PhC
H11A3	S8b	PhC
H11A4	S8b	PhC
H11A5	S8b	PhC
H11B1	S8b	PhC
H11B2	S8b	PhC
H11B3	S8b	PhC
H11B255	S8b	PhC
KMZ10A	S13	SEN
KMZ10B	S13	SEN
KMZ10C	S13	SEN
KP100A	S13	SEN
KP101A	S13	SEN
KPZ20G	S13	SEN
KPZ21G	S13	SEN
KTY81*	S13	SEN
KTY83*	S13	SEN
KTY84*	S13	SEN
LAE2001R	S11	M
LAE4000Q	S11	M
LAE4001R	S11	M
LAE4002S	S11	M
LAE6000Q	S11	M
LBE1004R	S11	M
LBE1010R	S11	M
LBE2003S	S11	M
LBE2005Q	S11	M
LBE2008T	S11	M
LBE2009S	S11	M
LCE1010R	S11	M
LCE2003S	S11	M
LCE2005Q	S11	M
LCE2008T	S11	M
LCE2009S	S11	M
LJE42002T	S11	M
LKE1004R	S11	M
LKE2002T	S11	M
LKE2004T	S11	M
LKE2015T	S11	M
LKE21004R	S11	M
LKE21015T	S11	M
LKE21050T	S11	M
LKE27010R	S11	M
LKE27025R	S11	M
LKE32002T	S11	M
LKE32004T	S11	M
LTE42005S	S11	M
LTE42008R	S11	M
LTE42012R	S11	M
LV1721E50R	S11	M
LV2024E45R	S11	M
LV2327E40R	S11	M
LV3742E16R	S11	M
LV3742E24R	S11	M
LWE2015R	S11	M
LWE2025R	S11	M
LZ1418E100R	S11	M
MCA230	S8b	PhC
MCA231	S8b	PhC
MCA255	S8b	PhC
MCT2	S8b	PhC
MCT26	S8b	PhC
MKB12040WS	S11	M
MKB12100WS	S11	M
MKB12140W	S11	M
MO6075B200Z	S11	M
MO6075B400Z	S11	M
MPS6513	S3	Sm
MPS6514	S3	Sm
MPS6515	S3	Sm
MPS6517	S3	Sm
MPS6518	S3	Sm
MPS6519	S3	Sm
MPS6520	S3	Sm
MPS6521	S3	Sm
MPS6522	S3	Sm
MPS6523	S3	Sm
MPSA05	S3	Sm
MPSA06	S3	Sm
MPSA13	S3	Sm
MPSA14	S3	Sm
MPSA42	S3	Sm
MPSA43	S3	Sm
MPSA55	S3	Sm
MPSA56	S3	Sm
MPSA63	S3	Sm
MPSA64	S3	Sm
MPSA92	S3	Sm
MPSA93	S3	Sm
MRB12175YR	S11	M
MRB12350YR	S11	M
MS1011B700Y	S11	M
MS6075B800Z	S11	M
MSB12900Y	S11	M
MZ0912B75Y	S11	M
MZ0912B150Y	S11	M
OM286; M	S13	SEN
OM287; M	S13	SEN
OM320	S10	WBM
OM321	S10	WBM
OM322	S10	WBM
OM323	S10	WBM
OM323A	S10	WBM
OM335	S10	WBM
OM336	S10	WBM
OM337	S10	WBM
OM337A	S10	WBM
OM339	S10	WBM
OM345	S10	WBM
OM350	S10	WBM
OM360	S10	WBM
OM361	S10	WBM
OM370	S10	WBM
OM386B	S13	SEN
OM386M	S13	SEN
OM387B	S13	SEN
OM387M	S13	SEN
OM388B	S13	SEN
OM389B	S13	SEN

type no.	book	section
OM931	S4a	P
OM961	S4a	P
OSB9115	S2a	St
OSB9215	S2a	St
OSB9415	S2a	St
OSM9115	S2a	St
OSM9215	S2a	St
OSM9415	S2a	St
OSM9510	S2a	St
OSM9511	S2a	St
OSM9512	S2a	St
OSS9115	S2a	St
OSS9215	S2a	St
OSS9415	S2a	St
P2105	S8b	I
PBMF4391	S5	FET
PBMF4392	S5	FET
PBMF4393	S5	FET
PDE1001U	S11	M
PDE1003U	S11	M
PDE1005U	S11	M
PDE1010U	S11	M
PEE1001U	S11	M
PEE1003U	S11	M
PEE1005U	S11	M
PEE1010U	S11	M
PH2222	S3	Sm
PH2222A	S3	Sm
PH2369	S3	Sm
PH2907	S3	Sm
PH2907A	S3	Sm
PH2955T	S4a	P
PH3055T	S4a	P
PH5415	S3	Sm
PH5416	S3	Sm
PH13002	S4b	SP
PH13003	S4b	SP
PHSD51	S2a	R
PKB3001U	S11	M
PKB3003U	S11	M
PKB3005U	S11	M
PKB12005U	S11	M
PKB20010U	S11	M
PKB23001U	S11	M
PKB23003U	S11	M
PKB23005U	S11	M
PKB25006T	S11	M
PKB32001U	S11	M
PKB32003U	S11	M
PKB32005U	S11	M
PMBF4391	S7	Mm
PMBF4392	S7	Mm
PMBF4393	S7	Mm
PMBT2222/A	S7	Mm
PMBT2907/A	S7	Mm
PMBT3903/4	S7	Mm
PMBT3906	S7	Mm
PMBT6428/9	S7	Mm
PMBTA05/06	S7	Mm
PMBTA13/14	S7	Mm
PMBTA42/43	S7	Mm
PMBTA55/56	S7	Mm
PMBTA63/64	S7	Mm
PMBTA92/93	S7	Mm
PMLL4148	S1	SD
PMLL4150	S1	SD
PMLL4151	S1	SD
PMLL4153	S1	SD
PMLL4446	S1	SD
PMLL4448	S1	SD
PMLL5225B to PMLL5267B	S1/S7	SD
PN2222	S3	Sm
PN2222A	S3	Sm
PN2369	S3	Sm
PN2369A	S3	Sm
PN2907	S3	Sm
PN2907A	S3	Sm
PN3439	S3	Sm
PN3440	S3	Sm
PN5415	S3	Sm
PN5416	S3	Sm
PO44	S8b	PhC
PO44A	S8b	PhC
PPC5001T	S11	M
PQC5001T	S11	M
PTB23001X	S11	M
PTB23003X	S11	M
PTB23005X	S11	M
PTB32001X	S11	M
PTB32003X	S11	M
PTB32005X	S11	M
PTB42001X	S11	M
PTB42002X	S11	M
PTB42003X	S11	M
PV3742B4X	S11	M
PVB42004X	S11	M
PXT3904	S7	Mm
PXT3906	S7	Mm
PZ1418B15U	S11	M
PZ1418B30U	S11	M
PZ1721B12U	S11	M
PZ1721B25U	S11	M
PZ2024B10U	S11	M
PZ2024B20U	S11	M
PZB16035U	S11	M
PZB27020U	S11	M
RPY97	S8b	I
RPY100	S8b	I
RPY101	S8b	I
RPY102	S8b	I
RPY103	S8b	I
RPY107	S8b	I
RPY109	S8b	I
RV3135B5X	S11	M
RX1214B300Y	S11	M
RXB12350Y	S11	M
RZ1214B35Y	S11	M
RZ1214B60W	S11	M

type no.	book	section	type no.	book	section	type no.	book	section
RZ1214B65Y	S11	M	TIP125	S4a	P	1N4003G	S1	R
RZ1214B125W	S11	M	TIP126	S4a	P	1N4004G	S1	R
RZ1214B125Y	S11	M	TIP127	S4a	P	1N4005G	S1	R
RZ1214B150Y	S11	M	TIP130	S4a	P	1N4006G	S1	R
RZ2833B45W	S11	M	TIP131	S4a	P	1N4007G	S1	R
RZ3135B15U	S11	M	TIP132	S4a	P	1N4148	S1	SD
RZ3135B15W	S11	M	TIP135	S4a	P	1N4150	S1	SD
RZ3135B25U	S11	M	TIP136	S4a	P	1N4151	S1	SD
RZ3135B30W	S11	M	TIP137	S4a	P	1N4153	S1	SD
RZB12100Y	S11	M	TIP140	S4a	P	1N4446	S1	SD
RZB12250Y	S11	M	TIP141	S4a	P	1N4448	S1	SD
RZZ1214B300Y	S11	M	TIP145	S4a	P	1N4531	S1	SD
SL5500	S8b	PhC	TIP146	S4a	P	1N4532	S1	SD
SL5501	S8b	PhC	TIP147	S4a	P	1N5059	S1	R
SL5502R	S8b	PhC	TIP2955	S4a	P	1N5060	S1	R
SL5504	S8b	PhC	TIP3055	S4a	P	1N5061	S1	R
SL5504S	S8b	PhC	1N821;A	S1	Vrf	1N5062	S1	R
SL5505S	S8b	PhC	1N823;A	S1	Vrf	2N918	S10	WBT
SL5511	S8b	PhC	1N825;A	S1	Vrf	2N930	S3	Sm
TIP29*	S4a	P	1N827;A	S1	Vrf	2N1613	S3	Sm
TIP30*	S4a	P	1N829;A	S1	Vrf	2N1711	S3	Sm
TIP31*	S4a	P	1N914	S1	SD	2N1893	S3	Sm
TIP32*	S4a	P	1N916	S1	SD	2N2219	S3	Sm
TIP33*	S4a	P	1N3879	S2a	R	2N2219A	S3	Sm
TIP34*	S4a	P	1N3880	S2a	R	2N2222	S3	Sm
TIP41*	S4a	P	1N3881	S2a	R	2N2222A	S3	Sm
TIP42*	S4a	P	1N3882	S2a	R	2N2297	S3	Sm
TIP47	S4a	P	1N3883	S2a	R	2N2368	S3	Sm
TIP48	S4a	P	1N3889	S2a	R	2N2369	S3	Sm
TIP49	S4a	P	1N3890	S2a	R	2N2369A	S3	Sm
TIP50	S4a	P	1N3891	S2a	R	2N2483	S3	Sm
TIP110	S4a	P	1N3892	S2a	R	2N2484	S3	Sm
TIP111	S4a	P	1N3893	S2a	R	2N2904	S3	Sm
TIP112	S4a	P	1N3909	S2a	R	2N2904A	S3	Sm
TIP115	S4a	P	1N3910	S2a	R	2N2905	S3	Sm
TIP116	S4a	P	1N3911	S2a	R	2N2905A	S3	Sm
TIP117	S4a	P	1N3912	S2a	R	2N2906	S3	Sm
TIP120	S4a	P	1N3913	S2a	R	2N2906A	S3	Sm
TIP121	S4a	P	1N4001G	S1	R	2N2907	S3	Sm
TIP122	S4a	P	1N4002G	S1	R	2N2907A	S3	Sm

type no.	book	section
2N3019	S3	Sm
2N3020	S3	Sm
2N3053	S3	Sm
2N3375	S6	RFP
2N3553	S6	RFP
2N3632	S6	RFP
2N3822	S5	FET
2N3823	S5	FET
2N3866	S6	RFP
2N3903	S3	Sm
2N3904	S3	Sm
2N3905	S3	Sm
2N3906	S3	Sm
2N3924	S6	RFP
2N3926	S6	RFP
2N3927	S6	RFP
2N3966	S5	FET
2N4030	S3	Sm
2N4031	S3	Sm
2N4032	S3	Sm
2N4033	S3	Sm
2N4091	S5	FET
2N4092	S5	FET
2N4093	S5	FET
2N4123	S3	Sm
2N4124	S3	Sm
2N4125	S3	Sm
2N4126	S3	Sm
2N4391	S5	FET
2N4392	S5	FET
2N4393	S5	FET
2N4400	S3	Sm
2N4401	S3	Sm
2N4402	S3	Sm
2N4403	S3	Sm
2N4427	S6	RFP
2N4856	S5	FET
2N4857	S5	FET
2N4858	S5	FET
2N4859	S5	FET
2N4860	S5	FET
2N4861	S5	FET
2N5086	S3	Sm
2N5087	S3	Sm
2N5088	S3	Sm
2N5089	S3	Sm
2N5400	S3	Sm
2N5401	S3	Sm
2N5415	S3	Sm
2N5416	S3	Sm
2N5550	S3	Sm
2N5551	S3	Sm
2N6659	S5	FET
2N6660	S5	FET
2N6661	S5	FET
4N25	S8b	PhC
4N25A	S8b	PhC
4N26	S8b	PhC
4N27	S8b	PhC
4N28	S8b	PhC
4N35	S8b	PhC
4N36	S8b	PhC
4N37	S8b	PhC
4N38	S8b	PhC
4N38A	S8b	PhC
502CQF	S8b	Ph
503CQF	S8b	Ph
504CQL	S8b	Ph
516CQF-B	S8b	Ph
56201d	S4b	A
56201j	S4b	A
56245	S3,10	A
56246	S3,10	A
56261a	S4b	A
56264	S2a/b	A
56295	S2a/b	A
56326	S4b	A
56339	S4b	A
56352	S4b	A
56353	S4b	A
56354	S4b	A
56359b	S2,4b	A
56359c	S2,4b	A
56359d	S2,4b	A
56360a	S2,4b	A
56363	S2,4b	A
56364	S2,4b	A
56367	S2a/b	A
56368b	S2,4b	A
56368c	S2,4b	A
56369	S2,4b	A
56378	S2,4b	A
56379	S2,4b	A
56387a,b	S4b	A
56397	S8b	A

NOTES

NOTES

NOTES

DATA HANDBOOK SYSTEM

DATA HANDBOOK SYSTEM

Our Data Handbook System comprises more than 60 books with specifications on electronic components, subassemblies and materials. It is made up of four series of handbooks:

ELECTRON TUBES	BLUE
SEMICONDUCTORS	RED
INTEGRATED CIRCUITS	PURPLE
COMPONENTS AND MATERIALS	GREEN

The contents of each series are listed on pages iv to vii.

The data handbooks contain all pertinent data available at the time of publication, and each is revised and reissued periodically.

When ratings or specifications differ from those published in the preceding edition they are indicated with arrows in the page margin. Where application information is given it is advisory and does not form part of the product specification.

Condensed data on the preferred products of Philips Electronic Components and Materials Division is given in our Preferred Type Range catalogue (issued annually).

Information on current Data Handbooks and on how to obtain a subscription for future issues is available from any of the Organizations listed on the back cover.

Product specialists are at your service and enquiries will be answered promptly.

ELECTRON TUBES (BLUE SERIES)

The blue series of data handbooks comprises:

T1	**Tubes for r.f. heating**
T2a	**Transmitting tubes for communications, glass types**
T2b	**Transmitting tubes for communications, ceramic types**
T3	**Klystrons**
T4	**Magnetrons for microwave heating**
T5	**Cathode-ray tubes** Instrument tubes, monitor and display tubes, C.R. tubes for special applications
T6	**Geiger-Muller tubes**
T8	**Colour display systems** Colour TV picture tubes, colour data graphic display tube assemblies, deflection units
T9	**Photo and electron multipliers**
T10	**Plumbicon camera tubes and accessories**
T11	**Microwave semiconductors and components**
T12	**Vidicon and Newvicon camera tubes**
T13	**Image intensifiers and infrared detectors**
T15	**Dry reed switches**
T16	**Monochrome tubes and deflection units** Black and white TV picture tubes, monochrome data graphic display tubes, deflection units

SEMICONDUCTORS (RED SERIES)

The red series of data handbooks comprises:

S1	**Diodes** Small-signal silicon diodes, voltage regulator diodes (<1,5 W), voltage reference diodes, tuner diodes, rectifier diodes
S2a	**Power diodes**
S2b	**Thyristors and triacs**
S3	**Small-signal transistors**
S4a	**Low-frequency power transistors and hybrid modules**
S4b	**High-voltage and switching power transistors**
S5	**Field-effect transistors**
S6	**R.F. power transistors and modules**
S7	**Surface mounted semiconductors**
S8a	**Light-emitting diodes**
S8b	**Devices for optoelectronics** Optocouplers, photosensitive diodes and transistors, infrared light-emitting diodes and infrared sensitive devices, laser and fibre-optic components
S9	**PowerMOS transistors**
S10	**Wideband transistors and wideband hybrid IC modules**
S11	**Microwave transistors**
S12	**Surface acoustic wave devices**
S13	**Semiconductor sensors**
S14	**Liquid Crystal Displays**

INTEGRATED CIRCUITS (PURPLE SERIES)

The purple series of handbooks comprises:

IC01	Radio, audio and associated systems Bipolar, MOS	
IC02a/b	Video and associated systems Bipolar, MOS	
IC03	Integrated circuits for telephony Bipolar, MOS	
IC04	HE4000B logic family CMOS	
IC05N	HE4000B logic family – uncased ICs CMOS	
IC06N	High-speed CMOS; PC74HC/HCT/HCU Logic family	
IC08	ECL 10K and 100K logic families	
IC09N	TTL logic series	
IC10	Memories MOS, TTL, ECL	
IC11	Linear Products	
IC12	I^2C-bus compatible ICs	
IC13	Semi-custom Programmable Logic Devices (PLD)	
IC14	Microcontrollers and peripherals Bipolar, MOS	
IC15	FAST TTL logic series	
IC16	CMOS integrated circuits for clocks and watches	
IC17	Integrated Services Digital Networks (ISDN)	not yet issued
IC18	Microprocessors and peripherals	

COMPONENTS AND MATERIALS (GREEN SERIES)

The green series of data handbooks comprises:

C2	**Television tuners, coaxial aerial input assemblies**
C3	**Loudspeakers**
C4	**Ferroxcube potcores, square cores and cross cores**
C5	**Ferroxcube for power, audio/video and accelerators**
C6	**Synchronous motors and gearboxes**
C7	**Variable capacitors**
C8	**Variable mains transformers**
C9	**Piezoelectric quartz devices**
C11	**Varistors, thermistors and sensors**
C12	**Potentiometers, encoders and switches**
C13	**Fixed resistors**
C14	**Electrolytic and solid capacitors**
C15	**Ceramic capacitors**
C16	**Permanent magnet materials**
C17	**Stepping motors and associated electronics**
C18	**Direct current motors**
C19	**Piezoelectric ceramics**
C20	**Wire-wound components for TVs and monitors**
C22	**Film capacitors**

Electronic components and materials for professional, industrial and consumer uses from the world-wide Philips Group of Companies

Argentina: PHILIPS ARGENTINA S.A., Div. Elcoma, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541 - 7141 to 7747.
Australia: PHILIPS INDUSTRIES LTD., Elcoma Division, 11 Waltham Street, ARTARMON, N.S.W. 2064, Tel. (02) 439 3322.
Austria: ÖSTERREICHISCHE PHILIPS INDUSTRIE G.m.b.H., UB Bauelemente, Triester Str. 64, A-1101 WIEN, Tel. (0222) 62 91 11-0.
Belgium: N.V. PHILIPS & MBLE ASSOCIATED, 80 Rue Des Deux Gares, B-1070 BRUXELLES, Tel. (02) 525-61-11.
Brazil: CONSTANTA-IBRAPE; (Active Devices): Av. Brigadeiro Faria Lima, 1735-SAO PAULO-SP, Tel. (011) 211-2600,
(Passive Devices & Materials): Av. Francisco Monteiro, 702 - RIBEIRAO PIRES-SP, Tel. (011) 459-8211.
Canada: PHILIPS ELECTRONICS LTD., Elcoma Division, 601 Milner Ave., SCARBOROUGH, Ontario, M1B 1M8, Tel. (416) 292-5161.
Chile: PHILIPS CHILENA S.A., Av. Santa Maria 0760, SANTIAGO, Tel. (02) 77 38 16.
Colombia: IND. PHILIPS DE COLOMBIA S.A., c/o IPRELENSO LTD., Cra. 21, No. 56-17, BOGOTA, D.E., Tel. (01) 2 49 76 24.
Denmark: MINIWATT A/S, Strandlodsvej 2, P.O. Box 1919, DK 2300 COPENHAGEN S, Tel. (01) 54 11 33.
Finland: OY PHILIPS AB, Elcoma Division, Kaivokatu 8, SF-00100 HELSINKI 10, Tel. (90) 1 72 71.
France: RTC-COMPELEC, 130 Avenue Ledru Rollin, F-75540 PARIS 11, Tel. (01) 43 38 80 00.
Germany (Fed. Republic): VALVO, UB Bauelemente der Philips G.m.b.H., Valvo Haus, Burchardstrasse 19, D-2 HAMBURG 1, Tel. (040) 3296-0.
Greece: PHILIPS HELLENIQUE S.A., Elcoma Division, No. 15, 25th March Street, GR 17778 TAVROS, Tel. (01) 48 94 339/48 94 911.
Hong Kong: PHILIPS HONG KONG LTD., Elcoma Div., 15/F Philips Ind. Bldg., 24-28 Kung Yip St., KWAI CHUNG, Tel. (0)-24 51 21.
India: PEICO ELECTRONICS & ELECTRICALS LTD., Elcoma Dept., Band Box Building,
254-D Dr. Annie Besant Rd., BOMBAY - 400 025, Tel. (022) 4930311/4930590.
Indonesia: P.T. PHILIPS-RALIN ELECTRONICS, Elcoma Div., Setiabudi II Building, 6th Fl., Jalan H.R. Rasuna Said (P.O. Box 223/KBY) Kuningan,
JAKARTA 12910, Tel. (021) 51 79 95.
Ireland: PHILIPS ELECTRICAL (IRELAND) LTD., Elcoma Division, Newstead, Clonskeagh, DUBLIN 14, Tel. (01) 69 33 55.
Italy: PHILIPS S.p.A., Div. Componenti Elcoma, Piazza IV Novembre 3, I-20124 MILANO, Tel. (02) 6752.1.
Japan: NIHON PHILIPS CORP., Shuwa Shinagawa Bldg., 26-33 Takanawa 3-chome, Minato-ku, TOKYO (108), Tel. (03) 448-5611.
(IC Products) SIGNETICS JAPAN LTD., 8-7 Sanbancho Chiyoda-ku, TOKYO 102, Tel. (03) 230-1521.
Korea (Republic of): PHILIPS ELECTRONICS (KOREA) LTD., Elcoma Div., Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. (02) 794-5011.
Malaysia: PHILIPS MALAYSIA SDN BHD, Elcoma Div., 345 Jalan Gelugor, 11700 PULAU PINANG, Tel. (04) 87 00 44.
Mexico: ELECTRONICA, S.A de C.V., Carr. México-Toluca km. 62.5, TOLUCA, Edo. de México 50140, Tel. Toluca 91 (721) 613-00.
Netherlands: PHILIPS NEDERLAND, Marktgroep Elonco, Postbus 90050, 5600 PB EINDHOVEN, Tel. (040) 78 37 49.
New Zealand: PHILIPS NEW ZEALAND LTD., Elcoma Division, 110 Mt. Eden Road, C.P.O. Box 1041, AUCKLAND, Tel. (09) 605-914.
Norway: NORSK A/S PHILIPS, Electronica Dept., Sandstuveien 70, OSLO 6, Tel. (02) 68 02 00.
Pakistan: PHILIPS ELECTRICAL CO. OF PAKISTAN LTD., Philips Markaz, M.A. Jinnah Rd., KARACHI-3, Tel. (021) 72 57 72.
Peru: CADESA, Av. Alfonso Ugarte 1268, LIMA 5, Tel. (014) 326070.
Philippines: PHILIPS INDUSTRIAL DEV. INC., 2246 Pasong Tamo, P.O. Box 911, Makati Comm. Centre, MAKATI-RIZAL 3116, Tel. (02) 86 89 51 to 59.
Portugal: PHILIPS PORTUGUESA S.A.R.L., Av. Eng. Duarte Pacheco 6, 1009 LISBOA Codex, Tel. (019) 68 31 21.
Singapore: PHILIPS PROJECT DEV. (Singapore) PTE LTD., Elcoma Div., Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. 35 02 000.
South Africa: S.A. PHILIPS (Pty) LTD., EDAC Div., 3rd Floor Rainer House, Upper Railway Rd. & Ove St., New Doornfontein, JOHANNESBURG 2001,
Tel. (011) 402-4600/07.
Spain: MINIWATT S.A., Balmes 22, BARCELONA 7, Tel. (03) 301 63 12.
Sweden: PHILIPS KOMPONENTER A.B., Lidingövägen 50, S-11584 STOCKHOLM 27, Tel. (08) 7821000.
Switzerland: PHILIPS A.G., Elcoma Dept., Allmendstrasse 140-142, CH-8027 ZÜRICH, Tel. (01) 488 22 11.
Taiwan: PHILIPS TAIWAN LTD., 150 Tun Hua North Road, P.O. Box 22978, TAIPEI, Taiwan, Tel. (02) 7120500.
Thailand: PHILIPS ELECTRICAL CO. OF THAILAND LTD., 283 Silom Road, P.O. Box 961, BANGKOK, Tel. (02) 233-6330-9.
Turkey: TÜRK PHILIPS TICARET A.S., Elcoma Department, Inönü Cad., No. 78-80, 80090 Ayazpasa ISTANBUL, Tel. (01) 143 59 10.
United Kingdom: MULLARD LTD., Mullard House, Torrington Place, LONDON WC1E 7HD, Tel. (01) 580 6633.
United States: (Active Devices & Materials) AMPEREX SALES CORP., Providence Pike, SLATERSVILLE, R.I. 02876, Tel. (401) 762-9000.
(Passive & Electromech. Dev.) MEPCO/CENTRALAB, INC., 2001 West Blue Heron Blvd, RIVIERA BEACH, Florida 33404,
Tel. (305) 881-3200.
(IC Products) SIGNETICS CORPORATION, 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. (408) 991-2000.
Uruguay: LUZILECTRON S.A., Avda Uruguay 1287, P.O. Box 907, MONTEVIDEO, Tel. (02) 98 53 95.
Venezuela: IND. VENEZOLANAS PHILIPS S.A., c/o MAGNETICA S.A., Calle 6, Ed. Las Tres Jotas, App. Post. 78117, CARACAS, Tel. (02) 239 39 31.

For all other countries apply to: Philips Electronic Components and Materials Division, International Business Relations, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Telex 35000 phtcnl

AS56

© Philips Export B.V. 1987

This information is furnished for guidance, and with no guarantee as to its accuracy or completeness; its publication conveys no licence under any patent or other right, nor does the publisher assume liability for any consequence of its use; specifications and availability of goods mentioned in it are subject to change without notice; it is not to be reproduced in any way, in whole or in part, without the written consent of the publisher.

Printed in The Netherlands

Date of release:

9398 148 80011